INTERNATIONAL TELECOMMUNICATION UNION

ITU-T V.300

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TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

SERIES V: DATA COMMUNICATION OVER THE TELEPHONE NETWORK

Modems on digital circuits

A 128 (144) kbit/s data circuit-terminating equipment standardized for use on digital point-to-point leased circuits

ITU-T Recommendation V.300

(Previously CCITT Recommendation)

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ITU-T RECOMMENDATION V.300

A 128 (144) kbit/s DATA CIRCUIT-TERMINATING EQUIPMENT STANDARDIZED FOR USE ON DIGITAL POINT-TO-POINT LEASED CIRCUITS

Summary

This Recommendation specifies the necessary functions of a 64, 128 and 144 kbit/s DCE for the provision of digital leased circuits. Interworking with DCEs complying with Recommendation V.38 is covered. The recommended functions also allow this DCE to be deployed as a remote access to a flexible multiplexer as specified in Recommendation G.797.

The V.24 and X.24 DTE-DCE interfaces are specified in terms of functions and electrical characteristics. The use of additional interfaces is not precluded. Core functions include scrambling of data, testing facilities, optional aggregation function and optional multiplexing function. This type of DCE may be part of a managed network.

This Recommendation contains three appendices providing information on complementary functions or applications for this type of equipment.

Source

ITU-T Recommendation V.300 was prepared by ITU-T Study Group 15 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 2nd of July 1999.

FOREWORD

ITU (International Telecommunication Union) is the United Nations Specialized Agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the ITU. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation the term *recognized operating agency (ROA)* includes any individual, company, corporation or governmental organization that operates a public correspondence service. The terms *Administration*, *ROA* and *public correspondence* are defined in the *Constitution of the ITU (Geneva, 1992)*.

INTELLECTUAL PROPERTY RIGHTS

The ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. The ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, the ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

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Recommendation V.300

A 128 (144) kbit/s DATA CIRCUIT-TERMINATING EQUIPMENT STANDARDIZED FOR USE ON DIGITAL POINT-TO-POINT LEASED CIRCUITS

(Geneva, 1999)

1 Scope

This data circuit-terminating equipment (DCE) is intended for use on $n \times 64$ kbit/s based digital point-to-point leased circuits other than ISDN. Signalling rates supported by the equipment are 64 kbit/s and 128 kbit/s. This may be expanded to 144 kbit/s when a digital leased line network supports this type of connection, or for DCE interconnection on short haul leased circuits employing metallic pair(s). The DCE is specified herein in terms of the DTE-to-DCE interface(s) and features including rate adaptation, end-to-end signalling, testing and multiplexing facilities. The line signal and the line signalling rate that are used to connect this type of DCE locally to a number of 64 kbit/s or 128 kbit/s or 144 kbit/s, digital bearer circuit(s) are considered to be national matters, and are hence not specified herein. The transmission scheme chosen should, however, be capable of providing an octet timing recovery where a multiplexing function as specified in clause 9 is employed.

The principal characteristics of the DCE are as follows:

a) duplex mode of operation on digital leased circuits;

b) signalling rates of 64 and 128/144 kbit/s;

c) inclusion of two (Note 3) different types of DTE-DCE functional interfaces;

d) inclusion of testing facilities;

e) optional provision of a means to differentiate between user and network data;

f) optional inclusion of a multiplexer (for further study);

g) optional inclusion of an equipment management function;

h) inclusion of an optional aggregation function;

i) backward compatibility with a DCE according to Recommendation V.38 [4].

NOTE 1 – Figure I.1 gives a schematic block diagram of the arrangement of functional blocks (without the multiplexer function) inside the DCE.

NOTE 2 – The term "line signalling rate" as used in the context of this Recommendation refers to the signalling rate at the input of the transmitter of the transmission unit (see Figure I.1).

NOTE 3 – The use of additional DTE-DCE interfaces, e.g. codirectional G.703 64 kbit/s [9], I.430 [11] or G.703/G.704 [9]/[10] is not precluded.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in the text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation V.10 (1993), *Electrical characteristics for unbalanced double-current interchange circuits operating at data signalling rates nominally up to 100 kbit/s*.

[2] ITU-T Recommendation V.11 (1996), *Electrical characteristics for balanced double-current interchange circuits operating at data signalling rates up to 10 Mbit/s*.

[3] ITU-T Recommendation V.24 (1996), *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE).*

[4] ITU-T Recommendation V.38 (1996), *A 48/56/64 kbit/s data circuit-terminating equipment standardized for use on digital point-to-point leased circuits*.

[5] CCITT Recommendation V.54 (1988), *Loop test devices for modems*.

[6] CCITT Recommendation X.21 (1992), *Interface between data terminal equipment and data circuit-terminating equipment for synchronous operation on public networks*.

[7] CCITT Recommendation X.24 (1988), *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks*.

[8] CCITT Recommendation X.150 (1988), *Principles of maintenance testing for public data networks using data terminal equipment (DTE) and data circuit-terminating equipment (DCE) test loops*.

[9] ITU-T Recommendation G.703, (1998), *Physical/electrical characteristics of hierarchical digital interfaces*.

[10] ITU-T Recommendation G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels.*

[11] ITU-T Recommendation I.430 (1995), *Basic user-network interface – Layer 1 specification*.

[12] CCITT Recommendation O.153 (1992), *Basic parameters for the measurement of error performance at bit rates below the primary rate*.

[13] ISO 4902:1989, *Information technology – Data communication – 37-pole DTE/DCE interface connector and contact number assignments*.

[14] ISO 4903:1989, *Information technology – Data communication – 15-pole DTE/DCE interface connector and contact number assignments*.

[15] ISO/IEC 11569:1993, *Information technology – Telecommunications and information exchange between systems – 26-pole interface connector mateability dimensions and contact number assignments*.

3 Abbreviations

This Recommendation uses the following abbreviations:

AIS Alarm Indication Signal

DCE Data Circuit-terminating Equipment

DTE Data Terminal Equipment

4 Signalling rates

4.1 Data signalling rates

The recommended data signalling rate (user rate) is synchronous at 128 kbit/s (144 kbit/s may also be supported).

4.2 Signalling rates on line

Data at either signalling rate may be supported by a digital bearer circuit being accessed with a line signalling rate that depends upon the leased line network implementation. This is not in the scope of this Recommendation. Appendix III depicts such an example with a 160 kbit/s line signalling rate.

5 Differentiation between user and network data signals

An optional scrambler/descrambler may be provided as a means of differentiating between user data and network data or network signalling towards the DCE [e.g. loss of synchronization or alarm indication signal (AIS)], and for fault detection. Where the scrambler/descrambler is provided, its use shall be subject to bilateral agreement between the Administrations concerned.

NOTE – The potential provision of an additional scrambler/descrambler inside the transmission unit of the DCE (see Figure I.1) is a national matter, and outside the scope of this Recommendation.

5.1 Scrambler

Where provided, the following self-synchronizing scrambler having the generating polynomial $1 + x^{-18} + x^{-23}$ shall be used for the transmitter of the DCE.

The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. The scrambler data output sequence thus shall be:

$$D_s = D_i \oplus D_s \cdot x^{-18} \oplus D_s \cdot x^{-23}$$

where:

D_s is the data sequence at the output of the scrambler

D_i is the data sequence applied to the scrambler

D_o is the data sequence at the output of the descrambler (see 5.2)

$\oplus$ denotes modulo 2 addition

$\cdot$ denotes binary multiplication

Figure 1 shows a suitable implementation.

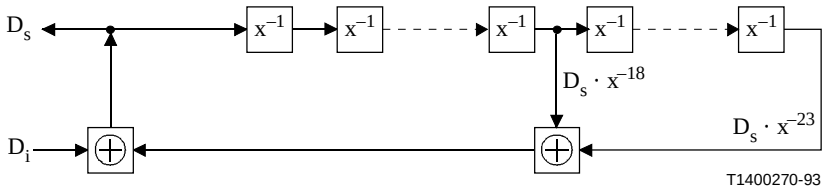


Figure 1/V.300 – Scrambler

5.2 Descrambler

Where the scrambler specified in 5.1 is provided, also a self-synchronizing descrambler having the polynomial $1 + x^{-18} + x^{-23}$ shall be provided in the receiver of the DCE. The message data sequence output by the receiver of the transmission unit (see Figure I.1) shall be effectively multiplied by the generating polynomial $1 + x^{-18} + x^{-23}$ to form the descrambled message. The coefficients of the recovered message sequence taken in descending order form the output data sequence D_o, which is given by:

$$D_o = D_s\ (1 \oplus x^{-18} \oplus x^{-23})$$

where the notation is defined in 5.1.

Figure 2 shows a suitable implementation.

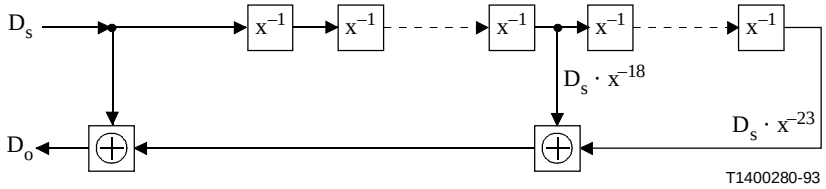


Figure 2/V.300 – Descrambler

6 Interfaces

One or both types of functional interfaces shall be provided in the DCE, as specified below. It shall be possible that two DCEs in accordance with this Recommendation can interoperate, where in these DCEs the opposite types of interfaces are employed.

6.1 V.24-type interface [3]

6.1.1 List of interchange circuits

The interchange circuits shall be as in Table 1.

Table 1/V.300 – V.24-type interface [3]

	Interchange circuit
102	Signal ground or common return
102a	DTE common return (Note 1)
102b	DCE common return (Note 1)
103	Transmitted data
104	Received data
105	Request to send (Note 2)
106	Ready for sending
107	Data set ready
108/2	Data terminal ready (Note 3)
109	Data channel received line signal detector
113	Transmitter signal element timing (DTE source) (Note 4)
114	Transmitter signal element timing (DCE source)
115	Receiver signal element timing (DCE source)
140	Loopback/maintenance test
141	Local loopback
142	Test indicator

NOTE 1 – Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 [1] are used.

NOTE 2 – It shall be possible to apply a permanent ON condition on this circuit inside the DCE.

NOTE 3 – Optional.

NOTE 4 – The use of circuit 113 is for further study, since its application is restricted by the synchronous nature of the network.

6.1.2 Electrical characteristics

Use of electrical characteristics conforming to Recommendation V.10 [1] and/or V.11 [2] is recommended as specified below, together with the use of the connector and pin assignment plan specified by ISO 4902 [13] or ISO/IEC 11569 [15].

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11 [2].

NOTE – In certain instances where V.11 [2] circuits are implemented on both sides of the interface, it may be necessary to add either serial impedance matching resistors or parallel cable terminating resistors as specified in Recommendation V.11 [2] to ensure proper operation of the interchange circuits.

ii) In the case of circuits 105, 106, 107, 108/2 and 109, generators shall comply with Recommendation V.10 [1] or alternatively Recommendation V.11 [2]. The receivers shall comply with Recommendation V.10 [1] category 1, or with Recommendation V.11 [2] without termination.

iii) In the case of all other circuits, Recommendation V.10 [1] applies with receivers configured as specified by Recommendation V.10 [1] for category 2.

6.1.3 Operational requirements

The normal operation for this DCE is constant carrier, i.e. the condition of circuit 105 has no influence upon the line signal and upon remote circuit 109.

Circuit 106 will follow OFF to ON or ON to OFF transitions on circuit 105 within 0.5 to 3.5 ms (this value is for further study). This time is from the application of an ON or OFF condition on circuit 105.

Optionally, the DCE may provide an end-to-end signalling of local circuit 105 to remote circuit 109. The method to be used is for further study.

Where a multiplexing function as described in clause 9 is employed, both circuits 106 and 109 shall be held in the OFF condition in the event of loss of frame synchronization.

Where the optional scrambler/descrambler function specified in clause 5 is provided, circuit 109 shall be switched to the OFF condition upon the reception of 1024 consecutive bits in the binary ONE condition.

The criteria for the control of circuit 109 depending upon a received line signal or other out-of-service codes are a national matter, and are outside the scope of this Recommendation.

6.2 X.24-type interface [7]

6.2.1 List of interchange circuits

The interchange circuits for this interface shall be as in Table 2.

Table 2/V.300 – X.24-type interface [7]

	Interchange circuit
G	Signal ground or common return (Note 1)
Ga	DTE common return
T	Transmit
R	Receive
C	Control
I	Indication
S	Signal element timing (Note 2)
X	DTE signal element timing (Note 3)
B	Byte timing (Notes 4, 5 and 6)

NOTE 1 – This conductor may be used to reduce environmental signal interference at the interface. In the case of shielded interconnecting cable, the additional connection considerations are part of Recommendation X.24 [7] and of ISO 4903 [14].

NOTE 2 – Timing for continuous isochronous data transmission shall be provided.

NOTE 3 – The use and termination of this circuit by the DCE is a national matter, the use being restricted by the synchronous nature of the network.

NOTE 4 – The inclusion of this interchange circuit is optional.

NOTE 5 – It should be noted that this interchange circuit is allocated to the same pole on the connector specified in ISO 4903 [14] as circuit X.

NOTE 6 – The means of providing the byte timing information are a national matter and outside the scope of this Recommendation.

6.2.2 Electrical characteristics

Use of electrical characteristics conforming to Recommendation V.10 [1] and/or V.11 [2] is recommended as specified below, together with the use of the connector and pin assignment plan specified by ISO 4903 [14].

i) Concerning circuits R, S, T and X, both the generators and the receivers shall be in accordance with Recommendation V.11 [2].

NOTE – In certain instances where V.11 [2] circuits are implemented on both sides of the interface, it may be necessary to add either serial impedance matching resistors or parallel cable terminating resistors as specified in Recommendation V.11 [2] to ensure proper operation of the interchange circuits.

ii) Concerning circuits C and I, generators shall comply with Recommendation V.10 [1] or alternatively with Recommendation V.11 [2]. The receivers shall comply with Recommendation V.10 [1] category 1, or with Recommendation V.11 [2] without termination.

6.2.3 Operational requirements

No end-to-end signalling of circuit C to remote circuit I is provided with this type of DCE. Instead, local circuit I shall be in the OFF condition when local circuit C is in the OFF condition.

Optionally, the DCE may provide an end-to-end signalling of local circuit C to remote circuit I. The method to be used is for further study.

A *DCE not ready* signal (r = 0, i = OFF) shall be output at the interface:

– in the event of a loss of frame synchronization where, depending on the data signalling rate and the line signalling rate, a multiplexing function as specified in clause 9 is employed;

– upon the reception of 1024 consecutive bits in the binary ONE condition where the optional scrambler/descrambler function specified in clause 5 is provided.

The DTE should be prepared to receive garbled signals or contiguous binary 1 on circuit R with i = ON, prior to this *DCE not ready* signal.

The criteria for the control of the interface depending on a received line signal are a national matter, and are outside the scope of this Recommendation.

7 Start-up procedure

No specific start-up procedure is needed for the transmission at 64 kbit/s. For the transmission at 128 and 144 kbit/s, the start-up procedure specified hereafter caters for the equalization of a propagation delay difference between the two (or three) 64 kbit/s channels of up to 300 ms.

In the case of transmission at 128 kbit/s, the delay equalization process is initiated by sending a continuous binary 0 signal in both channels for 700 ms, followed by an $0F_{16}$ character in channel B1 and an FF_{16} character in channel B2.

After this starting sequence, a scrambler having the polynomial $D_s = D_i \oplus D_s \cdot x^{-2} \oplus D_s \cdot x^{-5}$ is inserted in the data path and 16 bits of a scrambled binary 1 are transmitted, followed by user data. A guard circuitry to the scrambler shall insert one binary 1 after each sequence of 15 binary 0 bits.

The reception of an unscrambled continuous binary 0 sequence for a duration of at least 650 ms shall indicate that a delay equalization process has been initiated. The receiver shall be configured to monitor the two channels for the reception of an $0F_{16}$ character and an FF_{16} character, respectively, thus identifying the B1 and the B2 channel and measuring the propagation delay between the two channels. An appropriate delay shall be inserted in the channel with the lesser propagation delay.

Then the output of the descrambler shall be monitored for the reception of eleven binary 1 bits (five bits are necessary to synchronize the descrambler), indicating the correct delay equalization.

The start-up procedure for 144 kbit/s connections is for further study.

8 Testing facilities

While it is recognized that the primary means of fault detection/isolation on digital facilities will be accomplished by the network providers through in-service monitoring, the following testing facilities are specified for the case where user-initiated fault isolation is desired. The use of the procedure specified in Recommendation V.54 [5] is provided; other methods for providing fault isolation are for further study.

8.1 Test loops

As in Recommendation V.54 [5], the DCEs are referred to hereafter as DCE A and DCE B.

Test loops 2 for the V.24-type interface [3] case, and 2b for the X.24-type interface [7] case, shall be provided. Test loop 3 shall be provided for the V.24-type interface [3], and one of the test loops 3a or 3b for the X.24-type interface [7]. The precise location of these type-3 loops is beyond the scope of this Recommendation.

The definitions of these test loops are as described in Recommendations V.54 [5] and X.150 [8], respectively. Operation and signalling at the DTE-DCE interfaces of DCE A and DCE B shall be as specified in Recommendations V.54 [5] and X.21 [6], respectively.

8.1.1 Instigation of remote loop 2/2b

The control of loop 2 (loop 2b respectively) shall utilize the preparation and termination phases as specified in Recommendation V.54 [5].

NOTE – Clauses 5, 6 and 7 of Recommendation V.54 [5] describe the automatic control with synchronous DCEs for simple multipoint circuits, point-to-point duplex circuits and tandem circuits. Only the point-to-point duplex circuit case is applicable where in the DCE the X.24-type interface [7] is employed. Application of the two other configurations with the X.24-type interface [7] is for further study.

The instruction of a DCE (DCE A) to instigate a remote loop 2/2b may be manual or automatic. The automatic case shall be upon the recognition of an OFF-to-ON transition on circuit 140 (in the case of the V.24-type interface [3]) or upon the recognition of a *Send loop 2* command (state L21, c = OFF, t = 0011) (in the case of the X.24-type interface [7]) as defined in Recommendation X.21 [6].

This means, irrespective of the type of interface employed, scrambling of a binary 0 with the polynomial $1 + x^{-4} + x^{-7}$ and transmitting it as though it was introduced to the DCE via circuit 103 or circuit T, respectively.

8.1.2 Instigation of the type-3 loop

The instruction of a DCE to instigate a type-3 loop may be manual or automatic. The automatic case shall be upon the recognition of an OFF-to-ON transition on circuit 141 (in the case of the V.24-type interface [3]) or upon the recognition of a *Send loop 3* command (state L31, c = OFF, t = 00001111) (in the case of the X.24-type interface [7]) as defined in Recommendation X.21 [6].

8.2 Self tests

The provision of the self-test function specified herein is optional.

The tests described hereafter (in 8.2.1 and 8.2.2) employ an internally generated data pattern that is typically controlled by a switch on the DCE. It shall be possible to perform these tests with or without the DCE being connected to a DTE.

Upon activation of the self-test function, an internally generated data pattern at the selected user signalling rate shall be transmitted as though it was introduced to the DCE via circuit 103 or circuit T, respectively (see Figure I.1). An error detector, capable of identifying errors in the test pattern, shall be connected to the received data path. How the presence of errors is indicated is beyond the scope of this Recommendation.

NOTE – The test pattern has no end-to-end bearing. Its specification is therefore not part of this Recommendation. Examples for test patterns may be alternative binary ONEs and ZEROs (reversals) or the 511-bit test pattern in accordance with Recommendation O.153 [12].

During any self-test mode, interchange circuits 103, 105 and 108/2 (where provided) at the V.24-type interface, and interchange circuits T and C at the X.24-type interface [7], shall be ignored.

At the V.24-type interface [3], all generating interchange circuits except 114 (if used), 115 and 142 shall be clamped to the binary 1 or OFF condition. If circuit 113 is used, the DCE shall disregard this interchange circuit and shall use its internal clock.

At the X.24-type interface [7], the DCE shall signal state *DCE not ready* (r = 0, i = OFF) to the DTE. If circuit X is used, the DCE shall disregard this interchange circuit and shall use its internal clock.

8.2.1 Self test with the type-3 loop

The type-3 loop as defined in Recommendations V.54 [5] and X.150 [8], respectively, shall be activated in the DCE. The self-test function shall be activated, and the DCE operation shall be as described in 8.2.

8.2.2 Self test with remote loop 2/2b

The DCE shall be conditioned to instigate a loop 2/2b at the remote DCE as specified in 8.1.1. The self-test function shall be activated, and the DCE operation shall be as described in 8.2.

9 Multiplexing

A multiplexing function may optionally be included to convey two individual 64 kbit/s signals on a 128 kbit/s bearer circuit. The method for the identification of the two individual data channels is for further study.

10 Internal management

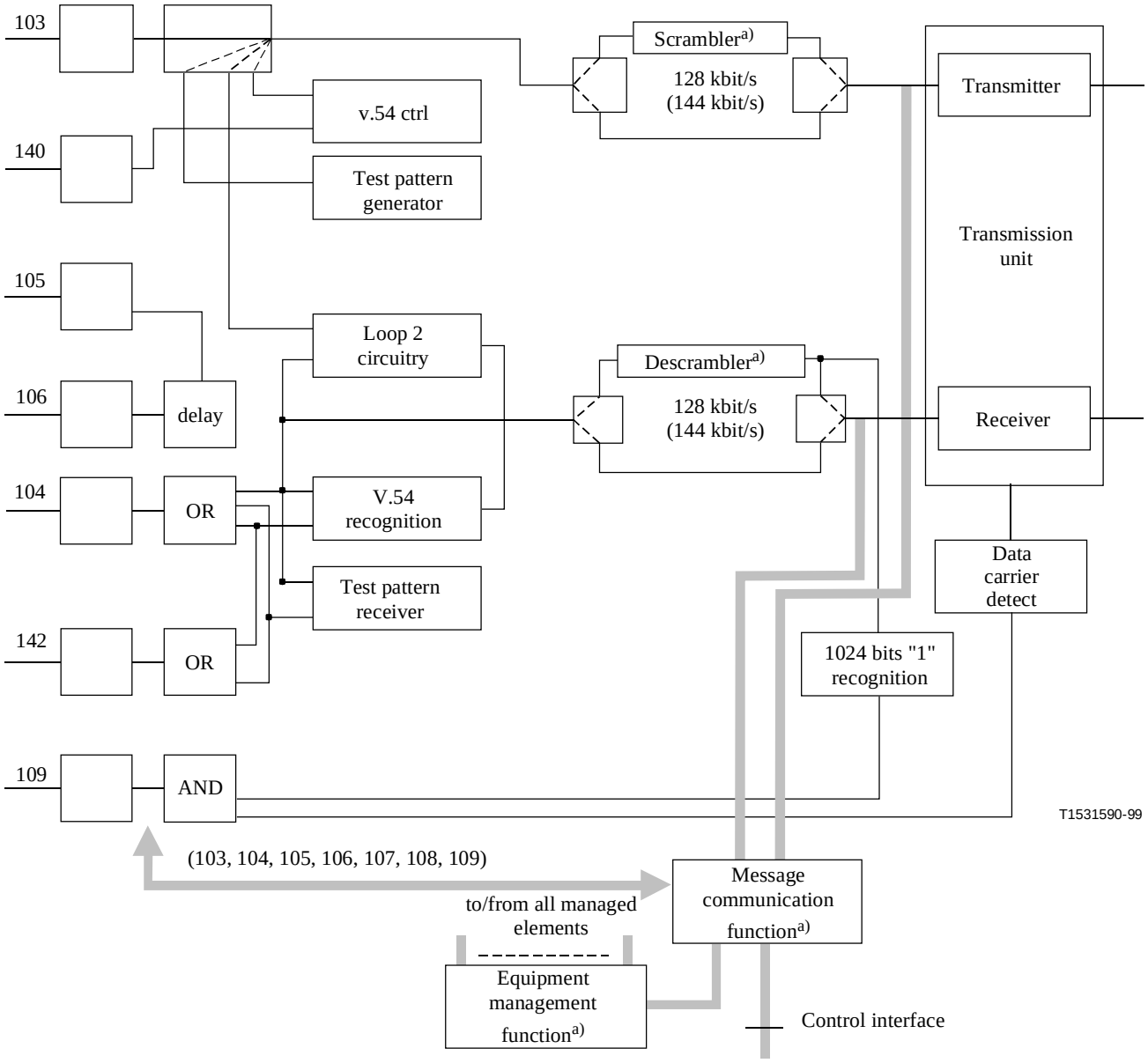
Optionally, internal management functions may be provided. This may include initialization of the DCE, adjustment of part of or all configurable parameters within the DCE. Access to these functions may be accomplished via various means (e.g. front panel menu, DTE-DCE interface, dedicated control interface in local operation mode or via a dedicated PSTN/ISDN connection). The corresponding requirements are beyond the scope of the Recommendation.

APPENDIX I

Functional block diagram

Figure I.1 gives an example of a simplified functional block diagram of a DCE in accordance with this Recommendation, that contains all functional blocks specified in the main part of this Recommendation when a V.24-type DTE-DCE interface is implemented.

The transmission unit contains all functions of a (typically baseband) transmitter and a receiver, which are necessary to interface the DCE to the cable plant of the individual national network. Details are a national matter. For this example it is assumed that the transmission unit is inside the DCE, and interworks with a transmission unit which is installed at the other end of the local loop (see also Appendix II).



a) Optional

Figure I.1/V.300 – An example of a simplified functional block diagram

APPENDIX II

Connection schematics

Figure II.1 provides an example of a 128 kbit/s digital leased circuit between two countries, where the intervening networks support the provision of 128 kbit/s circuits.

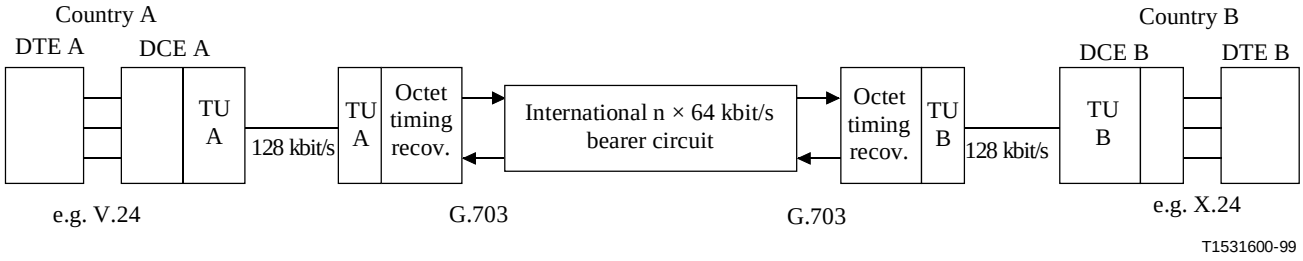
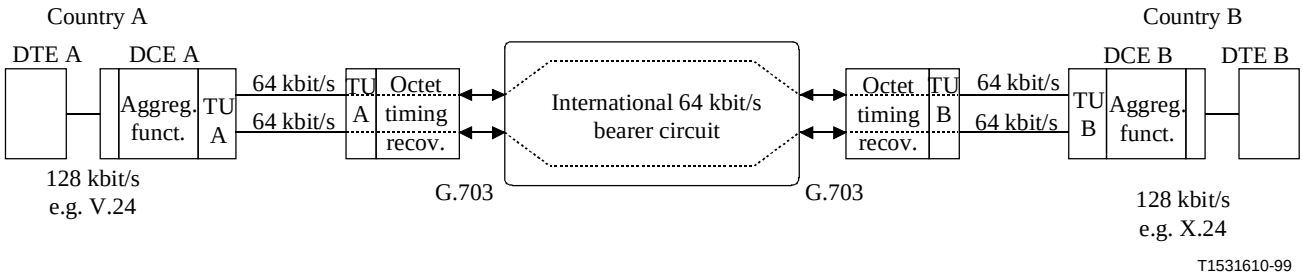


Figure II.1/V.300 – International end-to-end 128 kbit/s digital leased circuit

Figure II.2 provides an example of a 128 kbit/s digital leased circuit between two countries, where the intervening networks support only the provision of 64 kbit/s circuits.



Aggreg. funct. Aggregation function

Figure II.2/V.300 – A 128 kbit/s digital leased circuit on 64 kbit/s bearer circuit

Figure II.3 provides an example of a short haul 144 kbit/s digital leased circuit on metallic pair(s).

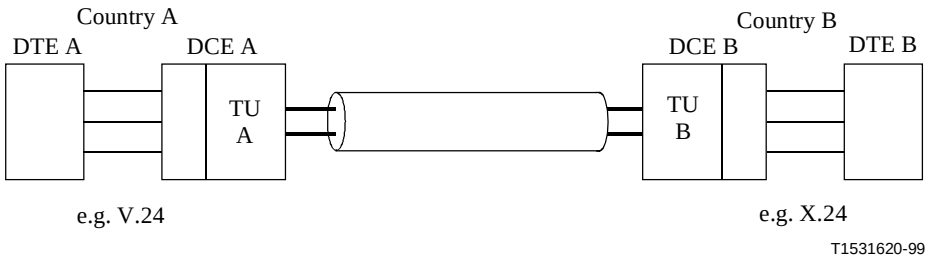


Figure II.3/V.300 – A short haul 144 kbit/s digital leased circuit

APPENDIX III

Example of implementation of the transmission unit

III.1 General

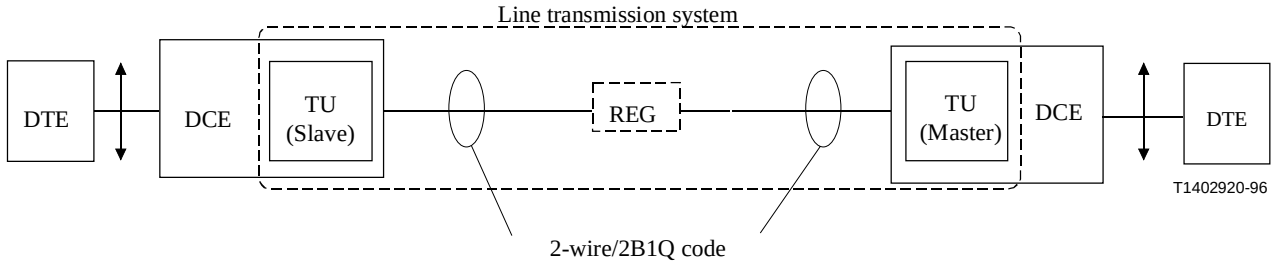
This appendix describes functional characteristics of an implementation of a transmission unit as shown in Figure III.1.

The objectives of this transmission unit are to operate on 2-wire metallic lines that meet minimum ISDN requirements and to use existing components designed for ISDN basic access line transmission system.

The information contained herein is informative and alternative systems may be implemented. The description of these systems requires further study.

III.2 Physical model of the line transmission system

The physical model of the line transmission system is shown in Figure III.1.

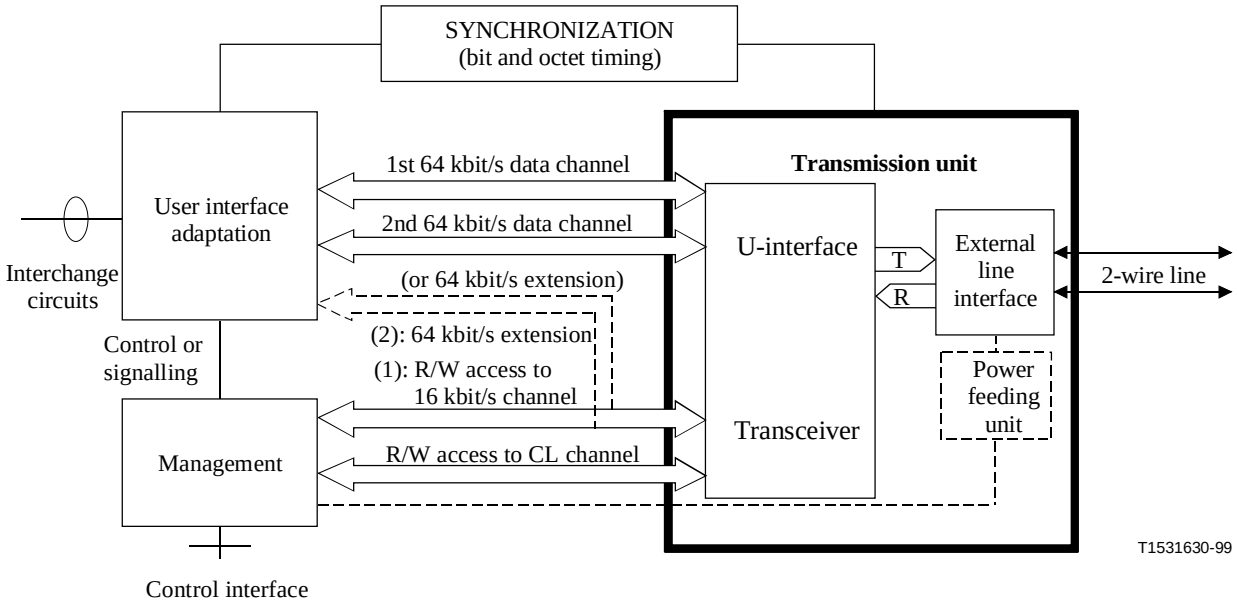


TU Transmission unit
REG Regenerator (optional)

Figure III.1/V.300 – Physical model of the line transmission system

III.3 Functional description of the DCE

DCE characteristics (DTE/DCE interface, end-to-end control or signalling, testing facilities) are specified in the main part to this Recommendation. See Figure III.2.



NOTE – (1) and (2) are exclusive.

Figure III.2/V.300 – Functional block diagram of the DCE

III.4 Functions of TU functional block

The transmission unit incorporated within the DCE (see Figure III.1) interworks with a remote transmission unit at the other end of the local loop that is part of the baseband line termination integrated within the DCE (see Figure III.1).

Operation of both units is not symmetrical. One is configured to operate in the master mode and the other is configured to operate in the slave mode. The decision as to which TU is to be operating in the master mode may be taken at the time of installation of the line transmission system (configurable parameter).

The TU working in slave mode provides the different NT1 functions. TU working in the master mode provides LT functions. NT1 and LT functions are specified in Recommendation G.961. Refer also to Figure III.3

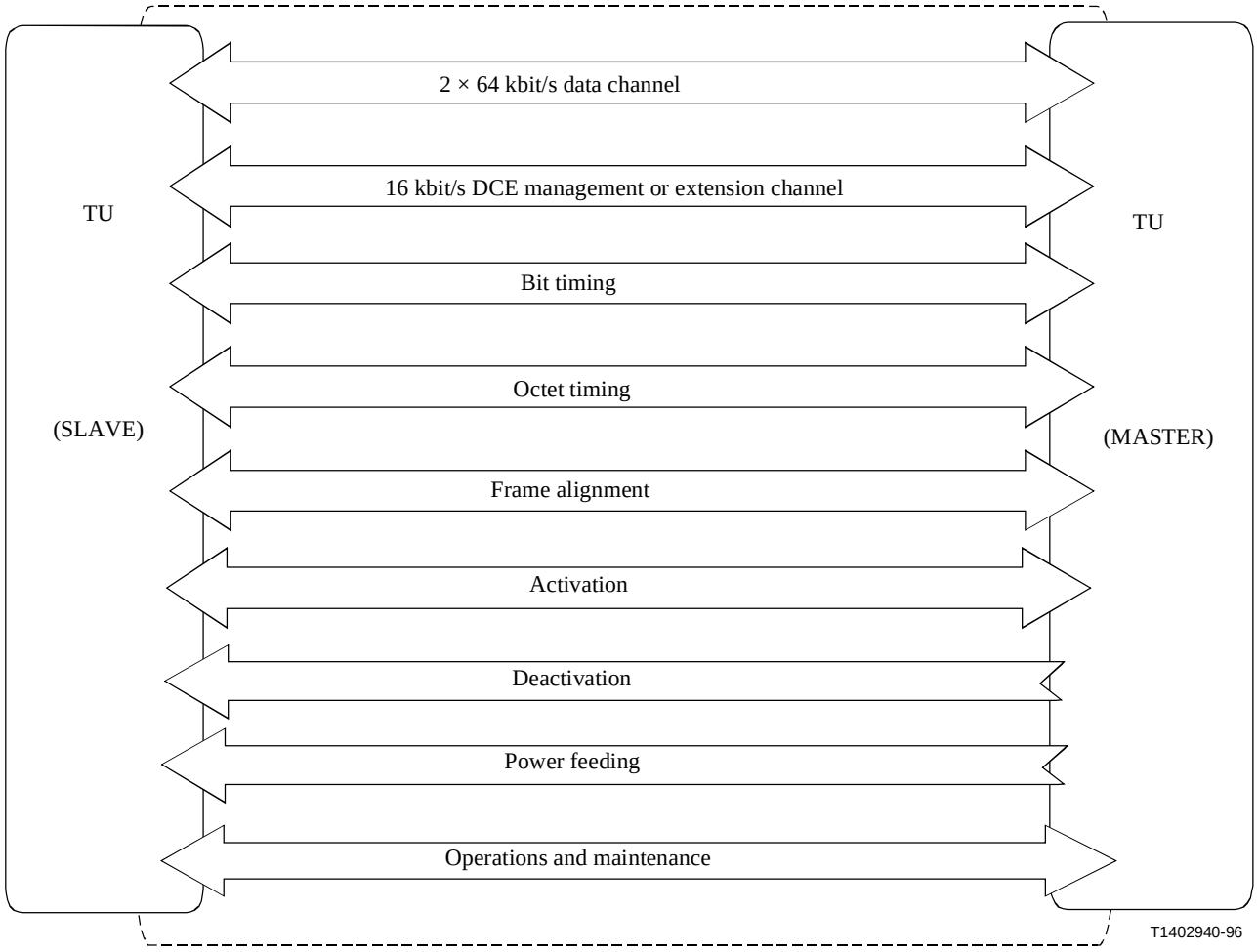


Figure III.3/V.300 – Functions of TU functional blocks

III.4.1 Data channels

This function may provide two bidirectional and independent 64 kbit/s data channels. These correspond to the two B-channels in ISDN basic access signals. For the purpose of this Recommendation, the two 64 kbit/s channels may be used aggregated (optionally individually). Where only one 64 kbit/s channel is used (e.g. interworking with a V.38-type DCE) it should correspond to the first B-channel in the ISDN application.

III.4.2 DCE management channel

This function provides a 16 kbit/s bidirectional channel for the remote management of the DCE. This corresponds to the D-channel in ISDN basic access signals. When this channel is not used for management purposes, it can provide an additional 16 kbit/s transfer capacity for data application allowing an overall bit rate of 144 kbit/s.

While the 16 kbit/s channel may not be allocated to the transmission of management information, the use of the eoc (defined in III.5.7.1) remains an alternative way of performing the remote management of the DCE.

III.4.3 Bit timing

This function provides bit timing to enable the TU to retrieve information from the aggregate stream. Bit timing for direction slave TU to master TU shall be derived from clock received by slave TU from the master TU.

III.4.4 Octet timing

This function provides an 8 kHz octet timing for the 64 kbit/s data channels. It shall be derived from the frame alignment.

III.4.5 Frame alignment

This function enables the TU to recover time-division multiplexed channels.

III.4.6 Activation

This function restores the line transmission system between two TU functional blocks to its normal operational status. At the end of the activation procedure, transparency of the data and the 16 kbit/s management or data channel is achieved; it is not necessary for DTE to be attached during this procedure. It is recommended that only the master TU initiates the activation procedure.

In normal operation, the line transmission system is always activated.

III.4.7 Deactivation

This procedure is only permitted to the master TU. This procedure is initiated by the master TU before initiating testing loops in the slave TU (and regenerator if required).

III.4.8 Power feeding

The power feeding of the TU is handled locally by the DCE. For the case of a power failure, a battery is provided to permit a restricted function and to indicate a fault condition to the distant unit.

The regenerator (if required) shall be locally power fed.

Optionally, the master DCE may provide remote power feeding of the regenerator and of the TU function in the DCE. Remote power feeding of the other DCE functions (user interface adaptation, management system, etc.) is not required.

III.4.9 Maintenance

The functions needed for operations and maintenance of the transmission system – including the TU and one regenerator (if required) – and for activation/deactivation procedures are combined in one transport resource available in the line signals along with the 64 kbit/s data channels and the 16 kbit/s management channel. This transport resource is referred to as the CL channel.

The following functions are provided by the CL channel:

– maintenance command (loopback control in the TU functional block or in the regenerator);
– maintenance information;
– indication of fault conditions;
– information regarding power feeding in the slave TU.

III.5 Requirements for a line transmission system using 2B1Q line code

III.5.1 Line code

The line code is 2B1Q (2 binary, 1 quaternary). This is a 4-level code and it is used without redundancy. This code is described in Appendix II/G.961.

The aggregate bit stream entering the TU functional block before transmission (2 × 64 kbit/s channel, 16 kbit/s management or data extension channel, CL channel) is grouped into pairs of bits for conversion into quaternary symbols called quats. Data input to the 64 kbit/s data channels and the 16 kbit/s management or data extension channel is scrambled before coding.

M1 through M6 bits of the CL channel are also paired, coded and scrambled the same way. The relationships of the bits in the 64 kbit/s data channels and the 16 kbit/s management or data extension channel to quats are shown in Figure III.4.

For convenience, the 64 kbit/s data channels and the 16 kbit/s management channel (or data extension channel) are presented as B1, B2 and D channels respectively, in Figure III.4.

	Time →								
Data	B1 (64 kbit/s data channel)				B2 (64 kbit/s data channel)				D (16 kbit/s channel)
Pair of bits	b11 b12	b13 b14	b15 b16	b17 b18	b21 b22	b23 b24	b25 b26	b27 b28	d1 d2
Quat	q1	q2	q3	q4	q5	q6	q7	q8	q9
Bits Quats	8 4				8 4				2 1

B1	1st 64 kbit/s data channel
B2	64 kbit/s data extension channel (or 2nd 64 kbit/s data channel)
D	16 kbit/s management or data extension channel
b11	First bit of B1 octet as received by TU
b18	Last bit of B1 octet as received by TU
b21	First bit of B2 as received by TU
b28	Last bit of B2 octet as received by TU
d1d2	Consecutive 16 kbit/s management or data extension channel
qi	ith quat relative to start of a given 18-bit 2B+D data field

Figure III.4/V.300 – 2B1Q bit encoding for 64 kbit/s data and 16 kbit/s management (or extension) channels

III.5.2 Line modulation rate

The gross bit rate is 160 kbit/s; 144 kbit/s are occupied by the data channels and the 16 kbit/s management channel (or data extension channel) and the CL channel presents a bit rate of 4 kbit/s. The remaining 12 kbit/s are used for the frame alignment word. The line symbol rate (modulation rate) is 80 kbauds.

III.5.3 Clock tolerance

Clock tolerance of the free running TU clock is ±50 ppm.

III.5.4 Frame structure

A frame shall consist of 120 quaternary symbols transmitted within a nominally 1.5 ms interval. Each frame contains a frame word, the data and/or management channel bits and the CL channel bits.

III.5.5 Frame and multiframe words

The frame word (FW) is used to allocate bit positions to the data, management channel and the CL channels.

The code for the frame word in all frames except the first in a multiframe is:

FW = + 3 + 3 –3 –3 –3 + 3 –3 + 3 + 3

The code for the first word of the first frame of a multiframe is the inverted frame word (IFW):

IFW = –3 –3 + 3 + 3 + 3 –3 + 3 –3 –3

The frame and multiframe words are the same for both directions.

III.5.6 Frame offset between slave TU and master TU

The slave TU synchronizes transmitted frames with received frames from the master TU. Transmitted frames are offset with respect to received frames by 60 ± 2 quaternary symbols (i.e. about 0.75 ms).

III.5.7 CL channel

III.5.7.1 Structure of the CL channel

The CL channel consists of the last three symbols (6 bits) in each basic frame of the multiframe; 48 bits of a multiframe are used for the CL channel.

The bit rate for the CL channel is 4 kbit/s:

– 24 bits per multiframe (2 kbit/s) are allocated to an embedded operation channel (eoc) which supports operations communications needs between the TU;

– 12 bits per multiframe (1 kbit/s) are allocated to a cyclic redundancy check (CRC) function;

– 12 bits per multiframe (1 kbit/s) are allocated to other functions as shown in Figure III.5.

		Framing	12 × (2B+D)	CL channel (bits M1 to M6)					
	Quat positions	1-9	10-117	118s	118m	119s	119s	120s	120m
	Bit positions	1-18	19-234	235	236	237	238	239	240
Multiframe	Frame	Frame word		M1	M2	M3	M4	M5	M6
		TU Master → TU Slave							
A	1	IFW	12 × (2B+D)	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	FW	12 × (2B+D)	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea	1	febe
	3	FW	12 × (2B+D)	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	FW	12 × (2B+D)	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	FW	12 × (2B+D)	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	FW	12 × (2B+D)	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	FW	12 × (2B+D)	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	FW	12 × (2B+D)	eoc_{i6}	eoc_{i7}	eoc_{i8}	aib	crc_{11}	crc_{12}
B, C...									
		TU Slave TU → Master							
1	1	IFW	12 × (2B+D)	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	FW	12 × (2B+D)	eoc_{dm}	eoc_{i1}	eoc_{i2}	ps_1	1	febe
	3	FW	12 × (2B+D)	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	FW	12 × (2B+D)	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	FW	12 × (2B+D)	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	FW	12 × (2B+D)	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	FW	12 × (2B+D)	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	FW	12 × (2B+D)	eoc_{i6}	eoc_{i7}	eoc_{i8}	1*	crc_{11}	crc_{12}
2, 3....									

2B+D	Data bits (data and management channels)
Quat	Any pair of bit forming a quaternary symbol
s	Sign bit (first) in a quat
m	Magnitude bit (second) in a quat
FW/IFW	Frame word/inverted frame word, bits 1-18 in a frame
1	Reserved for future definition
1*	Reserved for network use (network indicator)
CL	CL channel bits M1 to M6 (bits 235-240 in basic frame structure)
eoc	Embedded operation channel
eoc_{ai}	Address bits
eoc_{dm}	Data/message indicator
eoc_i	Information (data or message)
crc_n	Cyclic Redundancy Check procedure (applicable to 2B+D and M4) n Most significant bit n+1 Following most significant bit, etc.
febe	Far-end block error (ZERO for errored multiframe)
ps_1 and ps_2	Power status bits (ZERO indicate power problem)
ntm	Test mode bit (ZERO indicate the slave TU test mode)
cso	Cold start only bit (optional, set to ZERO if not used)
sai	S/T interface activity indicator (optional, set to ONE if not used)
act	Activation bit (set to ONE during activation to indicate readiness for layer 2 communication progress)
dea	Deactivation bit (ZERO indicates the Master TU's intention to deactivate)
uoa	U only activation (optional, set to ONE to activate user interface)
aib	Alarm indication bit (ZERO indicates interruption)

Figure III.5/V.300 – 2B1Q multiframe technique and bit assignment

III.5.7.2 Functions of the CL channel

Functions of the CL channel listed below are based on bit allocation for the multiframe defined in Figure III.5:

– Error monitoring function (crc bits).

– Far-end block error (febe bit).

– Activation (act).

– Deactivation (dea).

– Power status of slave TU (ps_1, ps_2).

– Slave TU test mode indicator (ntm); its use is optional. It may be used by the slave TU to indicate that a maintenance action has been locally initiated by the corresponding DTE.

– Alarm indicator bit (aib); its use is optional. It can be used by the master TU to indicate a failure of intermediate transmission system.

– Embedded operation channel functions (eoc). Functions provided are essentially 144 kbit/s signal (2B+D) loopbacks, 64 kbit/s signals (B1 and B2) loopbacks in the slave TU (type-2 loopback) or in regenerator (loopback 1A) if required. Only the master TU is permitted to control loopbacks this way.

64 eoc message codes have been reserved for standard applications or for internal network use. Other codes may be used for non-standard applications such as supporting DCE management functions. At least 120 codes are available for this purpose. Any use of such messages shall not interfere with the 16 kbit/s management channel when provided.

III.6 DCE management channel

III.6.1 Protocol and procedure

Detailed protocol and procedure for the management of DCE are for further study.

III.6.2 Functions provided

This channel may support end-to-end control or signalling and maintenance information and acknowledgements related to:

– alarm;

– performance;

– state of interchange circuits (105/109, C/I) when an in-band end-to-end control channel in the 64 kbit/s data channel is not provided;

– remote loop 2 command and acknowledgement;

– configuration of the remote DCE connected to the master DCE.

III.7 Equipment management function

III.7.1 General

This subclause only considers management aspects in relation with the transmission unit.

The equipment management function monitors the different testing facilities of the transmission unit.

It receives and analyses information coming from the control interface, from the user interface, from the local TU functional block, from the remote TU functional block through the CL channel and from the remote end DCE through the management channel, assuming that the intervening network supports this function.

The equipment management function handles the interworking of the DCE functions with the monitoring functions of the line transmission system.

III.7.2 Specific functions of the equipment management function with TU working in slave mode

Equipment management function:

– manages the procedure of activation for the line transmission system initiated by the master TU;

– generates loopback confirmation.

Optionally, where the equipment management function of a slave TU detects a loop command coming from the control interface or from the interchange circuits of the user interface or from the DCE management channel, it communicates this test mode status to the master TU by setting the ntm bit to binary ZERO.

III.7.3 Specific functions of equipment management function with TU working in master mode

Equipment management function:

– initiates and manages the procedure of activation/deactivation for the line transmission system;

– controls the procedures for the setting of loopbacks in the line transmission system.

When the equipment management function of the master TU has detected a loop command coming from the control interface of the master DCE or from the remote end DCE management channel, it communicates this test mode status to the slave TU by setting the aib bit to binary ZERO.

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