INTERNATIONAL TELECOMMUNICATION UNION

ITU-T V.54

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

LOOP TEST DEVICES FOR MODEMS

ITU-T Recommendation V.54

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.54 was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.54

LOOP TEST DEVICES FOR MODEMS

(Geneva, 1976; amended at Geneva, 1980,
Malaga-Torremolinos, 1984 and at Melbourne, 1988)

1 Introduction

The CCITT,

considering

the increasing use being made of data transmission systems, the volume of the information circulating on data transmission networks, the savings to be made by reducing interruption time on such links, the importance of being able to determine responsibilities in maintenance questions for networks, of necessity involving several parties, and the advantages of standardization in this field,

unanimously declares the following:

The locating of faults can be facilitated in many cases by looping procedures in modems. These loops allow local or remote measurements, analogue or digital, to be carried out optionally by the Administrations and/or users concerned.

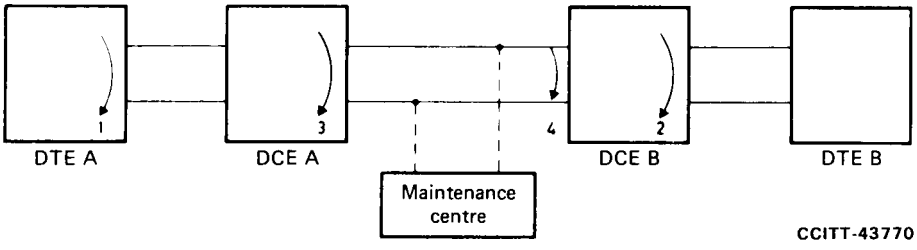
2 Scope

This Recommendation specifies modem loop testing procedures for the following cases:

- for synchronous mode of operation over point-to-point leased circuit, multipoint, tandem and general switched telephone network (GSTN) connections;
- for start-stop mode of operation over point-to-point leased circuit and GSTN connections.

3 Definition of the loops

Four loops are defined (numbered 1 to 4) and their locations as seen from DTE A are shown in Figure 1/V.54. A symmetrical set of four loops could exist as seen from DTE B.



DTE Data terminal equipment
DCE Data circuit-terminating equipment

FIGURE 1/V.54

3.1 *Loop 1*

This loop is used as a basic test on the operation of the DTE, by returning transmitted signals to the DTE for checking. The loop should be set up inside the DTE as close as possible to the interface.

While the DTE is in the loop 1 test condition:

- transmitted data (circuit 103) are connected to received data (circuit 104) within the DTE;
- circuit 108/1 or 108/2 must be in the same condition as it was before the test;
- circuit 105 must be in the OFF condition;
- circuit 125 should continue to be monitored by the DTE so that an incoming call can be given priority over a routine loop test.

Interchange circuit 103 as presented to the DCE must be in the binary 1 condition.

The conditions of the other interchange circuits are not specified but they should if possible permit normal working. The transmitter timing information, in particular if it comes from the DCE, will continue to be sent (see Recommendation V.24, § 4.6.2).

Note - When circuits 108 and 105 are not used by the DTE (for applications on leased lines, for example) the DCE will not be informed of the test condition. This is considered acceptable provided that the remote station is not disturbed.

3.2 *Loop 3*

This is a local loop established in analogue mode as close as possible to the line to check the satisfactory working of the DCE. The loop should include the maximum number of circuits used in normal working (in particular the signal conversion function, if possible) which may in some cases necessitate the inclusion of devices for attenuating signals, for example.

The establishment of the loop presents no difficulty when using a 4-wire line, except in certain cases in which parts of the line equalization system are removed from service.

For certain 2-wire lines the loop may be obtained by simple unbalance of the hybrid transformer.

While the DCE is in the loop 3 test condition:

- the transmission line is suitably terminated, as required by national regulations;
- all interchange circuits are operated normally, except in the case of 2-wire half-duplex operation where the mandatory clamping involving circuits 105 and 109 (as specified in Recommendation V.24, § 4.3.2 a) is disabled;
- circuit 125 should continue to be monitored by the DTE so that an incoming call can be given priority over a routine loop test, after abandoning the loop 3 condition;
- no signal is transmitted to line on the data channel.

Since most interchange circuits operate normally, a diagram of interchange circuit operation sequence is not presented.

Note 1 - In certain switched networks the loop 3 procedure may clear the connection due to national regulations. During the loop 3 condition, however, the DCE must not be switched to the line, if' not already connected.

Note 2 - In 4-wire point-to-point connections circuit 105 may be continuously ON. If in such cases synchronous modems are used, no test data should be transmitted until circuits 106, 109 and 142 are in the ON condition.

3.3 *Loop 2*

Loop 2 is designed to permit station A or the network to check the satisfactory working of the line (or part of the line) and of the DCE B. It can only be used with a duplex DCE; the application to the backward channel is left for

further study. Pseudo loop 2 may be defined for a half-duplex DCE and will be specified in the Recommendation relating to the DCE concerned.

The establishment of the loop will be effective when the control is applied, regardless of the condition of circuit 108 presented by the DTE associated with the DCE in which the loop is set up.

While the DCE B is in the loop 2 test condition:

- circuit 104 is connected internally in the DCE to circuit 103 (see Note 1);
- circuit 104 to the DTE is maintained in the binary 1 condition;
- circuit 109 is connected internally in the DCE to circuit 105 (see Note 1);
- circuit 109 to the DTE is maintained in the OFF condition;
- circuit 106 to the DTE is maintained in the OFF condition;
- circuit 107 to the DTE is maintained in the OFF condition;
- circuit 115 is connected internally in the DCE to circuit 113 if provided (see Note 1);
- circuit 115 and circuit 114, if provided, to the DTE continue to function.

Note 1 - For the internal DCE connections, the electrical signal characteristics may either be that of the interchange circuits or that of the logic level used inside the DCE.

Note 2 - In certain applications, it may not be desirable to connect circuit 115 to circuit 113. In these cases a flexible buffer between circuits 104 and 103 might be recommended. Alternatively, changes in the transmit clock may be done in a phase-continuous manner.

3.4 *Loop 4*

This loop arrangement is only considered in the case of 4-wire lines. Loop 4 is designed for the maintenance of lines by Administrations using analogue-type measurements. When receiving and transmitting pairs are connected in tandem, such a connection cannot be measured as a data circuit (conformity with a line characteristic curve, for example).

In the loop position the two pairs are disconnected from the DCE and are connected to each other through a symmetrical attenuator designed to prevent any oscillation of the circuit (the loop, therefore, does not include any of the amplifiers and/or distortion correctors used in the DCE). The value of the attenuator will be fixed by each Administration in compliance with Recommendation G.122 [1].

Loop 4 may be established inside the DCE or in a separate unit.

When loop 4 is inside the DCE, and while in the test condition, the DCE presents circuits 107 and 109 to the DTE in the OFF condition and circuit 142 is in the ON condition. When loop 4 is in a separate unit, these conditions are desirable but not mandatory.

4 Loop control

Two (non-exclusive) types of control might be possible on the DCE:

- manual control by a switch on the equipment;
- automatic control through the DCE-DTE interface or upon recognition of a loop initiation signal in the received data.

The test procedures shall be based on either manual or automatic control of loops. Combined use of these control methods shall be avoided. However, manual release of a test loop shall have priority over automatic control in those DCEs where both test methods are implemented.

Note - The response of a DCE to automatic or manual control attempts in the case where the other control method is used, is not specified.

Interchange circuit 142 shall be used to inform the DTE of a loop condition in the local DCE, even in the case of manual control (but see Note 3 to Table 1/V.54). To avoid ambiguity in interpretation of circuit 142 only one loop should be established at any one time in the DCE.

4.1 *Manual control*

See Table 1/V.54.

TABLE 1/V.54

Interface signalling for manual control of loops

Loop	Control switch on	Signal to DTE A		Signal to DTE B		Notes
		Circuit 107	Circuit 142	Circuit 107	Circuit 142	
2	DCE B	*)	*)	OFF	ON	Note 1
3	DCE A	ON	ON	*)	*)	Note 2
4	DCE B	*)	*)	OFF	ON	Note 3

*) Not applicable.

Note 1 - Data station A is in the normal operating condition. The loop is established by a switch on DCE B.

Note 2 - In DCE A, the condition of circuit 107 will be determined by the condition of circuit 108. When circuit 108 is not provided on the interface, circuit 107 is ON. The normal case is considered in the table.

Note 3 - When loop 4 is in a unit separate from the DCE, the signals to DTE B are desirable but not mandatory due to the difficulty of implementation. When the loop is implemented within the DCE, loop establishment, shall always be possible by a switch on the DCE.

Note 4 - The conditions represented by ON in the table may also activate a visual indicator on the DCE.

4.2 *Automatic control through the DTE/DCE interface* (see Table 2/V.54)

Automatic control through the interface is achieved by using circuit 140, 141 and 142 as defined in Recommendation V.24. Circuit 140 is used to control loop 2 and circuit 141 is used to control loop 3. The turning ON of circuit 142 indicates the test mode is established. If circuit 107 is ON, the associated terminal is concerned and subsequent data transmitted on circuit 103 will be looped back on circuit 104. If circuit 107 is OFF, the associated terminal is not concerned.

Note 1 - Automatic control of loop 4 is considered of no use either locally or in the remote station and therefore is not provided.

Note 2 - As an alternative to activation of loop 3 via circuit 141, it could be activated via the four-phase procedure defined in § 4.2 here.

TABLE 2/V.54

Interface signalling for automatic control of loops

Loop	Control signals from DTE A		Signals to DTE A		Signals to DTE B		Notes
	Circuit 140	Circuit 141	Circuit 107	Circuit 142	Circuit 107	Circuit 142	
2	ON	OFF	ON	ON	OFF	ON	Notes 1 and 2
3	OFF	ON	ON	ON	*)	*)	Note 2

*) Not applicable.

Note 1 - There is a risk of head-on collision of controls from the two ends.

Note 2 - In DCE A, the condition of circuit 107 will be determined by the condition of circuit 108. When circuit 108 is not provided on the interface, circuit 107 is ON. The normal case is considered in the table.

Normally circuit 103 can only be used to transmit data or the test sequence, so long as the conditions of circuits 106, 140, 141 and 142 are as indicated in Table 3/V.54.

TABLE 3/V.54

Circuit 103	Circuit 106	Circuit 140	Circuit 141	Circuit 142
Data	ON	OFF	OFF	OFF
Loop 2 test sequence	ON	ON	OFF	OFF
Loop 3 test sequence	ON	OFF	ON	ON

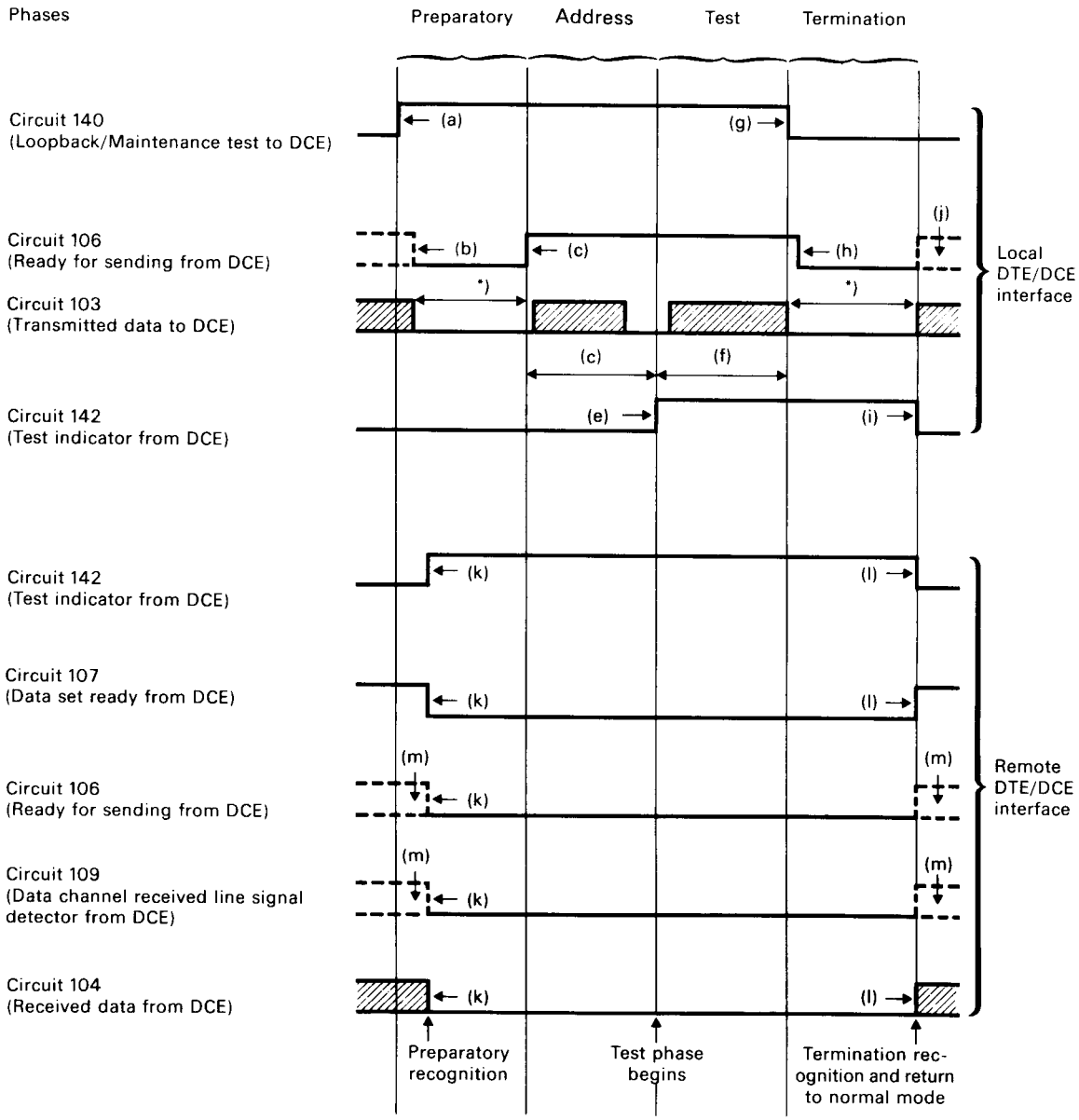
For inter-DCE signalling a four-phase action/reaction sequence should be used. The state of interchange circuits principally involved during this sequence is shown in Figure 2/V.54.

Automatic control with synchronous DCEs is described for:

- simple multipoint circuits (see § 5);
- point-to-point duplex circuits (see § 6);
- tandem circuits (see § 7).

Automatic control with asynchronous DCEs is described for:

- point-to-point duplex circuits (see § 8).



*) The DCE will ignore circuit 103 during preparatory and terminating phases.

Note – This sequence may be used for point-to-point duplex circuits. The address phase is not essential for point-to-point applications.

FIGURE 2/V.54

State of interchange circuits during the four-phase action/reaction sequence

Explanation of Figure 2/V.54

Central site

(a) Circuit 140 goes ON (to DCE), requesting a maintenance sequence.

(b) Circuit 106 goes OFF (from DCE), very shortly thereafter, if not already OFF.

(c) Circuit 106 goes ON (from DCE), after a delay, which signifies that the DCE can accept address information.

(d) Circuit 103 is active (to DCE), transmitting the address.

(e) Circuit 142 goes ON (from DCE), after a delay, signifying that the maintenance address has been acted upon and if a loop establishment has been requested, circuit 103 may now be used for the test message.

(f) Circuit 103 is active (to DCE), containing a test message or any other data as required by the maintenance routine being performed.

(g) Circuit 140 goes OFF (to DCE), requesting termination of the maintenance sequence and a return to normal operation.

(h) Circuit 106 goes OFF (from DCE), very shortly thereafter.

(i) Circuit 142 goes OFF (from DCE), after a delay, signifying that the terminating phase is complete and the system is returned to normal operation.

(j) Circuit 106 may be ON or OFF after the maintenance sequence.

During the maintenance the state of circuit 105 would be disregarded.

Remote site

(k) Circuit 142 goes ON (from DCE), indicating test mode to the remote DTE.

Circuit 107 goes OFF. Circuits 106 and 109 go OFF if not already OFF.

Circuit 104 is clamped to binary 1 condition. Before preparatory recognition spurious bits may appear on circuit 104.

(l) Circuit 142 is turned OFF, circuit 107 is turned ON, the clamping of circuit 104 by circuit 142 ON condition is removed, signifying that termination recognition has taken place at the remote DCE, and that it has returned to the normal mode.

(m) Circuits 106 and 109 may be ON or OFF, prior to and after the maintenance sequence.

5 Inter-DCE signalling for simple multipoint circuits with synchronous DCEs

Note 1 - Modems in accordance with Recommendation V.22 are excluded from this procedure.

Note 2 - Considering the fact that there already exist or will exist modems implementing other signalling techniques than the one defined in this Recommendation and that these signalling techniques have been designed according to special conditions formulated by Administrations or users, this Recommendation does not limit the use of such signalling techniques.

A state diagram of the preparatory, address, test and termination phase is shown in Figure A-2/V.54.

5.1 *Preparatory phase*

During the preparatory phase DCE A will transmit a pattern of 2048 ± 100 bits produced by scrambling a binary 0 with the polynominal $1 + x^{-4} + x^{-7}$. No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler. Before transmitting the preparatory pattern, DCE A has to establish a data channel, if not already available.

The criteria for the recognition of this pattern by DCE B are not part of this Recommendation. The criteria that are implemented should offer a very high protection against false recognition due to simulation by user data and some protection against failure to recognize the preparatory pattern due to a high bit error rate. In order to provide protection against false recognition caused by user HDLC frames, the bit sequence consisting of seven consecutive binary 1s, which is at present in the preparatory pattern, must be included in the recognition criteria.

DCE B will start Timer T1 (if implemented) upon recognition of the preparatory phase.

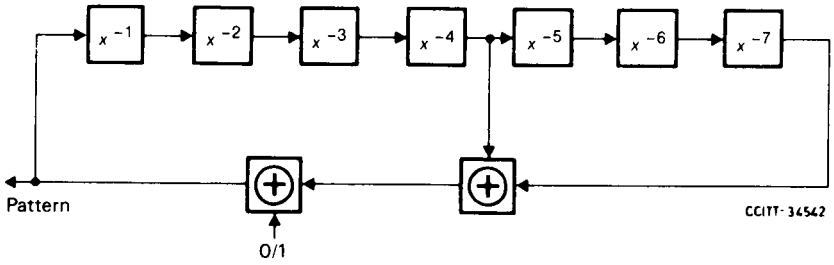


FIGURE 3/V.54

Example of scrambler implementation

5.2 *Address phase*

5.2.1 *Address signalling*

During the address phase the DTE will transmit an address sequence consisting of an address octet that is repeated at least 16 times. The sequence may be preceded and succeeded by other octets as required by the user link level protocol. Synchronous DCEs will transmit these octets in contiguous eight bit groups.

Table 4/V.54 contains a set of possible address octets and the constraints on their use.

When an extension of the address set is required, a similar set consisting of two-octet addresses can be generated.

Note - The set contained in Table 4/V.54 may be regarded as a subset of the extended set, i.e. one consisting of those two-octet addresses whose two octets are identical.

The DCE will recognize its address when it is detected in at least five contiguous octets received. No octet synchronization is required.

When the DCE detects an address sequence (five identical contiguous octets), not containing its address, it will disable the address detection function, thus avoiding false recognition of its own address due to simulation by subsequent test messages.

5.2.2 *Acknowledgment signalling*

DCE B, upon recognition of the address signal containing its address, will transmit a pattern of 1948 ± 100 bits produced by scrambling a binary 1 with the polynomial $1 + x^{-4} + x^{-7}$. No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler.

Before transmitting the acknowledgment pattern, DCE B has to ensure that the data channel to DCE A is available. Since the loop 2 test is in a synchronous DCE, DCE B will use its receiver signal element timing for this data channel.

TABLE 4/V.54

Single-octet address set

Hexadecimal code	Note	Hexadecimal code	Note	Hexadecimal code	Note
01	1	19	1	37	1
03	2	1B	2	3B	1
05	2	1D	2	3D	1
07	1	1F	1, 4	3F	2, 4
09	2	25	1	55	2
0B	3	27	2	57	1
0D	1	2B	2	5B	1
0F	2	2D	2	5F	2, 4
11	2	2F	1	6F	2
13	1	33	2	77	2
15	1	35	2	7F	1, 4
17	2	35	2	7F	1, 4

Note 1 - Odd parity.

Note 2 - Even parity.

Note 3 - Sync (1/6) with odd parity.

Note 4 - Not to be used in ISO 3309 (HDLC) frame structures.

The criteria for the recognition of this pattern by DCE A are not part of this Recommendation. The criteria that are implemented should offer good protection against failure to recognize the acknowledgment signal due to a high bit error rate.

DCE B, after transmission of the acknowledgment pattern, will enter the test phase.

DCE A, upon recognition of the acknowledgment pattern, will time out for a 2148 + 100 bit period and will then turn ON circuit 142, thus entering the test phase.

DCE A, upon recognition of the acknowledgment pattern, will not take any action if it is in the normal data mode.

5.3 *Test phase*

Signals transmitted during the test phase are not specified in this Recommendation.

5.4 *Termination phase*

During the termination phase, DCE A will transmit a pattern of 8192 ± 100 bits produced by scrambling a binary 1 with the polynomial $1 + x^{-4} + x^{-7}$, followed by 64 binary 1s.

No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler.

DCE B will terminate the test mode in any of the following situations:

- recognition of the termination pattern;
- carrier loss with a duration longer than 1s;
- expiration of the optional Timer T1.

The criteria for the recognition of this pattern by DCE B are not part of this Recommendation. The criteria that are implemented should offer good protection against false recognition due to simulation by test data and good protection against failure to recognize the termination pattern due to a high bit error rate.

DCE B will normally leave the termination phase during the reception of the binary 1 pattern that concludes the termination pattern.

DCE B upon recognition of the termination pattern will not take any action if it is in the normal data mode.

Note - The length of the time interval of the optional Timer T1 is not specified in this Recommendation.

6 Simplified inter-DCE signalling for use in point-to-point circuits with synchronous DCEs

For point-to-point circuits which require control of one loop 2 only, the four-phase sequence may be simplified by deleting the address signalling. The procedure is then as follows (see Figure A-3/V.54):

- Preparatory phase: in accordance with § 5.1.
- Address phase: acknowledgment signalling only in accordance with § 5.2.2 upon recognition of the preparatory pattern.
- Test phase: signals transmitted during the test phase are not specified in this Recommendation.
- Termination phase: in accordance with § 5.4.

7 Inter-DCE signalling for tandem circuits with synchronous DCEs

For tandem circuits the four-phase sequence may be used to control the loops shown in Figure 4/V.54.

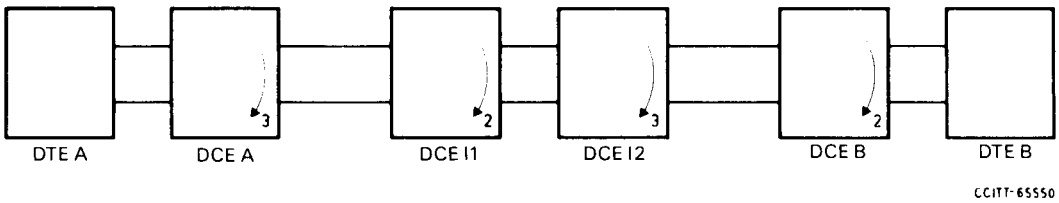
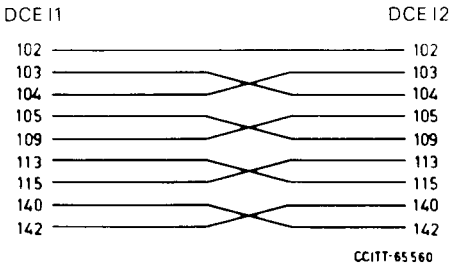


FIGURE 4/V.54

The inter-DCE signalling procedures apply to synchronous modems only, with or without multiplexer features. The interchange circuits of the DCEs at the intermediate site are connected as shown in Figure 5/V.54.



Note 1 - The ON condition on circuit 142 shall not clamp the interchange circuits 107, 109 and 104 in DCE I1.

Note 2 - Signalling the ON condition from circuit 142 to 140 shall not start transmission of the preparatory pattern from DCE I2, but activate the address monitor.

Note 3 - Only those interchange circuits essential for establishing the loops are shown.

FIGURE 5/V.54

A state diagram of the four-phase sequence is shown in Figure A-4/V.54. The procedure is as follows:

- Preparatory phase: in accordance with § 5.1.

  When DCE I1 recognizes the preparatory pattern it will signal this condition via the ON condition on circuit 142 to circuit 140 of DCE I2, which will activate its address monitor.

  The preparatory pattern is transmitted via circuit 103 of DCE I2 to DCE B.
- Address phase: in accordance with § 5.2.
- Test phase: signals transmitted during the test phase are not specified in this Recommendation.
- Termination phase: in accordance with § 5.4.

When a loop has been established in the intermediate site, the part of the link "behind" the loop is in fact inactivated.

When the loop that has been established is a loop 3 in DCE I2, the carrier towards DCE B will be removed from the line. When this condition lasts for more than one second, DCE B will regard the test condition as terminated and return to normal mode (i.e. with data carrier lost). As this situation was preceded by a 142 ON condition, the remote DTE may regard this as a normal situation. When the loop 3 condition in DCE I2 is terminated, which will normally be after the reception of the full termination pattern, the remote DTE will not receive garbled signals after DCE B has recovered the carrier.

When the loop that has been established is a loop 2 in DCE I1 all patterns will pass to DCE B. Thus DCE B will also receive the termination pattern and leave the test mode at the prescribed time. DCE I2 will leave the test mode upon detecting the OFF condition on circuit 140.

Note - When the connection of DCE I1 and DCE I2 is established via a multiplexer without remote signalling capabilities for interchange circuits 109 and 142, DCE 12 may optionally derive the required information from the patterns present on interchange circuit 103.

8 Inter-DCE signalling for point-to-point connections with asynchronous DCEs

For point-to-point duplex circuits with asynchronous DCEs for start-stop operation only, the four-phase sequence may be simplified by deleting the address signalling. Instead of the pseudo-random patterns used for synchronous transmission a simple signalling method shown in Figure 6/V.54 shall be used.

8.1 *Preparatory phase*

During the preparatory phase DCE A will transmit a SPACE-MARK-SPACE pattern. The duration of each interval shall be 320-400 ms.

8.2 *Address phase*

DCE B, upon recognition of the preparatory pattern, will establish loop 2 and transmit the acknowledgment signal consisting of a carrier OFF period of 100-150 ms.

DCE A will turn ON circuit 142 and enter the test phase after it has detected the OFF to ON transition of the carrier signal.

8.3 *Test phase*

Signals transmitted during the test phase are not specified in this Recommendation.

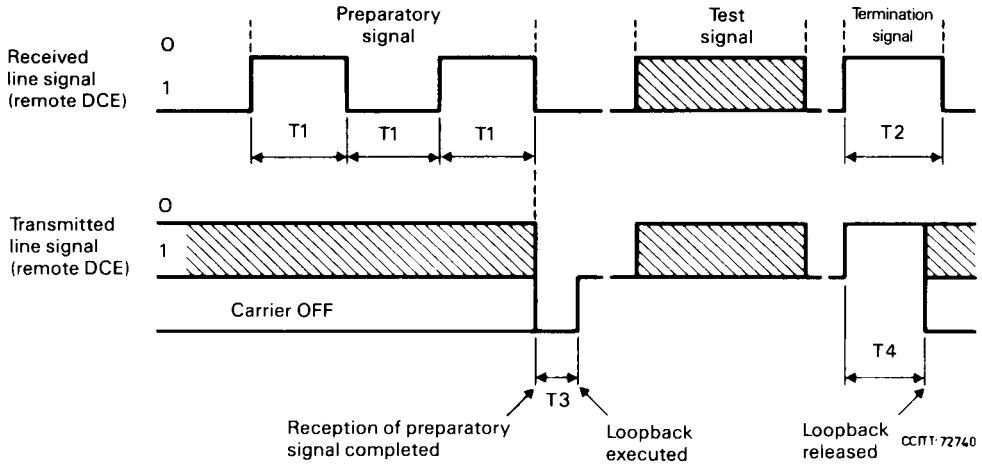
8.4 *Termination phase*

During the termination phase DCE A will transmit a signal consisting of binary 0 (SPACE) for at least 550 ms.

DCE B will terminate the test mode in any of the following situations:

- recognition of the termination signal for 480-550 ms;
- carrier loss with a duration longer than 1s.

DCE B upon recognition of the termination signal will not take any action if it is in the normal data mode.



Time duration
T1 : 320 - 400 ms
T2 : ≥ 550 ms
T3 : 100 - 150 ms
T4 : 480 - 550 ms

Note 1 - Line signals that are transmitted before reception of preparatory signal is completed, and after loopback is released, depend upon the data signals transmitted by the DTE on circuit 103.

Note 2 - Binary 0 (SPACE) and binary 1 (MARK) correspond to the frequencies F_A and F_Z respectively.

FIGURE 6/V.54

Loop 2 signalling method in asynchronous modems

ANNEX A

(to Recommendation V.54)

State diagrams

A.1 *Introduction*

Procedures as outlined in §§ 5, 6 and 7 of Recommendation V.54 are further explained in this Annex by means of state diagrams.

In order to facilitate understanding of these diagrams the following information is provided.

A.2 *Location*

The loop device is considered to be functionally located between the DTE and the remaining part of the DCE.

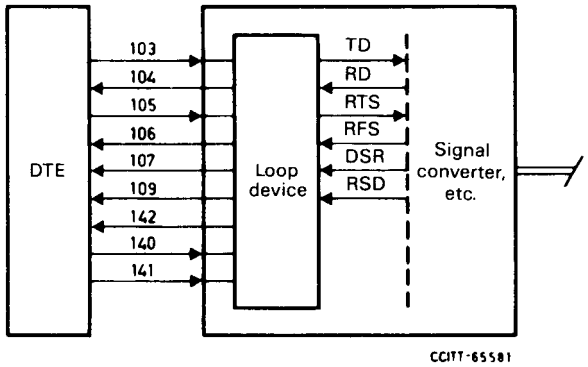


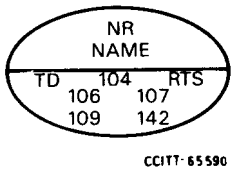
FIGURE A-1/V.54

During the data phase (i.e. no test loops applied), the following relations exist:

TD	(transmitted data)	=	103;
RD	(received data)	=	104;
RTS	(request to send)	=	105;
RFS	(ready for sending)	=	106;
DSR	(data set ready)	=	107;
RSD	(data channel received line signal detector)	=	109.

A.3 *Legend*

A.3.1 *States*



NR	State Number, with:
	LC = Loop Condition
	TL = Timing Loop;
NAME	State name;
TD	Signal on circuit TD to signal converter;
104	Signal on circuit 104 to DTE;
RTS	Signal on circuit RTS to signal converter;
106	Signal on circuit 106 to DTE;
107	Signal on circuit 107 to DTE;
109	Signal on circuit 109 to DTE;
142	Signal on circuit 142 to DTE;

A.3.2 *Signals*

"1"	Steady binary one;
OFF	Continuous OFF (= "1");
ON	Continuous ON (="0");
PREP	Preparatory pattern;
ACK	Acknowledgment pattern;

TERM	Termination pattern;
103	Follows circuit 103 from DTE;
RD	Follows circuit RD from signal converter;
105	Follows circuit 105 from DTE;
RFS	Follows circuit RFS from signal converter;
DSR	Follows circuit DSR from signal converter;
RSD	Follows circuit RSD from signal converter.

A.3.3 *Events*

14n ON	OFF to ON transition on circuit 14n;
14n OFF	ON to OFF transition on circuit 14n;
Peripheral	Valid in peripheral DCE;
intermed.	Valid in intermediate DCE;
nnnn	After nnnn bit intervals;
XXX rec.	Recognition of pattern XXX;
Own address	Recognition of unique DCE address sequence;
Other address	Recognition of other address sequence;
RSD OFF 1s	Circuit RSD OFF for 1 second.

A.4 *Examples*

In the lower half of the state symbols, the condition of all interchange circuits that originate in the loop device are given in the order:

- TD (to signal converter);
- 104 (to DTE);
- RTS (to signal converter);
- 106 (to DTE);
- 107 (to DTE);
- 109 (to DTE); and
- 142 (to DTE).

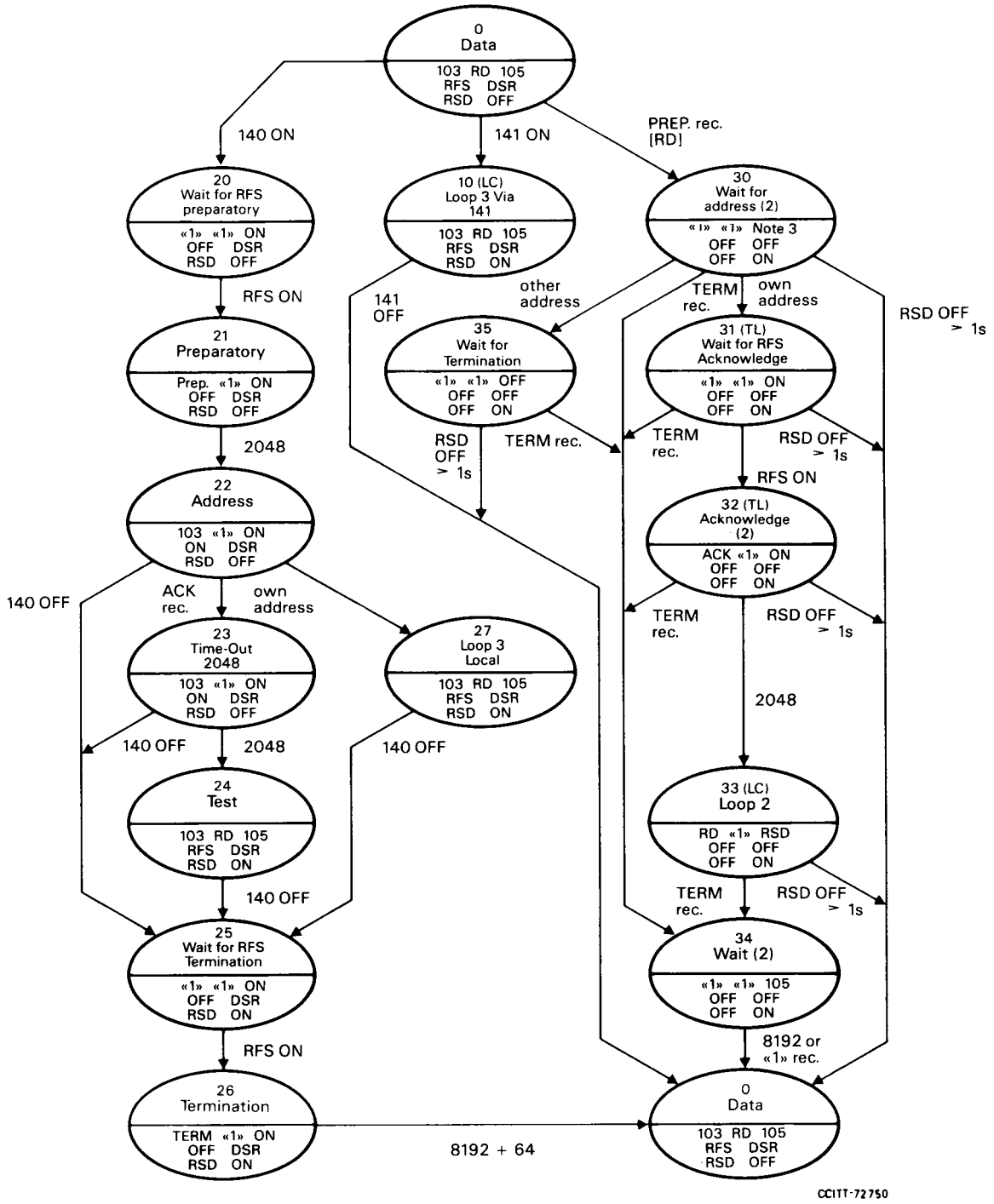
For example:

"RD" in the first position means that circuit TD to the signal converter is connected inside the loop device to RD from the signal converter.

"ACK" in the second position means that the acknowledgment pattern is transmitted on circuit 104.

"OFF" in the third position means that circuit RTS to the signal converter is kept in the OFF condition.

"RFS" in the fourth position means that circuit 106 to the DTE follows circuit RFS from the signal converter.



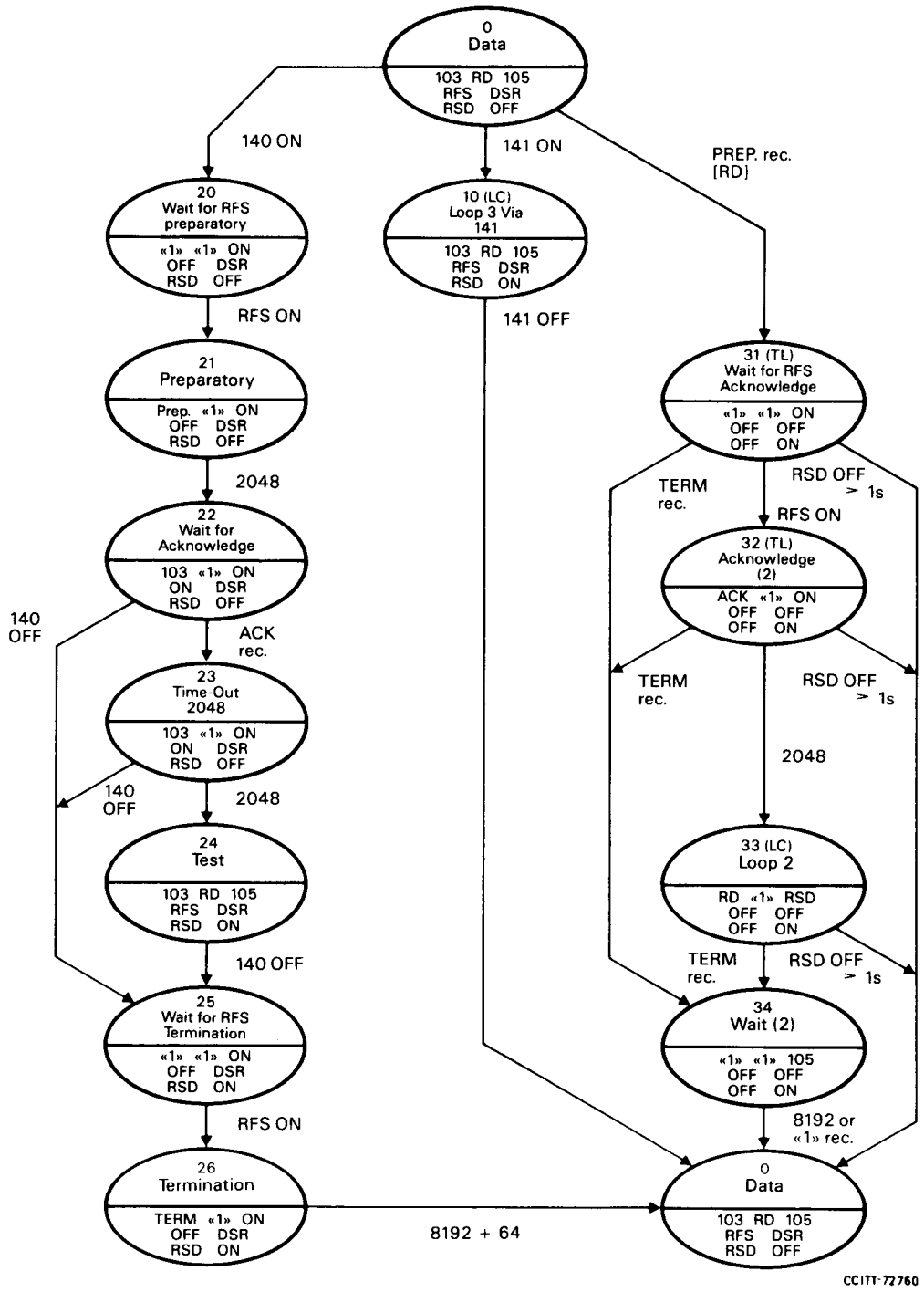
Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 30.

Note 3 - The condition of circuit RTS in state 30 may depend on the actual configuration. Normally circuit RTS will remain unchanged when moving from state 0 to state 30.

FIGURE A-2/V.54

State diagram for simple multipoint circuits

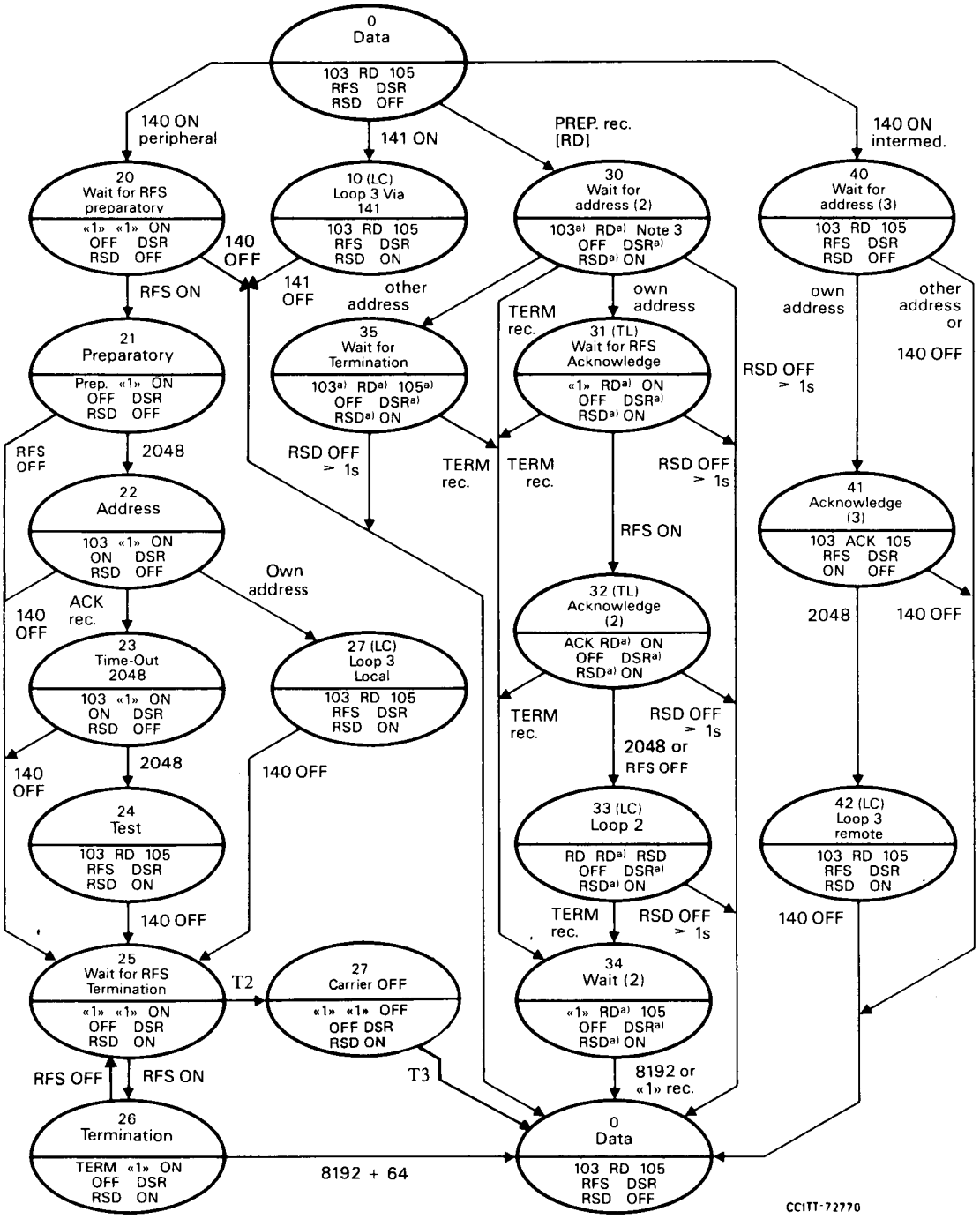


Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 31.

FIGURE A-3/V.54

State diagram for point-to-point circuits



a) Not clamped in intermediate DCE; clamped («1» or OFF) in peripheral DCE.

Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 30.

Note 3 - The condition of circuit RTS in state 30 may depend on the actual configuration. Normally circuit RTS will remain unchanged when moving from state 0 to state 30.

Note 4 - Where interconnection of circuit 109 in DCE 11 to circuit 105 in DCE 12 is possible, during Loop 2 the same condition as in peripheral DCE B is permitted on the interface.

Note 5 – Timer T2 is turned on at first entry of state 25 and turned OFF on exit of state 26.

Note 6 – Timer T3 is turned on at entry of state 27.

FIGURE A-4/V.54

State diagram for tandem circuits

Reference

[1] CCITT Recommendation *Influence of national systems on stability, talker echo and listener echo in international connections*, Vol. III, Rec. G.122.