INTERNATIONAL TELECOMMUNICATION UNION

ITU-T V.27 *bis*

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DATA COMMUNICATION OVER THE TELEPHONE NETWORK

4800/2400 BITS PER SECOND MODEM WITH AUTOMATIC EQUALIZER STANDARDIZED FOR USE ON LEASED TELEPHONE-TYPE CIRCUITS

ITU-T Recommendation V.27 *bis*

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.27 *bis* was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.27 *bis*

4800/2400 BITS PER SECOND MODEM WITH AUTOMATIC EQUALIZER STANDARDIZED FOR USE ON LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

Introduction

This modem is intended to be used over any general leased circuits not necessarily conforming to Recommendation M.1020 [1]. A provision for a fast start-up sequence is made to allow the use of this modem for multipoint polling applications if the circuits used conform to Recommendation M.1020.

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems. This Recommendation does not eliminate the need for manually equalized modems according to Recommendation V.27 or application of other automatically equalized 4800 bits per second modems.

The provisions of this Recommendation are to be regarded as provisional in order to provide service where it is urgently required and between locations where it is expected that a reasonably satisfactory service can be given.

1 Principal characteristics

The principal characteristics for this recommended modem are very similar to the characteristics of a modem conforming to Recommendation V.27 with the exception of the equalizer used and these characteristics are as follows:

a) operates in a full-duplex or half-duplex mode over 4-wire leased circuits or in a half-duplex mode over 2-wire leased circuits;

b) at 4800 bits per second operation, modulation is 8-phase differentially encoded as described in Recommendation V.27;

c) reduced rate capability at 2400 bits per second with 4-phase differentially encoded modulation scheme as described in Recommendation V.26, Alternative A;

d) possibility of a backward (supervisory) channel at modulation rates up to 75 bauds in each direction of transmission, the provision and the use of these channels being optional;

e) inclusion of an automatic adaptive equalizer with a specific start-up sequence for Recommendation M.1020 [1] lines and an alternate start-up sequence for much lower grade lines.

2 Line signals at 4800 and 2400 bits per second operation

2.1 *Carrier frequency*

The carrier frequency is to be 1800 ± 1 Hz. No separate pilot tones are provided. The power levels used will conform to Recommendation V.2.

2.1.1 *Spectrum at 4800 bits per second*

A 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1000 Hz and 2600 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1000 Hz and 2600 Hz.

2.1.2 *Spectrum at 2400 bits per second*

A minimum of 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1200 Hz and 2400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1200 Hz and 2400 Hz.

2.2 *Division of power between the forward and backward channel*

If simultaneous transmission of the forward and backward channels occurs in the same direction, a backward channel should be 6 dB lower in power level than the forward (data) channel.

2.3 *Operation at 4800 bits per second*

2.3.1 *Data signalling and modulation rate*

The data signalling rate shall be 4800 bits per second ± 0.01%, i.e. the modulation rate is 1600 bauds ± 0.01%.

2.3.2 *Encoding data bits*

The data stream to be transmitted is divided into groups of three consecutive bits (tribits). Each tribit is encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.27 *bis).* At the receiver, the tribits are decoded and the bits are reassembled in correct order. The left-hand digit of the tribit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.27 *bis*

Tribit values			Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note - The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.4 *Operation at 2400 bits per second*

2.4.1 *Data signalling and modulation rate*

The data signalling rate shall be 2400 bits per second ± 0.01%, i.e. the modulation rate is 1200 bauds ± 0.01%.

2.4.2 *Encoding data bits*

At 2400 bits per second the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 2/V.27 *bis).* At the receiver, the dibits are decoded and reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 2/V.27 *bis*

Dibit values	Phase change (see Note)
00	0°
01	90°
11	180°
10	270°

Note - The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5 *Operating sequences*

2.5.1 *Turn-ON sequence*

During the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106, synchronizing signals for proper conditioning of the receiving modem must be generated by the transmitting modem. These are signals to establish carrier detection, AGC if required, timing synchronization, equalizer convergence and descrambler synchronization.

Two sequences are defined, i.e.:

a) a short one for 4-wire circuits conforming to Recommendation M.1020 [1] operation,

b) a long one for 4-wire circuits which are much worse than Recommendation M.1020 [1] and for 2-wire circuits.

The sequences, for both data rates, are divided into three segments as in Table 3/V.27 *bis.*

TABLE 3/V.27 *bis*

	Segment 1	Segment 2	Segment 3	Total of Segments 1, 2 and 3	
Type of line signal	Continuous 180° phase reversals	0°-180° 2-phase equalizer conditioning pattern	Continuous scrambled ONEs	Total "**Turn**-ON" sequence time	
				4800 bit/s	2400 bit/s
Number of symbol intervals (SI) [a]	a) 14 SI b) 50 SI	a) 58 SI b) 1074 SI	8 SI	a) 50 ms b) 708 ms	a) 67 ms b) 943 ms

[a] SI = symbol intervals. The durations of Segments 1, 2 and 3 are expressed in number of symbol intervals, these numbers beign the same in fallback operation.

2.5.1.1 The composition of Segment 1 is continuous 180° phase reversals on line for 14 symbol intervals in the case of sequence a), for 50 symbol intervals in the case of sequence b).

2.5.1.2 Segment 2 is composed of an equalizer conditioning pattern which is derived from a pseudo-random sequence generated by the polynomial:

$$1 + x^{-6} + x^{-7}$$

2.5.1.2.1 For operation at 4800 bit/s the equalizer conditioning pattern is derived by using every third bit of the pseudo-random sequence defined in § 2.5.1.2. When the derived pattern contains a ZERO, 0° phase change is transmitted; when

it contains a ONE, 180° phase change is transmitted. Segment 2 begins with 0°, 180°, 180°, 180°, 180°, 180°, 0°, . . . according to the derived pattern and continues for 58 symbol intervals in the case of sequence a) and for 1074 symbol intervals in the case of sequence b). An example of the detailed sequence generation is described in Appendix I.

2.5.1.2.2 On leased circuits, considering that there exist modems which comply with § 2.5.1.2.1 at 4800 bit/s, but which differ in their "Turn-ON" sequences at 2400 bit/s, the following alternative equalizer conditioning patterns are defined:

i) In the first alternative, the equalizer conditioning pattern is identical to that defined in § 2.5.1.2.1.

ii) In the second alternative, the equalizer conditioning pattern is derived by using every second bit of the pseudo-random pattern defined in § 2.5.1.2. When the derived sequence contains a ZERO, 0° phase change is transmitted; when it contains a ONE, 180° phase change is transmitted. Segment 2 begins with 0°, 180°, 0°, 180°, 180°, 0°, 180°, . . . according to the derived pattern and continues for 58 symbol intervals in the case of sequence a) and for 1074 symbol intervals in the case of sequence b).

2.5.1.3 Segment 3 commences transmission according to the encoding described in §§ 2.3 and 2.4 above with continuous data ONEs applied to the input of the data scrambler. Segment 3 is 8 symbol intervals. At the end of Segment 3, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

2.5.1.4 The phase change sequences for Segments 2 and 3 for 4800 bit/s and 2400 bit/s are shown in Table 4/V.27 *bis*.

TABLE 4/V.27 *bis* [a)]

Data speed		Segment 2	Segment 3
4800 bit/s	Phase change PRS [b)]	0° 180° 180° 180° 180° 180° 0° .... 180° 180° 0° 0° 0̲11 1̲01 1̲01 1̲00 1̲00 1̲01 0̲01 .... 1̲10 1̲00 0̲10 0̲01	270° 225° 315° 90° 45° 45° 180° 180° 100 110 101 010 000 000 111 111
2400 bit/s alternative i)	Phase change PRS [b)]	0° 180° 180° 180° 180° 180° 0° .... 180° 180° 0° 0° 0̲11 1̲01 1̲01 1̲00 1̲00 1̲01 0̲01 .... 1̲10 1̲00 0̲10 0̲01	270° 90° 270° 270° 270° 270° 0° 0° 10 01 10 10 10 10 00 00
2400 bit/s alternative ii)	Phase change PRS [b)]	0° 180° 0° 180° 180° 0° 180° .. 180° 0° 180° 180° 180° 0° 0̲1 1̲1 0̲1 1̲0 1̲1 0̲0 1̲0 ... 1̲0 0̲0 1̲0 1̲0 1̲1 0̲0	0° 90° 90° 180° 270° 0° 180° 270° 00 01 01 11 10 00 11 10
	Duration	←——— 58 or 1074 symbol intervals ———→ (Beginning and ending PRS and symbol sequences are the same for both durations)	←——— 8 symbol intervals ———→

a) For a description of how the alternative sequences for Segments 2 and 3 may be generated, refer to the Note at the end of Appendix I.

b) PRS is the pseudo-random sequence defined in § 2.5.1.2. The underlined bits determine the phase changes.

2.5.2 *Turn-OFF sequence*

The line signal emitted after the ON to OFF transition of circuit 105 is divided into two segments as shown in Table 5/V.27 *bis.*

TABLE 5/V.27 *bis*

	Segment A	Segment B	Total of Segments A and B
Type of line signal	Remaining data followed by continuous scrambled ONEs	No transmitted energy	Total "Turn-OFF" time
Duration	5 to 10 ms	20 ms	25 to 30 ms

If an OFF to ON transition of circuit 105 occurs during the Turn-OFF sequence, it will not be taken into account until the end of the Turn-OFF sequence.

In addition, in the case of half-duplex operation on two wires, if circuit 105 goes ON during the reception of the Segment A of the Turn-OFF sequence, optionally the transmission of the Turn-ON sequence shall be started within a time period of less than 20 ms after the end of reception of Segment A.

3 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance of the transmitter is ± 1 Hz and assuming a maximum drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

4 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc. to be as recommended for the backward channel in Recommendation V.23. This does not preclude the use of a higher speed backward channel with operational capability of 75 bauds or higher, bearing the same characteristic frequencies as the V.23 backward channel.

5 Interchange circuits

5.1 *List of essential interchange circuits* (Table 6/V.27 bis)

5.2 *Response times of circuits 106, 109, 121 and 122* (Table 7/V.27 bis)

5.2.1 *Circuit 109*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104.

5.2.2 *Circuit 106*

Circuit 106 response times are from the connection of an ON or OFF condition on circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106.

TABLE 6/V.27 *bis*

Interchange circuit		Forward (data) channel half-duplex of full-duplex (see Note)	
No.	Designation	Without backward channel	With backward channel
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105	Request to send	X	X
106	Ready for sending	X	X
107	Data set ready	X	X
108/1	Connect data set to line	X	X
109	Data channel received line signal detector	X	X
111	Data signal rate selector (DTE source)	X	X
113	Transmitter signal element timing (DTE source)	X	X
114	Receiver signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
118	Transmitter backward channel data		X
119	Received backward channel data		X
120	Transmit backward channel line signal		X
121	Backward channel ready		X
122	Backward channel received line signal detector		X

Note - All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

TABLE 7/V.27 *bis*

Response times

Circuit 106	4800 bits per second	2400 bits per second
OFF to ON	a) 25 ms b) 708 ms	a) 67 ms b) 944 ms
ON to OFF	≤ 2 ms	
Circuit 109		
OFF to ON	See § 5.2.1	
ON to OFF	5 to 15 ms	
Circuit 121		
OFF to ON	80 to 160 ms	
ON to OFF	≤ 2 ms	
Circuit 122		
OFF to ON	< 80 ms	
ON to OFF	15 to 80 ms	

Note - a) and b) refer to sequence a) and sequence b) as defined in § 2.5.1.

5.3 *Threshold of data channel and backward channel received line signal detectors*

Levels of received line signal at receiver line terminals:

For use over ordinary quality leased circuits (ref. Recommendation M.1040 [2])

Threshold for circuits 109/122:

- greater than -43 dBm: OFF to ON
- less than -48 dBm: ON to OFF

- *For use over special quality leased circuits* (ref. Recommendation M.1020 [1])

Threshold for circuit 109:

- greater than - 26 dBm: OFF to ON
- less than -31 dBm: ON to OFF

Threshold for circuit 122:

- greater than - 34 dBm: OFF to ON
- less than -39 dBm: ON to OFF

The condition of circuits 109 and 122 for levels between the above levels is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

5.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

5.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

5.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note - Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangement

Clocks should be included in the modem to provide the data terminal equipment with transmitter element timing, circuit 114 and receiver signal element timing, circuit 115. The transmitter element timing may be originated in the data terminal equipment and be transferred to the modem via circuit 113.

8 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial:

$$1 + x^{-6} + x^{-7}$$

with additional guards against repeating patterns of 1, 2, 3, 4, 6, 8, 9 and 12 bits, shall be included in this modem. In Appendix I, Figure I-2/V.27 *bis* shows a suitable logical arrangement (see Note). The scrambler/descrambler is the same as that in Recommendation V.27 with the addition of circuitry to guard against repeating patterns of 8 bits.

Note - Figures I-1/V.27 *bis* and I-2/V.27 *bis* in Appendix I are given as an indication only, since with another technique these logical arrangements might take another form.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence, and at the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

9 Equalizer

An automatic adaptive equalizer shall be provided in the receiver. The receiver shall incorporate a means of detecting loss of equalization and be able to recover equalization from the normal data-modulated received line signal without initiating a new synchronizing signal from the distant transmitter.

10 Options

Since this modem is equipped with an automatic adaptive equalizer, and can operate on 2-wire lines, operation over the general switched network is possible. Thus, in the event of failure of the leased line, the general switched network may serve as a stand-by facility.

Options can be added to this modem in order to allow the use of the general switched network when the leased line fails. These options can also be added for use on 2-wire leased lines where echo protection is required.

Additional information for these options can be found in Recommendation V.27 *ter*.

11 The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

At 4800 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1100 Hz to 2500 Hz.

At 2400 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1300 Hz to 2300 Hz.

APPENDIX I

(to Recommendation V.27 *bis)*

A two phase equalizer training generator for 4800 bit/s

Rapid convergence for the equalizer with the least amount of circuitry is more readily accomplished by sending only an in-phase or out-of-phase carrier during training. This implies that the only tribits sent to the modulator will be 001 (0° phase) or 111 (180° phase). Refer to Figure I-1/V.27 *bis* for circuitry to generate the sequence and Figure I-3/V.27 *bis* for timing the sequence.

Let T1 be a timing signal equal to 1600 Hz (symbol clock), that is true (high) for one 4800-Hz period, and low for two 4800-Hz clock periods. T2 is the inversion of Tl.

During Tl select the input to the scrambler, during T2 select the first stage of the scrambler. During the period when T2 is high, C forces the output high. This may be accomplished by circuitry shown in Figure I-2/V.27 *bis.*

If T1 is forced continually high and T2 is forced continually low, normal operation is restored.

In order to ensure consistent training, the same pattern should always be sent. To accomplish this, the data input to the scrambler should be in mark hold during the training, and the first seven stages of the scrambler should be loaded with 0011110 (right-hand-most first in time) on the first coincidence on Tl and the signal that will cause the mute should be removed from the transmitter output. [Generally this signal will be *Request To Send* (RTS)].

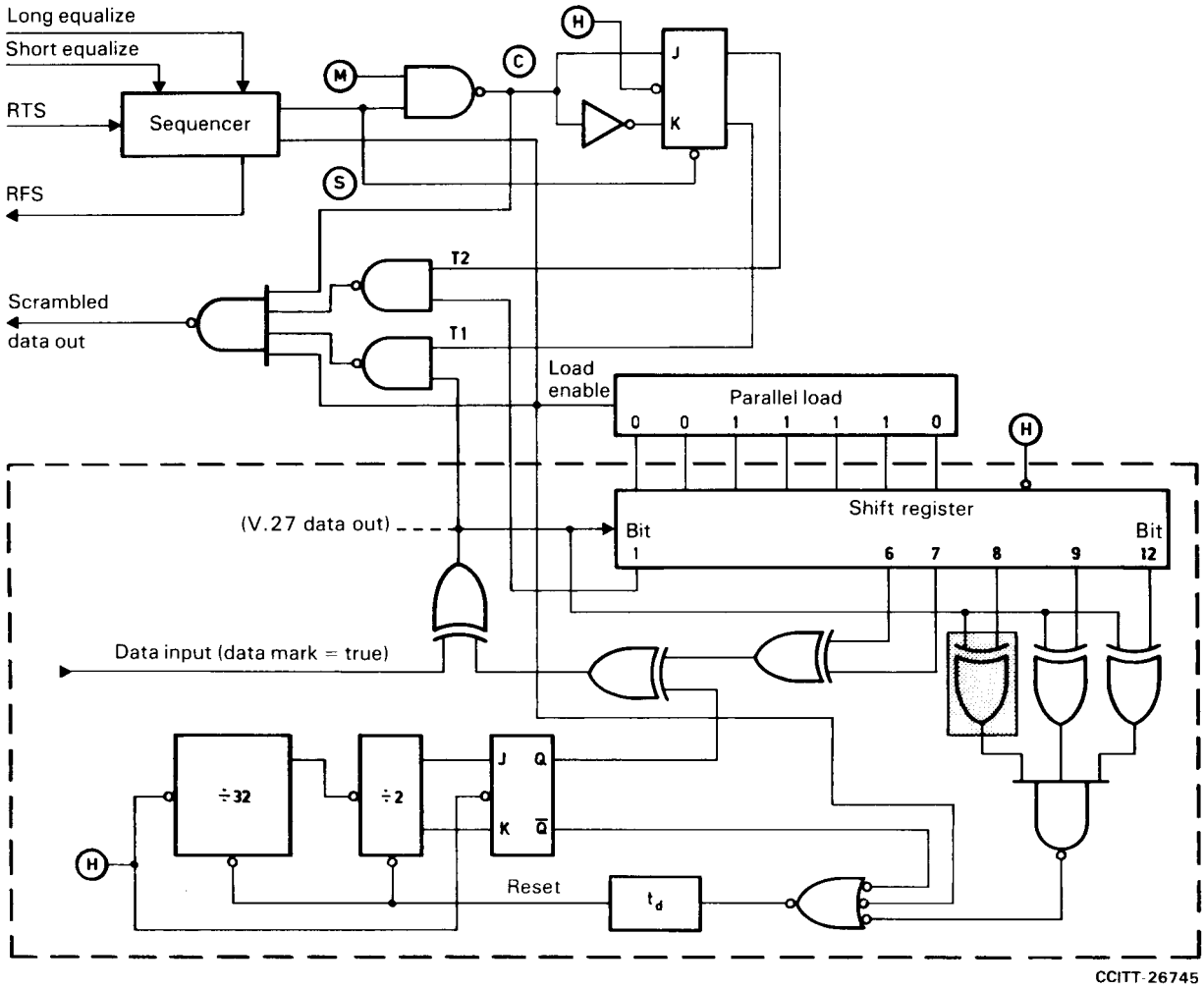
This particular starting point was chosen in order to ensure a pattern that has continuous 180° phase reversals at the beginning in order to ensure rapid clock acquisition, followed by a pattern that will ensure rapid equalizer convergence.

Within eight symbol intervals prior to the ON condition of *Ready For Sending* (RFS), the scrambler should be switched to normal operation, keeping the scrambler in mark hold until RFS, to synchronize the descrambler.

Note - At 2400 bits per second, a similar technique may be used with appropriate clocking changes, as shown in Table I-1/V.27 *bis.*

TABLE I-1/V.27 bis

		Segment 2	Segment 3
Clock (H)	i)	3600 Hz	2400 Hz
	ii)	2400 Hz	2400 Hz
Clock (M)	i)	1200 Hz	1200 Hz
	ii)	1200 Hz	1200 Hz



Note 1 – The dotted line encloses the V.27 scrambler.

Note 2 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 3 – (H) is 3 times baud rate clock.

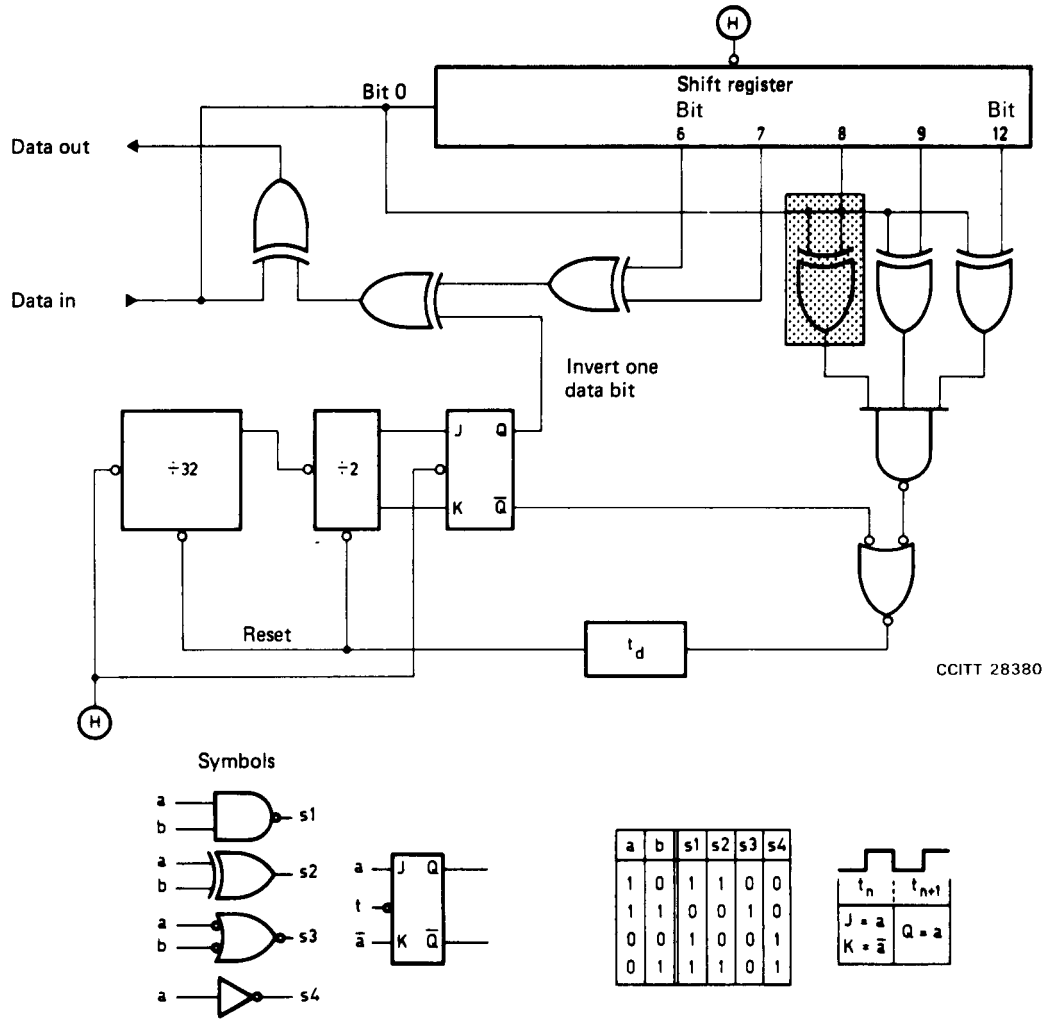
Note 4 – (M) is baud rate clock (1600 Hz).

Note 5 – Diagrams shown with positive logic.

Note 6 – Signals (C) and (S) are identified only to correlate with Figure I-3/V.27 *bis*.

FIGURE I-1/V.27 *bis*

An example of sequence generator and scrambler circuitry for 4800 bit/s



a	b	s1	s2	s3	s4
1	0	1	1	0	0
1	1	0	0	1	0
0	0	1	0	0	1
0	1	1	1	0	1

t_n	t_{n+1}
J = a K = ā	Q = a

Note 1 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 2 – (H) represents clock signal. The negative going transition is the active transition.

Note 3 – There is a delay time due to physical circuits between a negative going transition of (H) and the end of the "0" state represented by t_d on the non-reset wire; therefore the first coincidence between bit 0 and bit 8 or bit 9 or bit 12 is not taken into account by the counter.

FIGURE I-2/V.27 *bis*

An example of descrambler circuitry

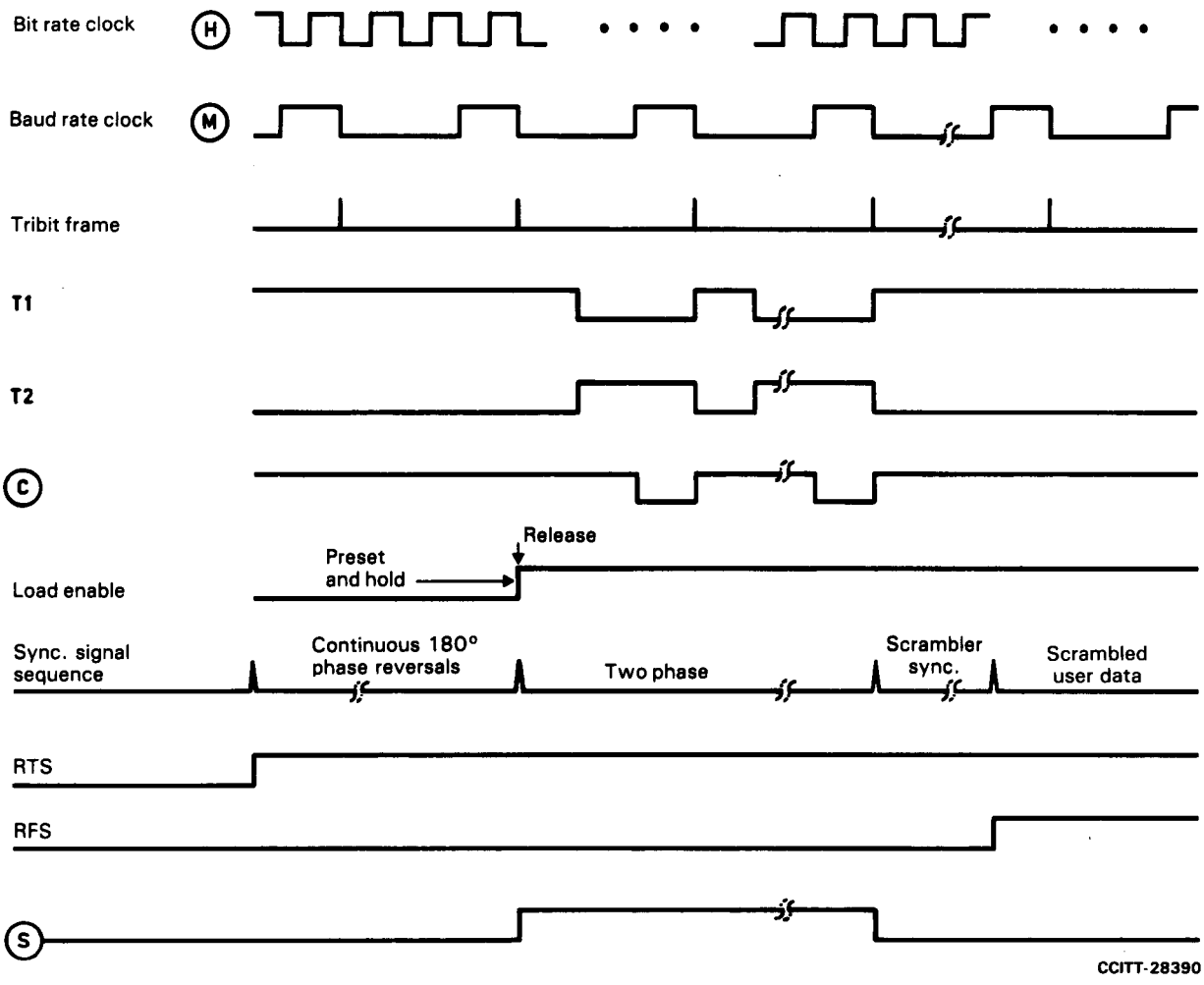


FIGURE I-3/V. 27 *bis*

Synchronizing signal sequence for 4800 bit/s (see Figure I-1/V.27 *bis)*

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special band-width conditioning*, Vol. IV, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of ordinary quality international leased circuits*, Vol. IV, Rec. M.1040.