INTERNATIONAL TELECOMMUNICATION UNION

ITU-T V.26 *ter*

TELECOMMUNICATION
STANDARDIZATION SECTOR
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DATA COMMUNICATION

OVER THE TELEPHONE NETWORK

2400 BITS PER SECOND DUPLEX MODEM USING THE ECHO CANCELLATION TECHNIQUE STANDARDIZED FOR USE ON THE GENERAL SWITCHED TELEPHONE NETWORK AND ON POINT-TO-POINT 2-WIRE LEASED TELEPHONE-TYPE CIRCUITS

ITU-T Recommendation V.26 *ter*

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.26 *ter* was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.26 *ter*

**2400 BITS PER SECOND DUPLEX MODEM
USING THE ECHO CANCELLATION TECHNIQUE
STANDARDIZED FOR USE ON THE GENERAL SWITCHED TELEPHONE NETWORK
AND ON POINT-TO-POINT 2-WIRE LEASED
TELEPHONE-TYPE CIRCUITS**

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

The CCITT,

considering

(a) that there is a demand for data transmission at 2400 bit/s in the duplex mode on the general switched telephone network (GSTN) and on point-to-point 2-wire leased telephone-type circuits;

(b) that there will be a demand to have compatibility with higher data signalling rate duplex modems in the fall-back mode;

(c) that in this case the echo cancellation technique (ECT) is foreseen,

unanimously declares

the view that the characteristics of the modems for this service shall provisionally be as follows:

1 Introduction

This modem is intended for use on connections on the GSTN and on point-to-point 2-wire leased telephone-type circuits (see Note 1). Its principal characteristics are as follows:

a) duplex mode of operation on the GSTN and point-to-point leased circuits,

b) half-duplex mode of operation (optional) on the GSTN and point-to-point leased circuits (Note 2),

c) channel separation by echo cancellation,

d) differential phase-shift modulation for each channel with synchronous line transmission at 1200 baud (nominal),

e) inclusion of a scrambler,

f) inclusion of a compromise or adaptive equalizer,

g) inclusion of test facilities,

h) operation with data terminal equipment (DTE) in the following modes:

2400 bit/s synchronous,

1200 bit/s synchronous (fall-back rate),

2400 bit/s start stop (optional),

1200 bit/s start stop (optional) (fall-back rate),

i) inclusion of an operating sequence intended to allow interworking with 2-wire duplex 4800 bit/s modem (which modem is for further study).

Note 1 - In certain countries the use of such a modem over the GSTN may not be allowed.

Note 2 - When the optional half-duplex mode of operation is used, provisions in § 7 shall supersede provisions given elsewhere in this Recommendation.

2 Line signals

2.1 *Carrier frequency*

The carrier frequency shall be 1800 ± 1 Hz. No separate pilot tones are provided.

2.2 *Data line signal level*

The power levels used will conform to Recommendation V.2.

2.3 *Equalizer*

If a fixed compromise equalizer is used, it shall be incorporated in the receiver. The characteristics of this equalizer may be selected by Administrations.

The possibility of producing compromise equalizer characteristics for international connections is for further study.

If an adaptive equalizer is used, it shall be able to converge on data signals at 2400 bit/s without a training sequence.

2.4 *Spectrum and group-delay characteristics*

A 100% raised cosine amplitude spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1200 Hz and 2400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1200 Hz and 2400 Hz.

The group-delay of the transmit filters shall be within ± 100 microseconds over the frequency range 1200-2400 Hz.

2.5 *Modulation*

2.5.1 *Data signalling rates*

The data signalling rate transmitted to line shall be 2400 bit/s or 1200 bit/s ± 0.01% with a modulation rate of 1200 baud ± 0.01%.

2.5.2 *Encoding of data bits*

2.5.2.1 *2400 bits per second*

At 2400 bit/s the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 1/V.26 *ter).* At the receiver, the dibits are decoded and reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modern after the scrambler.

TABLE 1/V.26 *ter*

Line encoding at 2400 bit/s

Dibit values	Phase change (see Note)
00	0°
01	90°
11	180°
10	270°

Note - The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5.2.2 *1200 bits per second*

At 1200 bit/s each bit shall be encoded as a phase change relative to the phase of the preceding signal element (see Table 2/V.26 *ter).*

TABLE 2/V.26 *ter*

Line encoding at 1200 bit/s

Bit values	Phase change (see Note)
0	0°
1	180°

Note - The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.6 *Received signal frequency tolerance*

The receiver shall be able to operate with frequency offsets in the signal received from the other modem of up to ± 7 Hz.

2.7 *Synchronizing signals*

Synchronizing signals are used in the operating sequence and in the half-duplex mode (see §§ 6.3 and 7). The synchronizing signals, for both data signalling rates, are divided into two segments as follows:

2.7.1 The composition of segment 1 is continuous 180° phase reversals for 32 symbol intervals.

2.7.2 Segment 2 is a pattern derived by scrambling binary ones with the scramblers defined in § 5. The length of the pattern is 64 bits (32 symbol intervals) for 2400 bit/s and 64 bit/s (64 symbol intervals) for 1200 bit/s. The patterns are defined in Table 3/V.26 *ter.* See also Appendix I.

TABLE 3/V.26 *ter*

Data signalling rate	Srambler (see § 5)	Segment 2 phase changes (in degrees)
2400 bit/s	GPC	0, 180, 180, 180, 180, 0, 0, 0, 0, 180, 180, 270, 90, 180, 0, 0, 90, 180, 0 . . .
2400 bit/s	GPA	0, 180, 180, 180, 180, 0, 0, 0, 0, 180, 180, 270, 90, 180, 0, 180, 180, 270, 0 . . .
1200 bit/s	GPC	0, 0, 180, 180, 180, 180, 180, 180, 180, 180, 0, 0, 0, 0, 0, 0, 0, 0, 180, 180, 180, 180, 180, 0, 0, 180, 180, 180, 0, 0, 0, 0, 0, 180, 180, 180 . . .
1200 bit/s	GPA	0, 0, 180, 180, 180, 180, 180, 180, 180, 180, 0, 0, 0, 0, 0, 0, 0, 0, 180, 180, 180, 180, 180, 0, 0, 180, 180, 180, 0, 0, 180, 180, 180, 0, 180, 0 . . .

3 Interchange circuits

3.1 *Essential and optional interchange circuits*

These are listed in Table 4/V.26 *ter.*

TABLE 4/V.26 *ter*

Interchange circuit (see Note 1)		Notes
No.	Designation	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	
106	Ready for sending	
107	Data se ready	
108/1 or	Connect data set to line	2
108/2	Data terminal ready	2
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	
112	Data signalling rate selector (DCE source)	3
113	Transmitter signal element timing (DTE source)	4
114	Transmitter signal element timing (DCE source)	5
115	Receiver signal element timing (DCE source)	5
125	Calling indicator	6
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 - All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.5).

Note 2 - This circuit shall be capable of operation as circuit 108/1 or circuit 108/2 depending on its use.

Note 3 - This circuit is optional.

Note 4 - When the modem is not operating in a synchronous mode at the interface, any signals on circuit 113 shall be disegarded. Many DTEs operating in an asynchronous mode do not have a generator connected to this circuit.

Note 5 - When the modem is not operating in a synchronous mode, this circuit shall be clamped to the OFF condition. Many DTEs operating in an asynchronous mode do not terminate this circuit.

Note 6 - This circuit is for use with the general switched telephone network only.

3.2 *Circuit 106 response times* (see Table 5/V.26 *ter)*

Circuit 106 response times are from the application of an ON or OFF condition on circuit 105. See also § 6.3 for conditions of circuit 106 during the operating sequence.

TABLE 5/V.26 *ter*

	Constant carrier
Circuit 106	
OFF to ON	≤ 2 ms
ON to OFF	≤ 2 ms

3.3 *Threshold and response times of circuit 109*

3.3.1 *Threshold*

The level of received line signal at the receive line terminals of the modem for all types of connections, i.e. the general switched telephone network or non-switched 2-wire leased telephone type circuits, is:

- greater than -43 dBm: circuit 109 ON
- less than -48 dBm: circuit 109 OFF

Where transmission conditions are known and allowed, it may be desirable at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. -33 dBm and -38 dBm respectively).

In addition, for use over special quality leased circuits (see Recommendation M.1020) the response levels of the received line signal detector shall be:

- greater than -26 dBm: circuit 109 ON
- less than -31 dBm: circuit 109 OFF

The condition of circuit 109 between the ON and OFF levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for the ON to OFF transition.

3.3.2 *Response time*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104.

The ON to OFF response time of circuit 109 is 5 ms to 15 ms. See also § 6.3 for the condition of circuit 109 during the operating sequence.

Following a drop-out after the initial handshake, circuit 109 shall be turned ON 40 to 50 ms after the level of the receiver signal appearing at the line terminal of the modem exceeds the relevant threshold defined in § 3.3. 1.

3.4 *Timing arrangement*

Clocks shall be included in the modem to provide the DTE with transmitter element timing (circuit 114) and receiver signal element timing (circuit 115). The transmitter element timing may be originated in the DTE and be transferred to the modem via the appropriate interchange circuit, circuit 113.

3.5 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note - Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.6 *Fault condition of interchange circuits*

(See § 7 of Recommendation V.28 for association of the receiver failure detection types.)

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Modes of operation

The modem can be configured for the following modes of operation:

Mode i) 2400 bit/s ± 0.01% synchronous

Mode ii) 2400 bit/s start-stop 8, 9, 10 or 11 bits per character (optional)

Mode iii) 1200 bit/s ± 0.01% synchronous

Mode iv) 1200 bit/s start-stop 8, 9, 10 or 11 bits per character (optional).

4.1 *Transmitter*

4.1.1 In the synchronous modes of operation, the modem shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or circuit 114. The data shall then be scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.

When circuit 114 is used, the modem shall derive its line signal clock from the internal clock source or, alternatively, from the receive signal element timing.

4.1.2 In the start-stop modes, the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of 2400 or 1200 bit/s. The start-stop data to be transmitted shall be converted in conformity with Recommendation V.14 to a synchronous data stream suitable for transmission in accordance with § 4.1.1.

4.2 *Receiver*

4.2.1 In the synchronous modes of operation, the modem shall give synchronous data to the DTE on circuit 104 under control of circuit 115.

4.2.2 In the start-stop modes, demodulated synchronous data shall be passed to the converter in conformity with Recommendation V.14 for regaining the data stream of start-stop characters.

The intracharacter signalling rate provided to the DTE over circuit 104 shall be in the ranges given in Table 6/V.26 *ter* when operating in the basic or in the extended signalling rate ranges, respectively.

TABLE 6/V.26 *ter*

Intracharacter signalling rate range

Data rate	Signalling rate range	
	Basic	Extented
2400 bit/s 1200 bit/s	2400 to 2424 bit/s 1200 to 1212 bit/s	2400 to 2455 bit/s 1200 to 1227 bit/s

5 Scrambler and descrambler

Each transmission direction uses a different scrambler. The way to allocate the scramblers/descramblers is described in § 6.1.1.

A self-synchronizing scrambler/descrambler shall be included in the modem. According to the direction of transmission (see § 6.1) the generating polynominal is: GPC = $1 + x^{-18} + x^{-23}$ or GPA = $1 + x^{-5} + x^{-23}$.

At the transmitter the scrambler shall effectively divide the message polynomial (of which the input data sequence represents the coefficients in descending order) by the scrambler generating polynomial to generate the transmitted sequence; at the receiver the received polynomial (of which the received data sequence represents the coefficient in descending order) shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix I.

6 Operating sequence

6.1 *Scrambler/descrambler allocation and signalling rate selection*

6.1.1 *General switched telephone network (GSTN)*

On the general switched telephone network the modem at the calling data station shall use the scrambler with the GPC generating polynomial and the descrambler with the GPA generating polynomial (call mode). The modem at the answering data station shall use the scrambler with the GPA generating polynomial and the descrambler with the GPC generating polynomial (answer mode).

In some situations, however, for example, when calls are established on the GSTN by operators, bilateral agreement on call mode/answer mode allocation will be necessary.

The calling and answering modems automatically condition themselves to operate at the correct data signalling rate by exchanging rate patterns at the bit rate of 1200 bit/s during the operating sequences, as defined in § 6.3.1.

6.1.2 *Point-to-point leased circuits*

Scrambler/descrambler allocation, data signalling rate selection and call mode and answer mode designation on point-to-point leased circuits will be by bilateral agreement between Administrations or users.

6.1.3 *Rate patterns*

The rate pattern is a scrambled sequence of a particular repeated octet transmitted 32 times.

Out of the possible 256 binary numbers, the 34 following hexadecimal numbers are selected:

01 - 03 - 05 - 07 - 09 - 0B - 0D - 0F - 11 - 13 - 15 - 17 - 19 - 1B - ID - 1F - 25 - 27 - 2B - 2D - 2F - 33 - 35 - 37 - 3B - 3D - 3F - 55 - 57 - 5B - 5F - 6F - 77 - 7F

Each of the binary octets (numbers listed above) may be replaced by one of its rotations.

The transmission of an octet begins by the least significant bit.

Table 7/V.26 *ter* shows the relationship between an octet value and one or two bit rates (see Note 2 of the table) enabled in a modem.

TABLE 7/V.26 *ter*

Rate pattern octet coding

Octet (see Note 1)		Bit rate (bit/s)		
Hexadecimal	Binary	1200	2400	4800 (see Note 2)
	LSB			
01	0 0 0 0 0 0 0 1	X		
03	0 0 0 0 0 0 1 1		X	
05	0 0 0 0 0 1 0 1			X
07	0 0 0 0 0 1 1 1	X	X	
09	0 0 0 0 1 0 0 1		X	X

Note 1 - In the case of an interface according to Recommendation V.24, only two rates can be selected by circuits 111 and 112. A new kind of interface under study may enlarge the possibilities.

Note 2 - These octets assignments are provisional.

6.2 *V.25 automatic answering sequence*

The V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted on point-to-point leased circuits or on national connections on the GSTN, where permitted by the Administration.

6.3 *Operating protocol*

The means of achieving automatic bit rate selection, initial echo cancellation and synchronism between the call mode and the answer mode modems on international GSTN connections and leased lines are shown in Figure 1 /V.26 *ter*.

The automatic bit rate selection, initial echo cancellation and synchronizing signals are based on a half-duplex procedure. After this procedure, both modems shall continue to operate adaptive echo cancellation during duplex data transmission.

The operating sequence is divided into three sub-sequences: A, B and C (see Note).

Sequence A is the answering sequence according to Recommendation V.25.

Sequence B is the data bit rate selection sequence operated at 1200 bit/s.

Sequence C is the echo cancelling sequence operated at the selected bit rate.

At the end of these three sequences, the modem is conditioned to transmit and receive data.

Note - Manufacturers should note that the impedance of the modems as seen by the telephone line should not be varied throughout the duration of the connection.

6.3.1 *Description*

6.3.1.1 *Sequence A (answering sequence)*

6.3.1.1.1 *Call mode modem*

a) On connection to line it shall condition the scrambler and the descrambler in accordance with § 6.1.1.

b) In accordance with Recommendation V.25, after the detection of the 2100 Hz tone and a silent period of 75 ± 20 ms, the modem shall apply an ON condition to circuit 107.

6.3.1.1.2 *Answer mode modem*

a) On connection to line it shall condition the scrambler and the descrambler in accordance with § 6.1.1.

b) In accordance with Recommendation V.25, the modem is silent during 2.15 ± 0.35 seconds, sends a 2100 ± 15 Hz tone for 3.3 ± 0.7 seconds, and then remains silent for 75 ± 20 ms.

c) In accordance with Recommendation V.25, after the silent period, it shall apply an ON condition to circuit 107.

6.3.1.2 *Sequence B (data bit rate selection sequence)*

The call and the answer mode modems are conditioned to transmit and receive at 1200 bit/s in a half-duplex mode.

6.3.1.2.1 *Call mode modem*

a) The modem waits until it detects at least 4 consecutive error free octets of the rate pattern (see Note 1).

The calling modem selects the maximum rate compatible with the answering modem or the maximum rate it can transmit.

b) Then, it remains silent during 250 ± 5 ms.

c) After that it transmits the synchronization sequence followed by 256 bits of a rate pattern corresponding to the selected bit rate in accordance with § 6.1.3.

d) Then, it applies the appropriate condition to circuit 112 (if used).

6.3.1.2.2 *Answer mode modem*

a) The modem transmits the receiver synchronization signals defined in § 2.7 followed by 256 bits of the rate pattern which indicates the set of rates available for the answering modem in accordance with § 6.2.

b) The modem remains silent until it detects at least 4 consecutive error-free octets of a rate pattern.

If a rate pattern is not detected within 2 seconds following the end of the rate pattern transmitted by the answering modem, it shall resume the operating sequence at the beginning of sequence B.

If the rate pattern indicates a rate not available, the modem shall disconnect from the line.

If the rate pattern indicates a rate available, the modem applies the appropriate condition to circuit 112 (if used).

c) Then, it remains silent again during 250 ± 5 ms.

d) In accordance with Recommendation G.164, the modem transmits a 2100 ± 15 Hz tone for 500 ± 50 ms to disable echo suppressors, then remains silent for 75 ± 20 ms.

6.3.1.3 *Sequence C (echo cancelling procedure)*

The call and the answer mode modems are conditioned to transmit, to receive and to cancel the echo at the selected data bit rate.

6.3.1.3.1 *Call mode modem*

a) The modem remains silent until 64 consecutive received scrambled binary 0s are detected. The modem shall then transmit the echo cancellation sequence (see Notes 2 and 3) until a sufficient degree of echo cancellation is available locally.

b) At the end of this sequence the modem shall be silent during 25 ± 3 ms and then transmit the receiver synchronization signals followed by scrambled binary 0s.

c) After detection of scrambled binary 0s, refinement of echo cancellation and detection of consecutive received scrambled binary 0s (Note 4) during a period of 64 bits, the calling modem shall apply the ON condition to circuit 109 and transmit scrambled binary 1s during a fixed period of 128 bits.

d) Then, the circuit 106 is enabled to respond to the condition of circuit 105 (see Notes 5 and 6).

6.3.1.3.2 *Answer mode modem*

a) The modem transmits the echo cancellation sequence (see Note 2) until a sufficient degree of echo cancellation is available locally (see Note 3).

b) After this sequence, the modem is silent during 25 ± 3 ms and then transmits the receiver synchronization signals followed by scrambled binary 0s.

c) After detection of a signal transmitted by the calling modem during a period of 50 ± 5 ms, the answering modem remains silent.

d) After detection of 64 consecutive received scrambled binary 0s, the modem transmits the' receiver synchronization signals followed by scrambled binary 0s.

e) After refinement of echo cancellation and the detection of a further 64 consecutive scrambled binary 0s whilst operating in duplex mode, the modem transmits scrambled binary 1s.

f) After detection of 64 consecutive received scrambled binary 1s the modem applies an ON condition on circuit 109 and enables circuit 106 to respond to the condition of circuit 105 (see Notes 5 and 6).

Note 1 - If 4 consecutive error-free octets of the rate pattern are not detected the modem remains silent.

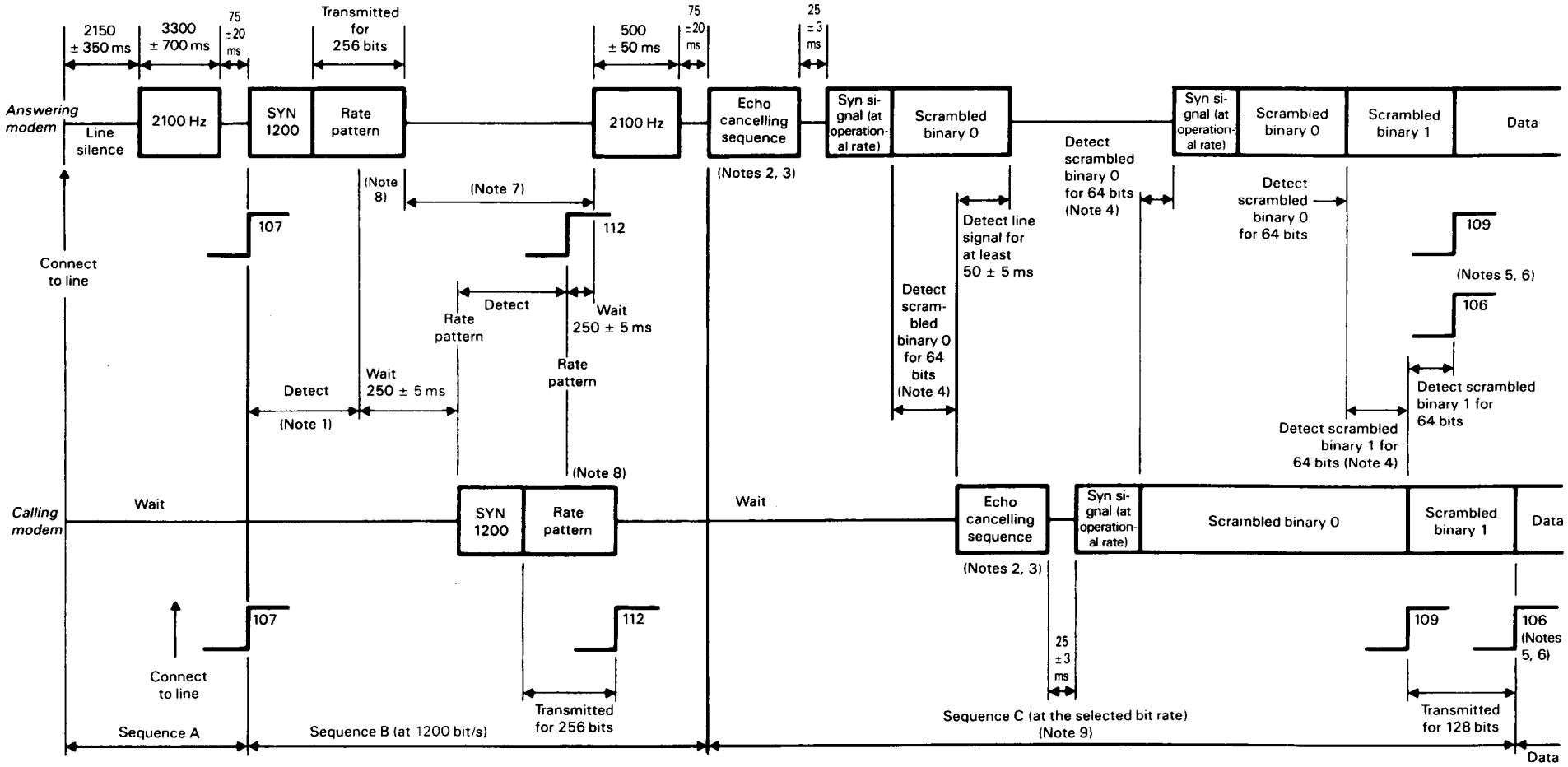
Note 2 - The echo cancellation sequence must not contain more than 32 consecutive unscrambled or scrambled binary 0s.

Note 3 - Manufacturers are cautioned that the time duration of the echo cancellation sequence has to be at least 650 ms when operating with network echo cancellers in accordance with Recommendation G.165.

Note 4 - The detection of scrambled binary 1s or 0s should start only after the receiver synchronization signals are completed.

Note 5 - When circuit 106 is. in the OFF condition, circuit 103 shall be changed to the binary 1 condition.

Note 6 - Users may wish to note that if in the DTE a time-out exists between the ON conditions of circuit 107 and circuit 106, this time-out shall be greater than 15 seconds.



Notes 1 to 6 - See Notes 1 to 6 of § 6.3.

Note 7 - If 4 consecutive octets of rate pattern are not detected within 2 seconds, the modem resumes sequence B.

Note 8 - Rate pattern is defined in § 6.1.3.

Note 9 - Sequence C is defined for operation at 2400 bit/s and 1200 bit/s and is under study for the higher bit rate of 4800 bit/s.

FIGURE 1/V.26 *ter*

Operating sequences

7 Half-duplex mode of operation

This mode of operation is optional.

7.1 *Synchronizing signals*

The synchronizing signals for both data signalling rates are divided into segments.

7.1.1 *Segment 1*

The composition of segment 1 is continuous 180° phase reversals for 32 symbol intervals without protection against talker echo or for 256 symbol intervals with protection against talker echo.

7.1.2 *Segment 2*

As defined in § 2.7.2.

7.2 *Response times of circuits 106 and 109*

See Table 8/V.26 *ter*.

TABLE 8/V.26 *ter*

Response times				
Circuit 106	With protection against talker echo		Without protection against talker echo	
	2400 bit/s	1200 bit/s	2400 bit/s	1200 bit/s
OFF to ON	240 ± 10 ms	267 ± 10ms	55 ± 2 ms	82 ± 2 ms
ON to OFF	≤ 2 ms			
Circuit 109 OFF to ON	See § 7.2.1			
ON to OFF	5 to 15 ms			

7.2.1 *Circuit 109*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104. Circuit 109 is prevented from turning ON during reception of unmodulated carrier when the optional protection against talker echo is used.

7.2.2 *Circuit 106*

Circuit 106 response times are from the connection of an ON or OFF condition on:

- circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106; or

- circuit 107 (where circuit 105 is already ON) to the appearance of the corresponding ON or OFF condition on circuit 106 as defined in the operating sequence in § 7.4.

7.3 *Clamping of circuits 104 and 109*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations.

7.4 *Operating sequence*

The means of achieving automatic bit rate selection, and synchronism between the call mode and the answer mode modems on international GSTN connections and leased lines are shown in Figure 2/V.26 *ter.*

The operating sequence is divided in two sequences, A and B_l.

The sequence A is the answering sequence according to Recommendation V.25 defined in § 6.3.1.1 above.

The sequence B_l is the data bit rate selection sequence operated at 1200 bit/s.

At the end of these two sequences, the modem may now transmit or receive data.

7.4.1 *Description of sequence B_1*

During the sequence B_1 circuits 106 and 109 are clamped to the OFF condition.

The call and the answer mode modems are conditioned to transmit and receive at 1200 bit/s in a half-duplex mode.

7.4.1.1 *Call mode modems*

a) The modem waits until it detects at least 4 consecutive error-free octets of the rate pattern (see Note 1, Figure 2/V.26 *ter).* The calling modem selects the maximum rate compatible with the answering modem or the maximum rate it can transmit.

b) Then, it remains silent during 250 ± 5 ms.

c) After that it transmits the synchronization sequence defined in § 7.1 followed by 256 bits of a rate pattern corresponding to the selected bit rate in accordance with § 6.1.3 (see Note 1, Figure 2/V.26 *ter).*

d) Then, it applies the appropriate condition to circuit 112 (if used).

e) The modem remains silent during 250 ± 5 ms, and then it enables circuit 106 to respond to circuit 105 and circuit 109 to operate as defined in § 7.2.1.

7.4.1.2 *Answer mode modem*

a) The modem transmits the receiver synchronization signals defined in § 7.1 followed by 256 bit of the rate pattern which indicates the set of rates available for the answering modem in accordance with § 6.1.3.

b) The modem remains silent until it detects at least 4 consecutive error-free octets of a rate pattern.

If a rate pattern is not detected within 2 seconds following the end of the rate pattern transmitted by the answering modem, it shall resume the operating sequence at the beginning of sequence B_1.

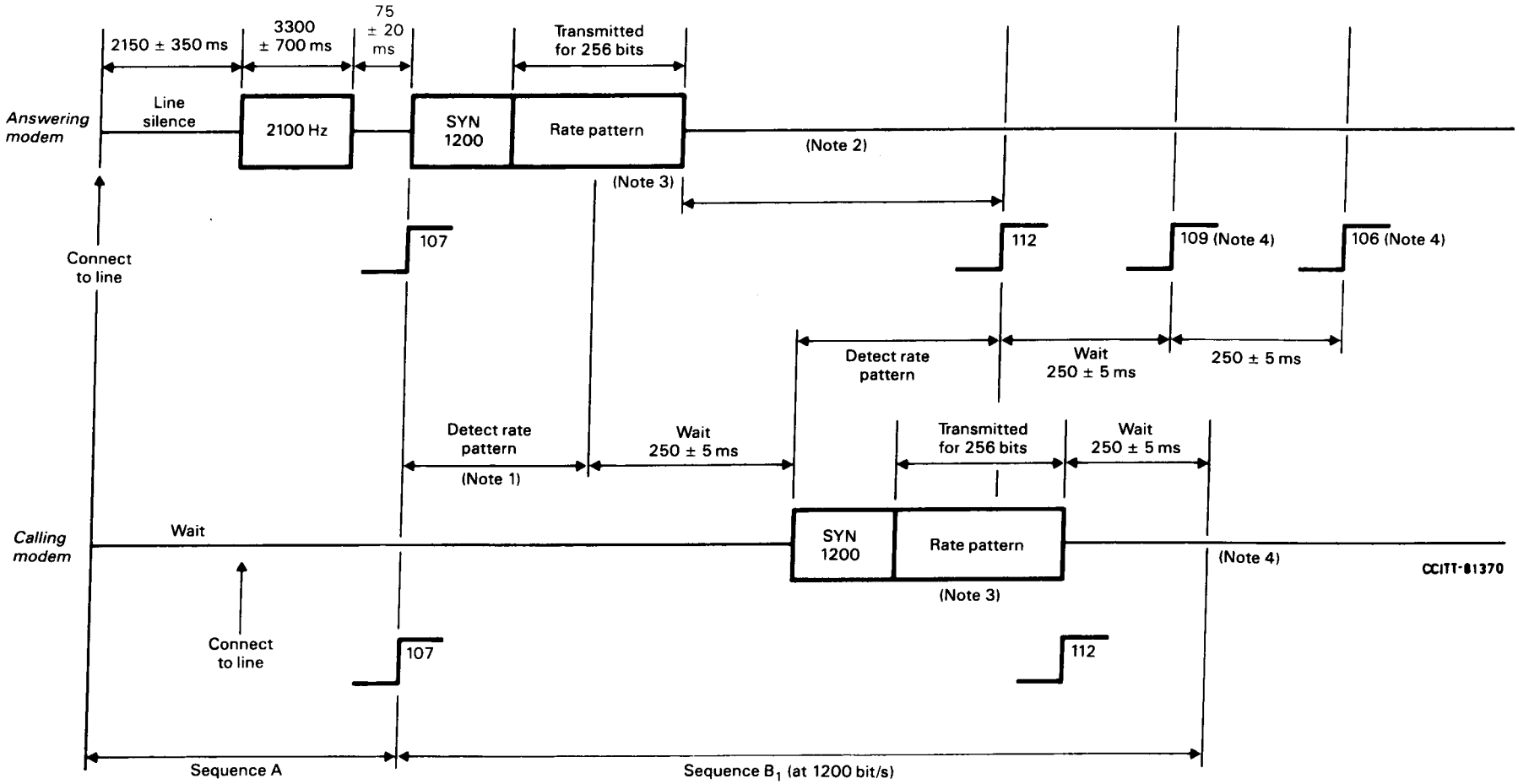
If the rate pattern indicates a rate not available, the modem shall disconnect from the line.

if the rate pattern indicates a rate available, the modem applies the appropriate condition to circuit 112 (if used).

c) Then, it remains silent again during 250 ± 5 ms.

d) After the silent period the modem enables circuit 109 to operate as defined in § 7.2.1.

e) The modem waits 250 ± 5 ms prior to enabling circuit 106 to respond to circuit 105.



Note 1 - If 4 consecutive error free octets of the rate pattern are not detected the modem remains silent.

Note 2 - If 4 consecutive error free octets of the rate pattern are not detected within 2 seconds the modem resumes sequence B_1.

Note 3 - Rate pattern is defined in § 6.1.2.

Note 4 - The condition of circuit 106 shall respond to circuit 105, and the circuit 109 shall operate as defined in § 7.2.1.

FIGURE 2/V.26 *ter*

Operating sequences in half-duplex mode

8 Testing facilities

Test loops 2 and 3 as defined in Recommendation V.54 shall be provided. Interface operation shall be as defined in Recommendation V.54.

8.1 *Remote loop 2*

Instigation and termination of remote loop 2 shall be in accordance with Recommendation V.54.

APPENDIX I

(to Recommendation V.26 *ter)*

Detailed scrambling and descrambling process

I.1 *Scrambling*

The message polynomial is divided by the generating polynomial GPC = $1 + x^{-18} + x^{-23}$ or GPA = $1 + x^{-5} + x^{-23}$ (see Figure I-1/V.26 *ter* and I-2/V.26 *ter* respectively), according to the transmission direction. The coefficients of the quotient of this division taken in descending order from the data sequence D_s to be transmitted. The expression of this sequence is:

$D_s = D_i \oplus D_s\, x^{-18} \oplus D_s\, x^{-23}$, when the generating polynomial GPC is used;

$D_s = D_i \oplus D_s\, x^{-5} \oplus D_s\, x^{-23}$, when GPA is used.

D_i is the data sequence applied to the scrambler.

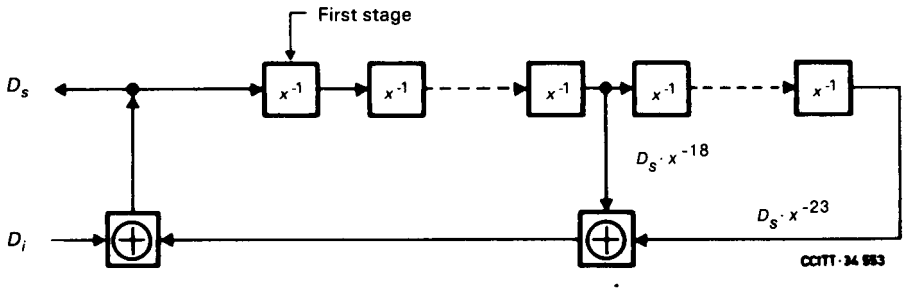


FIGURE I-1/V.26 *ter*

Scrambler with GPC generating polynomial

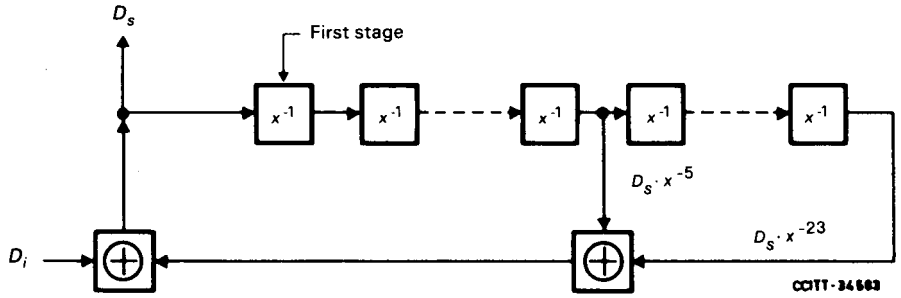


FIGURE I-2/V.26 *ter*

Scrambler with GPA generating polynomial

1.2 *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial GPC or GPA (see Figures I-3/V.26 *ter* and I-4/V.26 *ter* respectively) to form the recovered message polynomial. The coefficients of the recovered polynomial taken in descending order form the output data sequence D_o with the expression:

$$D_o = D_s (1 \oplus x^{-8} \oplus x^{-23}) \text{ for the GPC polynomial}$$

or

$$D_o = D_s (1 \oplus x^{-5} \oplus x^{-23}) \text{ for the GPA polynomial.}$$

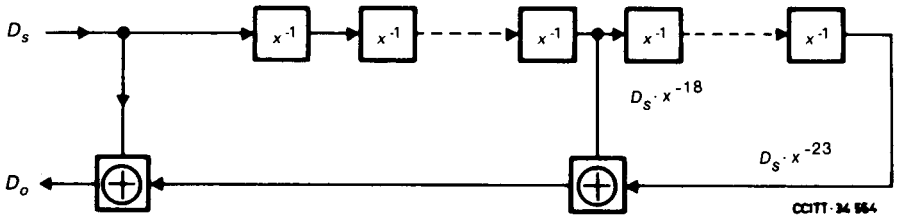


FIGURE 1-3/V.26 *ter*

Descrambler with GPC polynomial

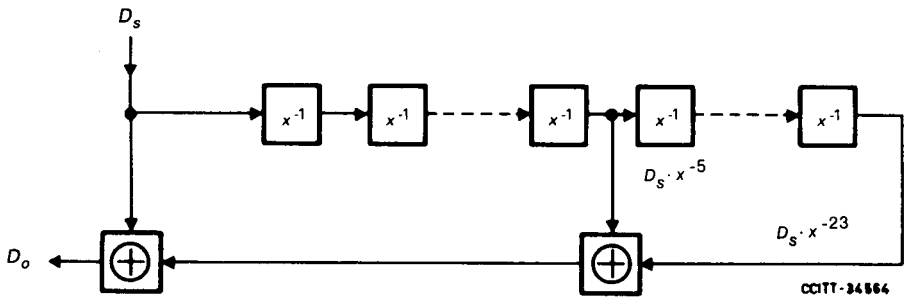


FIGURE I-4/V.26 *ter*

Descrambler with GPA polynomial

Note - The scrambler output patterns required to produce the synchronizing signal segment are as follows for both data rates:

GPC: 00 11 11 11 11 00 00 00 00 11 11 10 01 11 00 00 01 11 00

↑ First bit

GPA: 00 11 11 11 11 00 00 00 00 11 11 10 01 11 00 11 11 10 00

↑ First bit

Scrambler contents immediately preceding the output pattern above are as follows:

GPC: 10 01 11 11 11 11 11 11 00 00 01 1

↑

GPA: 01 10 00 00 11 10 00 00 11 10 00 0

First stage of scrambler ↑