INTERNATIONAL TELECOMMUNICATION UNION

ITU-T Q.274

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

SPECIFICATIONS OF SIGNALLING SYSTEM No. 6

SIGNALLING LINK

TRANSMISSION METHODS
MODEM AND INTERFACE REQUIREMENTS

ITU-T Recommendation Q.274

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation Q.274 was published in Fascicle VI.3 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

6.3 TRANSMISSION METHODS

6.3.1 *Analogue modulation methods*

The modulation technique described in this Recommendation uses *phase shift keying* to transmit serial binary data over analogue telephone channels. The binary data signal is encoded by first grouping it into bit pairs (dibits). Each dibit is represented by one of four possible carrier phase shifts. Thus, the output from the phase modulator consists of a serial train of phase-shifted carrier pulses at half the data bit rate. The phase shift between two consecutive modulation elements contains the information to be transmitted.

The data receiver uses differentially coherent detection to recover the sense of the binary data from the line signal. This type of detection has proven to be relatively insensitive to the types of distortions and interference encountered on telephone-type transmission media. It also allows rapid recovery from such catastrophic impairments as dropouts and large phase hits.

Receiver timing recovery can be accomplished in several ways. A very rapid timing recovery scheme can be provided using certain properties of the transmitted spectrum.

Receiver timing information can also be extracted from the zero crossings, on a dibit basis, of the received baseband data signals. The latter method is capable of providing synchronization holdover through extended drop-outs and periods of high noise.

6.3.2 *Digital transmission methods*

The methods used to derive the 4 and 56 kbit/s digital channels from the 1544 and 2048 kbit/s primary multiplexes are described below.

6.3.2.1 *Derivation from the 1544 kbit/s primary multiplex*

The binary data from the signalling terminal is transferred serially at the data transmission rate of 4 kbit/s to the 1544 kbit/s primary multiplex. At the primary multiplex each bit of the data stream is successively inserted into the S bit position (see Recommendation Q.47, § 4.1).

In the receive direction the primary multiplex extracts the bits from the S-bit position and transfers them serially to the signalling terminal.

6.3.2.2 *Derivation from the 2048 kbit/s primary multiplex*

a) *Data transmission at 4 kbit/s rate.* - The binary data from the signalling terminal is transferred serially to the digital interface adaptor. At the digital interface adaptor the 4 kbit/s data stream is modulated on a 64 kbit/s bearer channel such that 16 bits of the bearer channel correspond to one bit of the 4 kbit/s channel. The 64 kbit/s data stream is transferred serially to the 2048 kbit/s primary multiplex in alignment with an 8 kHz clock (byte timing). At the primary multiplex the 16 bits corresponding to one signalling information bit are inserted into the designated channel time slot of two successive frames.

In the receive direction the primary multiplex extracts the bits from the designated channel time slot and transfers them serially at 64 kbit/s in alignment with an 8 kHz clock to the digital interface adaptor. At the digital interface adaptor the 16 bits corresponding to one signalling information bit are detected and the binary data is transferred serially to the signalling terminal at the data transmission rate of 4 kbit/s.

b) *Data transmission at 56 kbit/s rate.* - The binary data from the signalling terminal is transferred serially to the digital interface adaptor. At the digital interface adaptor, the 28 bits of a signal unit are placed in bit positions 1 to 7 of four 8 bit bytes [see also § 6.4.2.4 c) below]. These four bytes are transferred serially at the data transmission rate of 64 kbit/s to the 2048 kbit/s primary multiplex in alignment with an 8 kHz clock (byte timing). At the primary multiplex, the four bytes are inserted into the designated channel time slot of four successive frames.

In the receive direction the primary multiplex extracts the bits from the designated channel time slot and transfers them serially at the data transmission rate of 64 kbit/s to the digital interface adaptor in alignment with an 8 kHz clock. In the digital interface adaptor the bits 1 to 7 of each 8 bit byte are transferred serially to the signalling terminal at the data transmission rate of 56 kbit/s.

6.4 MODEM AND INTERFACE REQUIREMENTS

6.4.1 *Analogue modem requirements*

The requirements for a 2400 bits per second modem are given below.

6.4.1.1 *Principal requirements*

The principal requirements of a modem used for System No. 6 are as follows:

a) Use of differential four-phase modulation (see Recommendation V.26, alternative B);

b) Use of differential coherent 4-phase demodulation;

c) Full duplex operation over a 4-wire data link;

d) A modulation rate of 1200 bauds;

e) A bit rate of 2400 bits per second.

6.4.1.2 *Frequency requirements*

a) The basic timing frequency shall be 2400 Hz (one cycle per bit);

b) The carrier frequency shall be 1800 Hz;

c) The carrier envelope frequency shall be 600 Hz (see § 6.4.1.4 below);

d) All frequencies generated in the modem shall be stable to within ± 0.005% of the nominal value. They must have a constant phase relationship with respect to one another. This implies that all frequencies should be derived from a basic clock or that they be phase-locked.

6.4.1.3 *Encoding phase relationships*

The encoding phase relationship must be as follows:

Dibit	Phase change
00	+ 45°
01	+ 135°
11	+ 225°
10	+ 315°

The phase change is the actual on-line phase shift in the transition region from the end of one signalling element to the beginning of the following signalling element.

6.4.1.4 *Line signal envelope*

The data carrier pulse shape can be closely approximated by the following expression for a signal element centred at $t = 0$ (see Figure 17/Q.274):

$$\text{Envelope } (t) = \frac{\cos \frac{2\pi f_d \cdot t}{2} - \cos \frac{2\pi f_d \cdot \frac{3}{4} T}{2}}{1 - \cos \frac{2\pi f_d \cdot \frac{3}{4} T}{2}}$$

$$\text{for } -\tfrac{3}{4} T \leqslant t \leqslant \tfrac{3}{4} T$$

$$\text{and} \quad \text{Envelope } (t) = 0 \text{ for } -T \leqslant t \leqslant -\tfrac{3}{4} T \text{ and } \tfrac{3}{4} T \leqslant t \leqslant T$$

where f_d = the dibit rate of 1200 Hz,

and T = the dibit period of 1/1200 s.

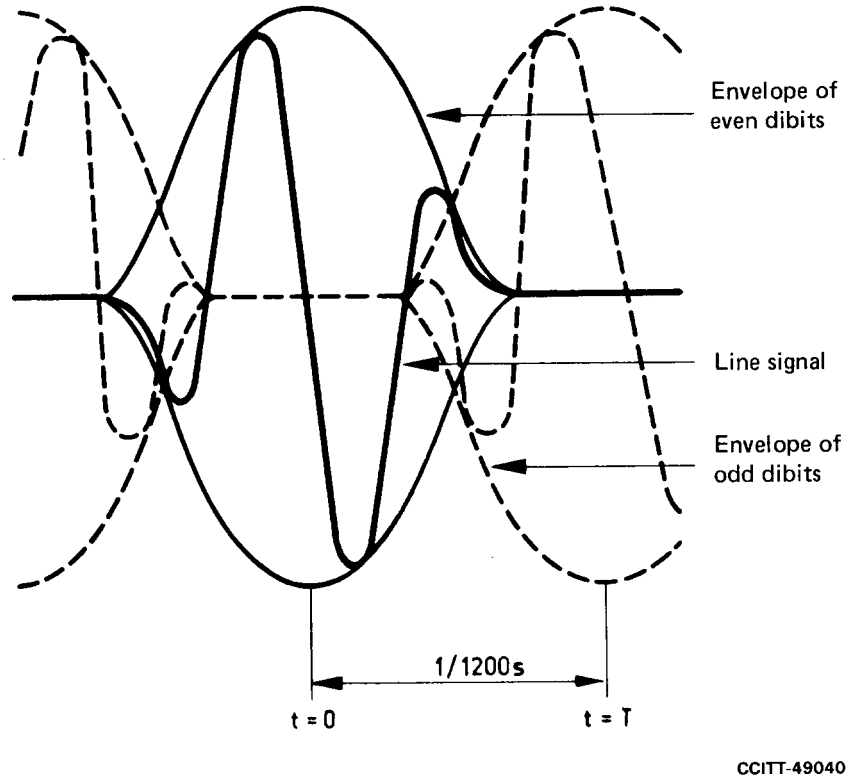

FIGURE 17/Q.274
Composite line signal

6.4.1.5 *Line power spectrum*

The line power spectrum produced by the transmission of random data is shown in Figure 18/Q.274. The spectral lines produced by the transmission of repeated dibits (using the encoding phase relationship of § 6.4.1.3 above) are also shown.

6.4.1.6 *Transmitter requirements*

a) The transmitter output level shall be -15 ± 1 dBm0 (see also Recommendation Q.272, § 6.1.4).

b) In the data transmitter, the bit timing and carrier frequency are derived from the same source to facilitate receiver timing recovery.

6.4.1.7 *Receiver requirements*

a) The receiver sensitivity range shall be -15 ± 8 dBm0 [see § 6.4.1.6 above and Recommendation Q.272, § 6.1.3 b)].

b) The modem receiver shall be capable of establishing bit synchronization as fast as possible, but in any case within 150 milliseconds while receiving synchronization signal units.

c) The receiver shall maintain bit synchronization with the distant transmitter for at least 500 milliseconds during a loss of data carrier after initial bit synchronization has been established.

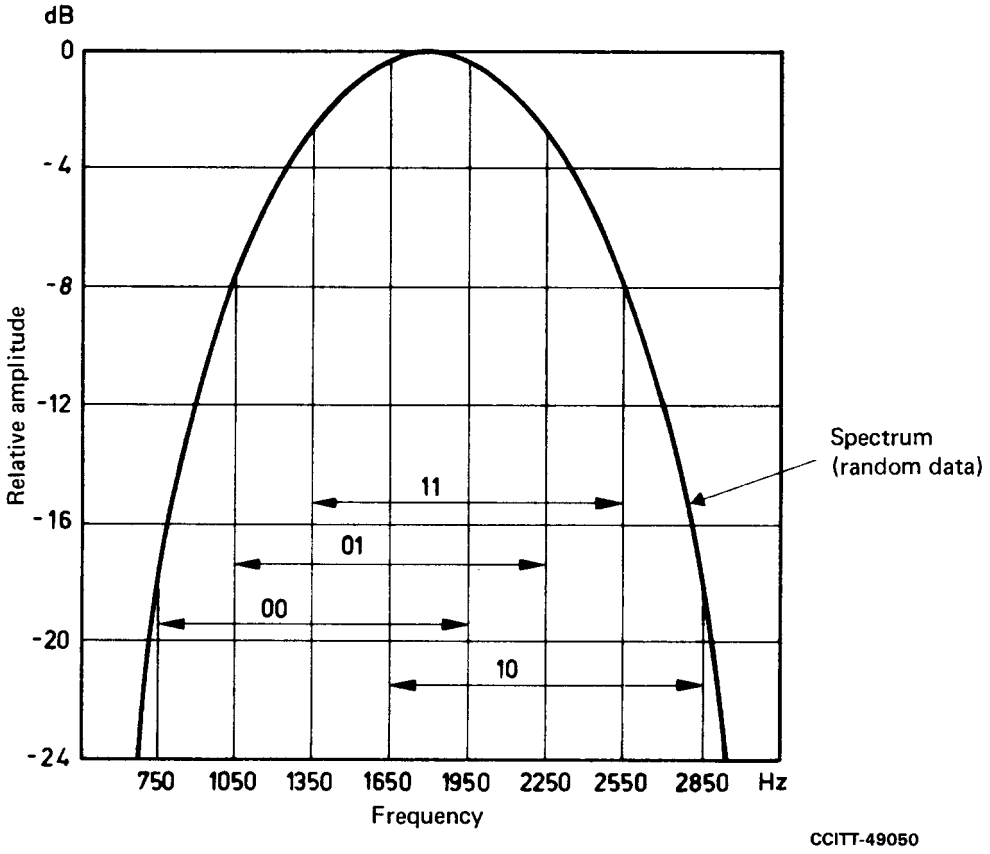

FIGURE 18/Q.274
Line power spectrum

6.4.1.8 *Interface requirements*[1)]

Each Administration may at its discretion integrate the modem into the signalling terminal equipment or use a separate modem. If the modem is a separate unit, then the interface requirements of Recommendations V.24/V.28 should be followed as far as possible. Alternatively the interface requirements of § 6.4.2.3 below may be followed.

The transmitting and receiving signalling terminals derive timing from the timing frequency of the modem transmitter and receiver respectively.

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1) The interface requirements for the digital version can be followed for the analogue version. This admits the use of a universal signalling terminal.

6.4.2 *Digital interface requirements*

6.4.2.1 *General*

a) The interface between the signalling terminal and primary multiplex equipment can be functionally represented as shown in Figures 19/Q.274, 20/Q.274 and 21/Q.274. See also Recommendation G.703.

b) The interface adaptor functions are rate conversion of data where required, rate and/or direction conversion of clocks where required, generation of a receive holdover clock and transfer of a loss of frame alignment indication.

c) The receive holdover clock must maintain bit synchronism for at least 500 ms during data channel failure at all data rates after initial bit synchronization has been established.

d) The transmit and receive clock signals shall be in phase with the respective data signals.

6.4.2.2 *Interface and adaptor requirements*

a) *The 4 kbit/s data transmission rate, 1544 kbit/s primary multiplex.* - The interface and adaptor functions for the 4 kbit/s data transmission rate over a 1544 kbit/s primary multiplex are shown in Figure 19/Q.274. The diagram is intended to show functions and should not be construed as depicting equipment.

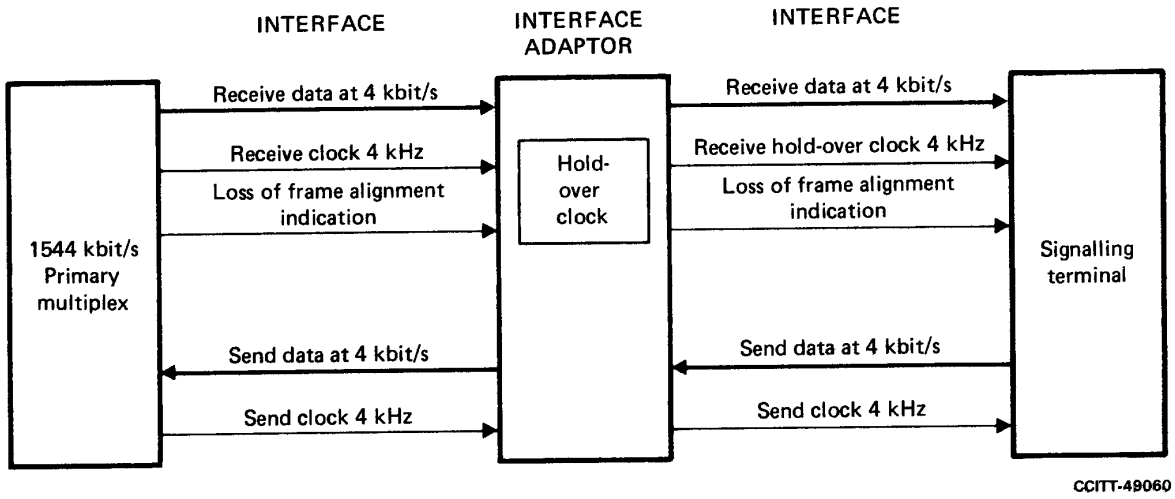

FIGURE 19/Q.274

Interface and adaptor functions, 4-kbit/s, 1544-kbit/s primary multiplex

The interface adaptor is transparent to the send and receive data and to a loss of frame alignment indication. Data channel failure is covered in § 6.5.

A holdover function on the 4 kHz receive clock to the signalling terminal is provided to maintain bit synchronism for a minimum interval during which the receive clock is not present.

b) *The 4 kbit/s data transmission rate, 2048 kbit/s primary multiplex.* - The interface and adaptor functions for the 4 kbit/s data transmission rate over a 2048 kbit/s primary multiplex are shown in Figure 20/Q.274. The diagram is intended to show functions and should not be construed as depicting equipment.

The receive-rate converter converts the receive data on the 64 kbit/s bearer channel to receive data at 4 kbit/s using the 8 kHz and 64 kHz receive clocks. The 4 kHz receive clock is derived in the receive clock converter.

The send rate converter converts the send data at 4 kbit/s to send data on the 64 kbit/s digital bearer channel using the 8 kHz and 64 kHz send clocks. The 4 kHz send clock is derived in the send clock converter. [2)]

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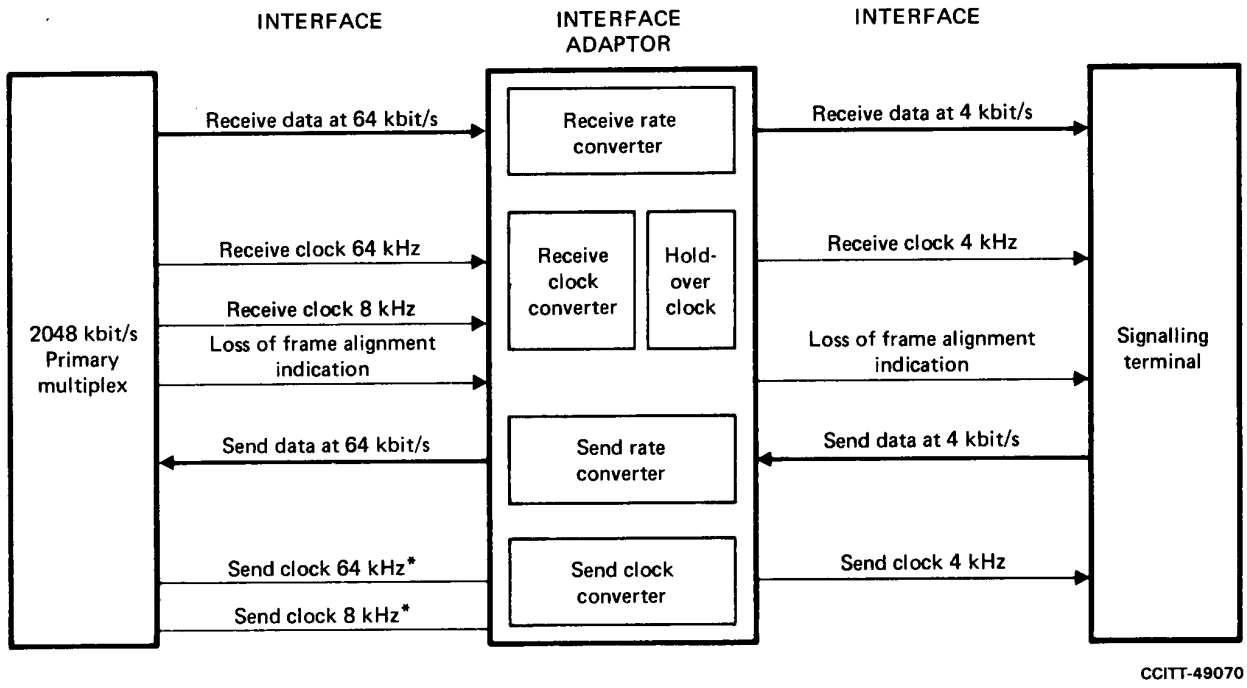
2) This material is subject to revision pending results of further work by Study Group XVIII.

The interface adaptor is transparent to a loss of frame alignment information. A holdover function on the 4 kHz receive clock to the signalling terminal is provided to maintain bit synchronism for a minimum interval during which the receive clock is not present. Data channel failure is covered in § 6.5 below.

c) *The 56 kbit/s data transmission rate, 2048 kbit/s primary multiplex.* - The interface and adaptor functions for the 56 kbit/s data transmission rate over a 2048 kbit/s primary multiplex are shown in Figure 21/Q.274. The diagram is intended to show functions and should not be construed as depicting equipment.



*The direction of the 64 kHz and 8 kHz clocks between the 2048 kbit/s primary multiplex and interface adaptor in Figures 20/Q.274 and 21/Q.274 are dependent on whether a codirectional or contra-directional interface is used.

FIGURE 20/Q.274

Interface and adaptor functions, 4 kbit/s, 2048 kbit/s primary multiplex

The interface adaptor is transparent to the send and receive data and to a loss of frame alignment indication. Data channel failure is covered in § 6.5 below.[3)]

The send data at 56 and 64 kbit/s is aligned with the 8 kHz send clock. Similarly, the receive data is aligned with the 8 kHz receive clock.

A holdover function on the receive clock to the signalling terminal is provided to maintain bit synchronism for a minimum interval during which the receive clock is not present.

6.4.2.3 *Interface electrical requirements*[3)]

Interface electrical requirements are given in Recommendation G.732 and Recommendation G.733, for the interface between the primary multiplex and the interface adaptor. Arrangements for the interface between the interface adaptor and the signalling terminal are left to the discretion of Administrations.

Each Administration may at its discretion integrate the interface adaptor into the signalling terminal or the primary multiplex equipment or may use a separate interface adaptor. If the interface adaptor is a separate unit then the interface electrical requirements above must be met. If it is integrated into either the signalling terminal equipment or the multiplex equipment the remaining interface must meet the interface electrical requirements.

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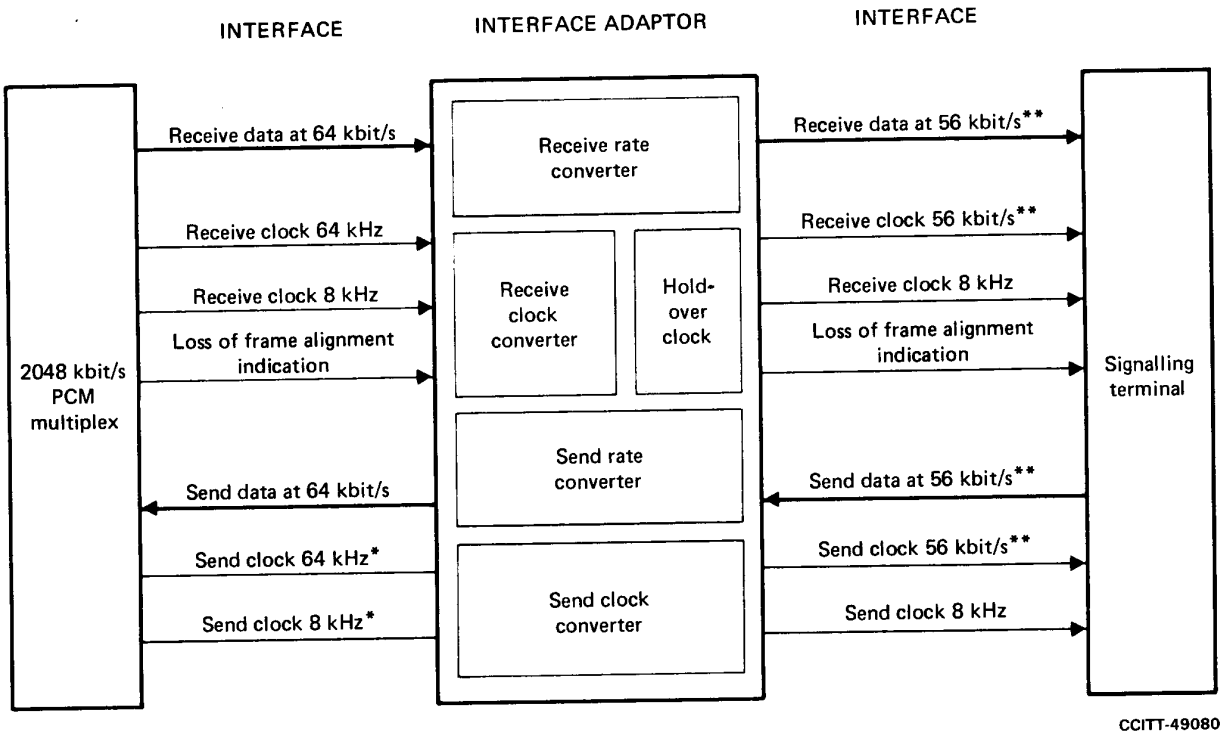
3) This material is subject to revision pending results of further work by Study Group XVIII.



*The direction of the 64 kHz and 8 kHz clocks between the 2048 kbit/s primary multiplex and interface adaptor in Figures 20/Q.274 and 21/Q.274 are dependent on whether a codirectional or contra-directional interface is used.

** The nature of the 56 kbit/s data and the 56 kbit/s clocks between the interface adaptor and the signalling terminal is left to the discretion of each Administration. The clocks may be at 56 kHz with the data arriving at a smooth rate or the clocks may be at 64 kHz with every eighth bit deleted and the seven data bits occuring at a 64 kbit/s rate with every eighth bit discarded.

FIGURE 21/Q.274

Interface and adaptor functions, 56-kbit/s, 2048-kbit/s primary multiplex

6.

4.2.4 *Interface adaptor electrical requirements*

a) *The 1544 kbit/s primary multiplex, 4 kbit/s channel*

The send and receive data and the send clock signals traverse the interface adaptor without modification.

The receive clock and the data channel failure information are separated in the interface adaptor. The receive clock from the primary multiplex synchronizes the receive holdover clock. The holdover clock provides the receive clock to the signalling terminal. The interface adaptor recognizes data channel failure by the absence of the receive clock from the primary multiplex. This information is separately transferred to the signalling terminal.

The receive holdover clock should:

- maintain bit synchronism for at least 500 ms after initial bit synchronism is established, and
- have a tolerance of ± 70 parts per million when the receive clock is not present.

b) *The 2048 kbit/s primary multiplex, 4 kbit/s channel*

Each bit of the 4 kbit/s data is represented by two channel-time-slots in the transmitted 64 kbit/s stream. These sixteen bits are encoded by the send-rate converter according to Table 4/Q.274. The 8 bit bytes are aligned with the 8 kHz clock.

TABLE 4/Q.274

4-kbit/s channel encoding for 2048 kbit/s primary multiplex

Binary figure	Bit position	Encoded transmission	
1	odd	**00111100**	**00111100**
1	even	**11000011**	**11000011**
0	odd	**01100110**	**01100110**
0	even	**10011001**	**10011001**

Transmission of the data in this form makes it possible to detect and correct for single, channel-time-slot slip avoiding the loss of signalling data. This is achieved in the receiver-rate converter as follows. The 64 kbit/s data stream is collected into 8 bit bytes using the 8 kHz clock, and each byte is decoded. The reception of three consecutive bytes of the same code indicates that channel-time-slot duplication has occurred, and that a half cycle delay must be introduced into the 4 kHz receive clock, whereas reception of a single byte with a given code followed by a byte with a code signifying a different bit position, indicates that omission of a channel-time-slot has occurred and that the 4 kHz clock must be advanced by half a cycle.

The send clock at 4 kHz is derived directly from the 64 kHz and 8 kHz send clocks. The 4 kHz receive clock is derived from the 64 kHz and 8 kHz receive clocks, but it must be adjustable to take account of channel-time-slot slip detected in the receive rate converter. The receive holdover clock provides the receive clock to the signalling terminal. The interface adaptor recognizes loss of frame alignment by the absence of the 8 kHz clock from the primary multiplex or by an indication transmitted from the primary multiplex over a separate connection. [4)] This information is separately transferred to the signalling terminal.

The receive holdover clock should:

- maintain bit synchronism for at least 500 ms after initial bit synchronism is established, and
- have a tolerance of ± 70 parts per million when the receive clocks are not present.

c) *The 2048 kbit/s primary multiplex, 56 kbit/s channel*

The send and receive data and the send clock signals traverse the interface adaptor without modification.[4)]

The 28 bits of a signal unit are represented by bit positions 1 to 7 of four consecutive channel time slots in the 64 kbit/s stream transmitted from or received at the interface adaptor. Bit position 8 of consecutive octets is coded **0**, **0**, **1**, **1**, **0**, **0**, **1**, **1**, ...in a continuing sequence. This pattern is not suitable for direct transmission to the 1544 kbit/s multiplex.[4)]

The receive holdover clock should:

- maintain channel-time-slot synchronism for at least 500 ms after initial synchronism is established, and
- have a tolerance of ± 50 parts per million when the receive clocks are not present.

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4) This material is subject to revision pending results of further work by Study Group XVIII.