INTERNATIONAL TELECOMMUNICATION UNION

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

I.741

(06/99)

SERIES I: INTEGRATED SERVICES DIGITAL NETWORK

B-ISDN equipment aspects – Transport functions

Interworking and interconnection between ATM and switched telephone networks for the transmission of speech, voiceband data and audio signals

ITU-T Recommendation I.741

(Previously CCITT Recommendation)

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ITU-T RECOMMENDATION I.741

INTERWORKING AND INTERCONNECTION BETWEEN ATM AND SWITCHED TELEPHONE NETWORKS FOR THE TRANSMISSION OF SPEECH, VOICEBAND DATA AND AUDIO SIGNALS

Summary

This Recommendation provides requirements for the interworking and interconnection functions between public ATM and other types of public switched telephone networks (including wireless networks) for the transmission of speech, voiceband data and audio signals. The functions include: interfaces of TDM to ATM networks, TDM to ATM conversion, transport, multiplexing, switching and echo cancellation.

Source

ITU-T Recommendation I.741 was prepared by ITU-T Study Group 15 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 22nd of June 1999.

FOREWORD

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INTERWORKING AND INTERCONNECTION BETWEEN ATM AND SWITCHED TELEPHONE NETWORKS FOR THE TRANSMISSION OF SPEECH, VOICEBAND DATA AND AUDIO SIGNALS

(Geneva, 1999)

1 Scope

The scope of this Recommendation is to provide requirements for the interworking and interconnection functions between public ATM and other types of public switched telephone networks (including wireless networks) for the transmission of speech, voice band data and audio signals. The functions include: interfaces of TDM to ATM networks, TDM to ATM conversion, transport, multiplexing, switching and echo cancellation.

2 References

The following Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision: all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

– ITU-T Recommendation G.114 (1996), *One-way transmission time*.

– ITU-T Recommendation G.131 (1996), *Control of talker echo*.

– ITU-T Recommendation G.165 (1993), *Echo cancellers*.

– ITU-T Recommendation G.168 (1997), *Digital network echo cancellers*.

– ITU-T Recommendation G.176 (1997), *Planning guidelines for the integration of ATM technology into networks supporting voiceband services*.

– ITU-T Recommendation G.703 (1998), *Physical/electrical characteristics of hierarchical digital interfaces*.

– ITU-T Recommendation G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels*.

– CCITT Recommendation G.706 (1991), *Frame alignment and cyclic redundancy check (CRC) procedures relating to basic frame structures defined in Recommendation G.704*.

– ITU-T Recommendation G.707 (1996), *Network node interface for the synchronous digital hierarchy (SDH)*.

– CCITT Recommendation G.711 (1988), *Pulse code modulation (PCM) of voice frequencies*.

– CCITT Recommendation G.726 (1990), *40, 32, 24, 16 kbit/s adaptive differential pulse code modulation (ADPCM)*.

– CCITT Recommendation G.727 (1990), *5-, 4-, 3-, and 2-bits/sample embedded adaptive differential pulse code modulation (ADPCM)*.

– CCITT Recommendation G.728 (1992), *Coding of speech at 16 kbit/s using low-delay code excited linear prediction*.

– ITU-T Recommendation G.729 (1996), Coding of speech at 8 kbit/s using Conjugate-Structure Algebraic-Code-Excited Linear-Prediction (CS-ACELP).

– CCITT Recommendation G.732 (1988), *Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s*.

– CCITT Recommendation G.751 (1988), *Digital multiplex equipments operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification*.

– ITU-T Recommendation G.763 (1998) *Digital circuit multiplication equipment using ADPCM (Recommendation G.726) and digital speech interpolation*.

– ITU-T Recommendation G.766 (1996) *Facsimile demodulation/remodulation for digital circuit multiplication equipment.*

– ITU-T Recommendation G.804 (1998), *ATM cell mapping into plesiochronous digital hierarchy (PDH)*.

– ITU-T Recommendation G.823 (1993), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

– ITU-T Recommendation G.824 (1993), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.

– ITU-T Recommendation G.832 (1998), *Transport of SDH elements on PDH networks: Frame and multiplexing structures*.

– ITU-T Recommendation G.957 (1995), *Optical interfaces for equipments and systems relating to the synchronous digital hierarchy*.

– ITU-T Recommendation I.356 (1996), *B-ISDN ATM layer cell transfer performance*.

– ITU-T Recommendation I.361 (1999), *B-ISDN ATM layer specification*.

– ITU-T Recommendation I.363.1 (1996), *B-ISDN ATM Adaptation Layer specification*: *Type 1 AAL*.

– ITU-T Recommendation I.363.2 (1997), *B-ISDN ATM Adaptation layer specification*: *Type 2 AAL*.

– ITU-T Recommendation I.363.3 (1996), *B-ISDN ATM Adaptation Layer specification*: *Type 3/4 AAL*.

– ITU-T Recommendation I.363.5 (1996), *B-ISDN ATM Adaptation Layer specification*: *Type 5 AAL*.

– ITU-T Recommendation I.371 (1996), *Traffic control and congestion control in B-ISDN*.

– ITU-T Recommendation I.580 (1995), *General arrangements for interworking between B-ISDN and 64 kbit/s based ISDN*.

– ITU-T Recommendation I.610 (1999), *B-ISDN operation and maintenance principles and functions*.

– ITU-T Recommendation I.751 (1996), *Asynchronous transfer mode management of the network element view*.

– ITU-T Recommendation Q.50 (1997), *Signalling between circuit multiplication equipments (CME) and international switching centres (ISC)*.

– ITU-T Recommendation Q.115 (1997), *Logic for the control of echo control devices*.

– ITU-T Recommendation Q.2660 (1995), *Interworking between Signalling System No. 7 – Broadband ISDN User Part (B-ISUP) and Narrow-band ISDN User Part (N-ISUP)*.

3 Abbreviations

This Recommendation uses the following abbreviations:

AAL	ATM Adaptation Layer
AAL CS	AAL Convergence Sublayer
ACR	Adaptive Clock Recovery
ADPCM	Adaptive Differential Pulse Code Modulation
ATM	Asynchronous Transfer Mode
B-ISDN	Broadband-ISDN
B-ISUP	Broadband-ISUP
CDV	Cell Delay Variation
CLP	Cell Loss Priority
CLR	Cell Loss Rate
CRC	Cyclic Redundancy Check
CS-ACELP	Conjugate-Structure Algebraic-Code Excited Linear Prediction
DBR	Deterministic Bit Rate
DCME	Digital Circuit Multiplication Equipment
FDM	Frequency Division Multiplex
GFC	Generic Flow Control
HEC	Header Error Control
ISDN	Integrated Services Digital Network
ISUP	ISDN User Part
IWF	Interworking Function
LD-CELP	Low-Delay Code Excited Linear Prediction
MTE	Mobile Terminal Equipment
N-ISDN	Narrowband-ISDN
N-ISUP	Narrowband-ISUP
OAM	Operation and Maintenance
PCM	Pulse Code Modulation
PRC	Primary Reference Clock
PSTN	Public Switched Telecommunication Network
PTI	Payload Type Information
QoS	Quality of Service
SN	Sequence Number
SRTS	Synchronous Residual Time Stamp
TDM	Time Division Multiplex
TE	Terminal Equipment
VCI	Virtual Channel Identifier

VCLAD Voice Cell Assembly and Disassembly

VPI Virtual Path Identifier

4 Terms and definitions

This Recommendation defines the following terms:

4.1 ATM island: An ATM island is a self-contained telecommunication infrastructure segment where access is provided exclusively by ATM interfaces. Traffic outside an ATM island is typically transported by the PSTN.

4.2 Interconnection: This is the configuration when two like-network (e.g. ATM) islands are linked through a different network (e.g. PSTN) using a permanent circuit between them. Interconnection also covers the connection of two non-ATM networks (e.g. PSTN/N-ISDN or mobile) through an ATM backbone. Examples of various ATM-PSTN/N-ISDN and ATM/Mobile Network scenarios are shown in clause 6.

4.3 Interworking: This is the configuration when an ATM network and another type of network (e.g. PSTN or mobile) are linked through the necessary functions to convert from one network format to the other and vice versa. These functions may include the mapping and demapping of voiceband signals and signalling conversion.

5 Generic configuration of PSTN/N-ISDN/ATM interworking/interconnection

Figure 5-1 shows the generic interworking and interconnection of the circuit-switched (PSTN/ISDN) and cell-switched (ATM) networks.

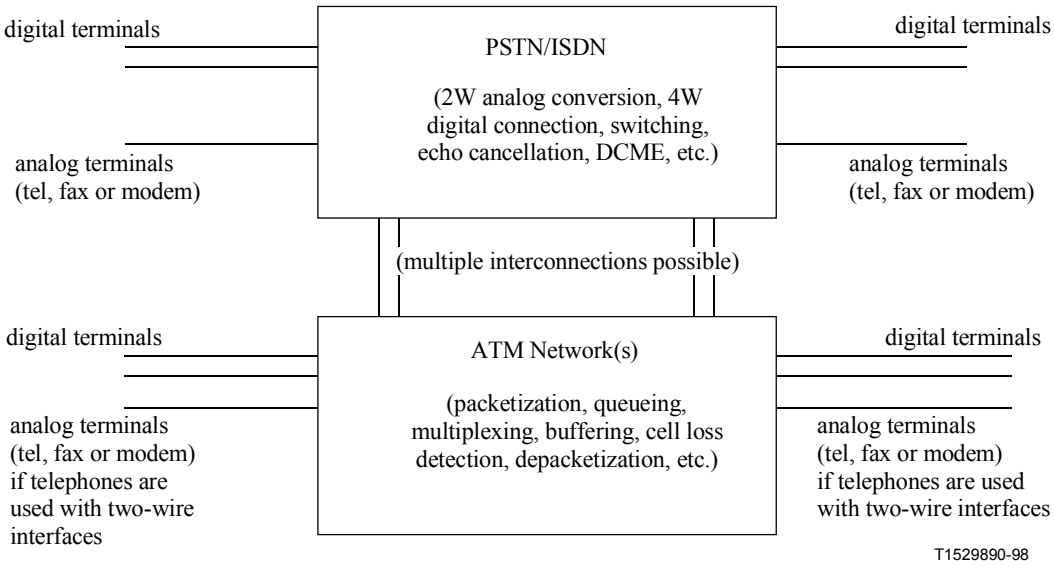


Figure 5-1/I.741 – Generic configuration for PSTN/N-ISDN-ATM interworking and interconnection

NOTE – A single call may traverse several circuit and cell networks. This will be further defined in the next clauses.

6 Examples of networking scenarios

Below are examples of networking scenarios that include both interworking and interconnection. In these examples and unless there is a bilateral agreement to do otherwise, the interface between the ATM and the PSTN/N-ISDN is through G.711 compliant primary multiplex signals that are transported across the boundary between the two networks. Special interface requirements between an ATM network and PSTN/N-ISDN-based DCME are described in Annex A.

The following scenarios are considered:

1) Reference PSTN/N-ISDN;
2) Reference ATM;
3) ATM-PSTN/N-ISDN;
4) PSTN/N-ISDN-ATM-PSTN/N-ISDN;
5) Mobile-ATM-Mobile.

6.1 Interworking and interconnection

The general arrangements for the interworking between B-ISDN and 64-kbit/s-based (narrow-band) ISDN have been specified in I.580. Recommendation I.580 gives an overview of five basic communication scenarios for N-ISDN services in B-ISDN and N-ISDN.

In these scenarios, interworking functions are performed by an "IWF". Such an IWF may be either a separate device with physical interfaces to the narrow-band network and B-ISDN network (ATM network) or it may be integrated in ATM equipment such as ATM network nodes. The basic functionality is illustrated in Figure 6-1.

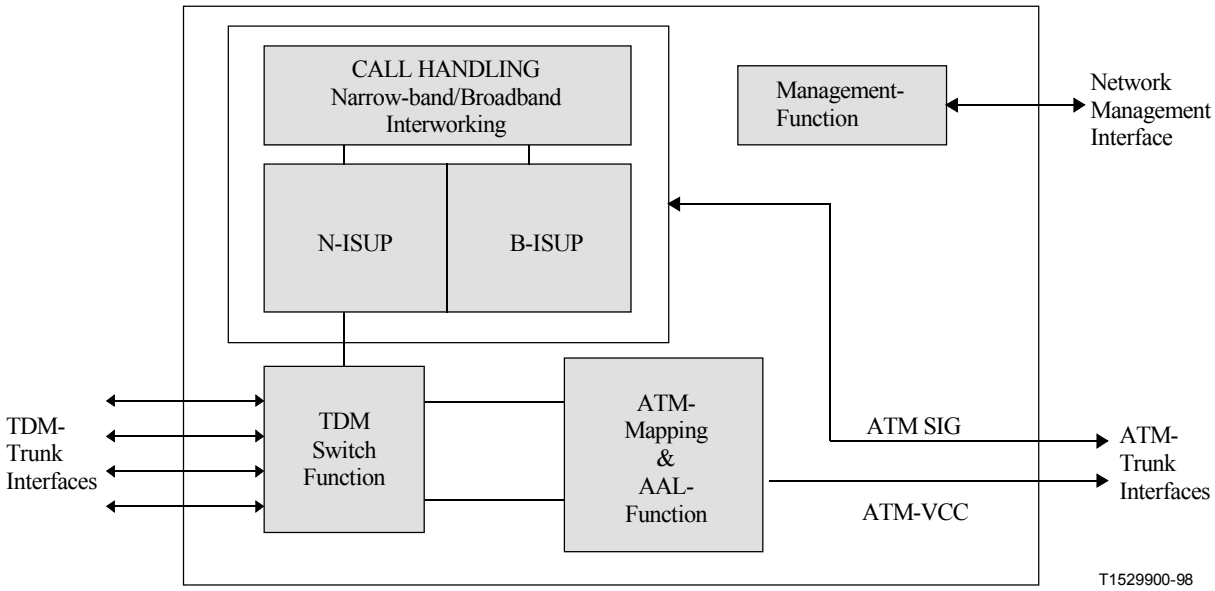


Figure 6-1/I.741 – Functionality of the IWF

6.2 Scenario 1: Reference PSTN/N-ISDN

The reference scenario of an all-PSTN/N-ISDN connection between two PSTN/N-ISDN-based Terminal Equipment (TE) points is shown in Figure 6-2. The likely speech encodings algorithms in this purely PSTN/N-ISDN-based network would be:

– G.711 PCM;

– G.726, G.727 ADPCM;

– G.728 LD-CELP;

– G.729 CS-ACELP.

Figure 6-2/I.741 – Reference PSTN/N-ISDN scenario

6.3 Scenario 2: Reference ATM

The standard all-ATM scenario between two ATM-Based Terminal Equipment (TE) points is shown in Figure 6-3. The packet assembly and disassembly strategy for low rate voice and voiceband signals is described in 6.4.3 and 7.

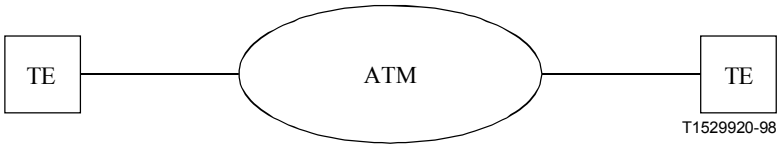


Figure 6-3/I.741 – Reference ATM scenario

6.4 Scenario 3: ATM-PSTN interconnection and interworking

The interface between the PSTN/N-ISDN and ATM island shown in Figure 6-4 and will be through an Interworking Function (IWF) having the functionality and interfaces described below.

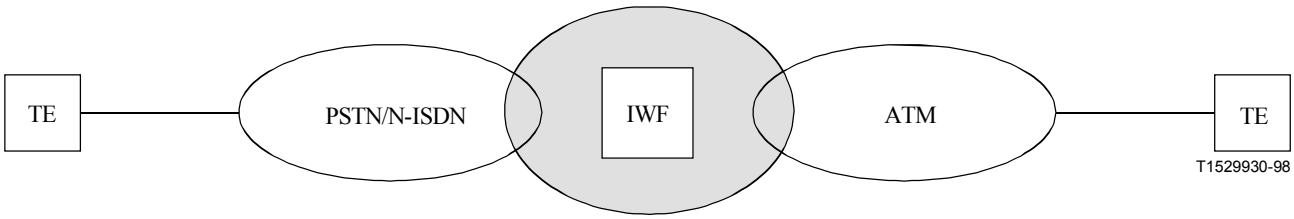


Figure 6-4/I.741 – ATM-PSTN/N-ISDN interworking scenario

The physical and logical aspects of the PSTN/N-ISDN-ATM Interworking Function (IWF) as well as specific performance limits are as follows:

6.4.1 Physical interfaces

The physical interface between the PSTN/N-ISDN and the IWF can be any TDM interfaces defined in Recommendations G.703, G.704, G.751, G.707 and G.957.

The physical interface between the IWF and the ATM network can be any ATM interfaces defined in Recommendations G.703, G.704, G.707, G.957, G.804, G.832 and I.432.1-I.432.5.

6.4.2 Service-related criterias

6.4.2.1 Framing

For further study.

6.4.2.2 Synchronization

In common with the ideas in Appendix I "Timing issues related to echo cancellation in ATM networks", it should be noted that there are three main methods for synchronization in B-ISDN/ATM networks, these being:

- Network Synchronous Operation;
- Synchronous Residual Time Stamp (SRTS);
- Adaptive Clock Recovery (ACR).

6.4.2.2.1 Network-synchronous operation

This is the recommended method when traffic streams must be merged and when interworking with PSTN/N-ISDN. It is also the recommended method when a network clock is available at the IWF and the service user does not require timing transparency. If network synchronous operation is used, it is required that the CBR service timing is synchronous with the network clock.

The effects of CDV can be completely eliminated by forcing an end-station to operate in synchronism with the network clock. Given the presence of a network clock at both the transmitting and receiving end-stations, the service bit stream can simply be clocked out of the playout buffer at the service bit rate, fully independent of the cell delay variations caused by the ATM network. A playout buffer with correct dimensions and initial delay in playout is still required to ensure that CDV does not cause cell loss or padding bits to be required. In the event of network clock failure the buffer will require a buffer slip algorithm with the receive clock placed in a hold-over mode. The use of adaptive clocking algorithm is for further study.

6.4.2.2.2 Synchronous residual time stamping

This is the recommended method when frequency transparency is required through an ATM network. It is also suitable for limiting the wander caused by CDV.

With SRTS when using AAL type 1 (see 6.4.3), the number of derived network clock cycles in N cycles of the service clock is counted in a p-bit counter and this p-bit SRTS value is transmitted across the network to the receiving network terminating point. At the receiving terminal the local service clock can be adjusted against the reference network clock to ensure that the same number of derived network clock cycles are counted over the same N cycles of the local service clock, thus locking the local service clock to the transmitter service clock by use of the received residual time stamps and the reference network clock.

6.4.2.2.3 Adaptive clock recovery

This method is recommended when frequency transparency through ATM network is required and there are no strong requirements on wander at the service interfaces. There are several ways of implementing the adaptive method (ACR), leading to different performances.

When ATM cells pass through a number of different ATM networks, it may not be possible to provide a common network clock to the transmitting and receiving end-stations. Also, some services may not require the purity of clock available from the network synchronous or SRTS schemes. In these instances it may only be possible or more cost-effective to use an adaptive clock-recovery technique.

In general, adaptive clock recovery relies on the fact that, irrespective of the amount of delay variation experienced in the network, the DBR cell stream has an underlying average inter-arrival time. The job of any adaptive clock recovery mechanism is to extract this longer term average inter-arrival time from the "noise" produced by both the CDV and cell loss, and uses this as a basis for received service clock derivation.

The data buffer acts as a phase comparator of the incoming cell stream and outgoing cell stream – the buffer fill level being the output of the phase comparison. Since on cell arrival the service bits are delivered in bulk by the ATM payload the buffer fill varies in a "saw-tooth" fashion.

If the receiving clock is too slow compared to the transmitter the average buffer level will rise with time. This trend, once detected, can be used to increase the receive clock frequency to bring the buffer level back to a nominal value and lock-in the receiving clock to that of the transmitter. The converse is true when the receiving clock is too fast compared to the transmitter and the average buffer level falls with time. In this case the receive clock frequency will be decreased to bring the buffer level back to a nominal value.

A full description of these timing recovery methods is outside the scope of this Recommendation. The choice of timing recovery method used will affect the amount of phase noise experienced on a connection which may subsequently affect the performance of any echo cancellers seeing this in their echo tail. Network synchronous and SRTS clock recovery methods produce the least amount of phase noise and also isolate the connection from the effects of CDV. It is therefore recommended that either of these two methods are used.

Adaptive clock recovery techniques have the potential to produce phase noise which may impact on the performance of echo cancellers. The use of adaptive clock recovery as a timing recovery mechanism is therefore for further study.

6.4.2.2.4 Modes of operation

There are two modes of operation for timing information to be transported between service interfaces.

- Synchronous – Timing information given to the service interfaces is directly traceable to a PRC.
- Asynchronous – Timing information is generated by a user's clocking source which is independent of the ATM and/or GSTN network reference source. The user's timing information is transported between connected devices either via the ATM network through the use of SRTS or ACR, or independently of the ATM network.

6.4.2.3 Jitter and wander

Jitter measured at the output of the IWF Service Interface and tolerated at the input of the IWF Service Interface shall meet G.823 and G.824.

In network synchronous operation or SRTS, the jitter and wander requirements of G.823 and G.824 apply.

If ACR is used, the service must tolerate a certain amount of wander. The requirements are to be defined by the specific service interface.

6.4.2.4 Alarms

The OAM (operation and maintenance) functions and consequent actions are defined in Recommendation G.706, G.707, G.732, G.804, I.432.1-5 and I.610.

For some services ATM and PSTN/N-ISDN alarm information is terminated at the IWF. The handling of failures and defects from the PSTN/N-ISDN network to the ATM/Broadband side and vice versa is for further study. F4- and F5-Flows (as specified in I.610) are terminated at the IWF as "Connection Termination Point" in accordance with I.751.

6.4.2.5 Signalling

For switched connections, scenario 1 requires both mapping of the user information and mapping between the signalling protocols of B-ISDN and N-ISDN. The interworking between the ISDN User Part (ISUP) of N-ISDN and the B-ISDN User Part (B-ISUP) of B-ISDN at the NNI can be found in Q.2660. This Recommendation shows the mapping/interworking between B-ISUP and N-ISUP for the basic call and supplement services. If the capabilities of the capability-sets e.g. Point-to-Multipoint should be used the application of the corresponding recommendations are necessary.

6.4.2.6 Delay

The delay of voice band connections in ATM-networks can be calculated as follows:

Total end-to-end delay = Voiceband signal coding delay + cell assembly delay + propagation delay*) + cell delay variation + cell disassembly delay + voiceband signal decoding delay

*) The propagation delay consists of the transmission delay resulting from the length of a connection and equipment such as switches, cross connects, line equipments etc.

For the routing of voice connections the maximum delay requirements of G.114 should be met. The total delay caused by multiple transitions between PSTN/N-ISDN and ATM/B-ISDN should be compatible with this requirement.

The following delay effects occur in ATM networks.

6.4.2.6.1 Cell assembly and disassembly delay

Conversion of 64-kbit/s-connections into ATM cells at the IWF introduces a cell assembly delay. For example a 47-octet information field filled with 64-kbit/s-speech-samples causes a cell assembly delay of 5.875 ms. In order to minimize the delay introduced by cell assembly the method of "partially filled ATM cells" (see 6.4.3) can be used.

6.4.2.6.2 Cell transfer delay and cell delay variation

For the definition and requirements for cell transfer delay and cell delay variation see subclause 6.5/I.356 and Table 2/I.356. The definition of 2-point cell delay variation is used.

6.4.2.6.3 Cell delay variation

When PSTN/N-ISDN-based voiceband signals such as voice, voiceband data or facsimile traverse an ATM network the end-to-end delay through the composite network should ideally remain constant. However, since the ATM/B-ISDN network is cell-based and cells experience delay variation across the network, special attention must be given to minimizing the cumulative end-to-end delay. Cell delay variation is caused by ATM switches, queues in line equipment used for medium access and queues within receivers for adaptation of cell-rates. Eliminating cell delay variation depends upon correctly scheduling the playout time for each cell. To keep the delay constant, the IWF will include

a buffer. The size of this buffer depends on specifications provided in Recommendation I.356 and should be large enough to accommodate expected CDV.

6.4.3 AAL requirements

The term AAL is used in ATM/B-ISDN for the layer between ATM and the higher layers. Four AAL types have been identified and defined in I.363.1. For voice communication, a major function of the AAL is to convert speech, voiceband data and audio signals into ATM cells and vice versa.

6.4.3.1 Simplified AAL type 1

For transport of a single voiceband signal, i.e. one 64 kbit/s A-Law or μ-Law coded Recommendation. G.711 signal, it has been agreed that the AAL for voice is a simplified AAL type 1 described in I.363.1 which provides for a circuit transport that preserves the service timing with the basic AAL type 1 functions. Methods to achieve this are SRTS and ACR. Structured data transfer pointers or forward error correction methods are not used.

6.4.3.1.1 Cell fill

For simplified AAL Type 1 signals, 100% cell fill is used.

6.4.3.1.2 Cell coding

The arrangement of the channels/samples within the cell is for further study.

6.4.3.1.3 Bit ordering

The arrangement of the bits within the bytes is for further study.

6.4.3.2 Other AAL types

Use of AAL Type 1 (i.e. not the simplified Type 1) and AAL type 2 (I.363.2) are for further study.

6.4.3.2.1 Cell fill

The strategy of 100% cell fill, from the same PCM channel, can provide several advantages like simpler and more efficient use of ATM, the possibility of using existing cell loss detection mechanisms, and minimization of the effort required to study new cell sequencing algorithms. Nevertheless, organizations wishing to provide partially filled cell strategy are free to do so. For example the assembly delay will be halved by filling only 24 octets of the 48 octet cell information field. The wastage of bandwidth in this case may be tolerable but partly filling cells would require extra information to be exchanged indicating how much of a cell has been filled e.g. with structured data transfer pointers.

6.4.3.2.2 Cell coding

The arrangement of the channels/samples within the cell is for further study.

6.4.3.2.3 Bit ordering

The arrangement of the bits within the bytes is for further study.

6.4.4 Lost and misinserted cells

6.4.4.1 Cell loss

The receiving AAL entity must detect/compensate for lost cell events to maintain bit count integrity and must also minimize the delay, i.e. to alleviate echo performance problems, in conveying the individual voiceband signal octets from the SAR-PDU payload to the AAL user. The receiving AAL entity may take actions based on the received SN values, but such actions must not increase the

conveyance delay across the AAL receiving entity beyond the nominal CDV value to alleviate echo performance problems.

The AAL receiving entity must accommodate a sudden increase or decrease in the nominal cell transfer delay. (Such a change in cell transfer delay can be the result of a protection switching event in the network.)

The cell loss attribute in an IWF represents a count of the number of lost cells. This count records the number of cells detected as lost in the network prior to the destination interworking function AAL layer processing.

6.4.4.2 Cell misinsertion

In accordance with 2.5.1.3/I.363.1 there is no need to detect misinserted cells for voiceband signals. If implemented in an IWF the cell misinsertion attribute represents a count of sequence violation events which the AAL CS interprets as misinserted of cells.

6.4.4.3 Buffer-underflows

The buffer-underflow attribute in an IWF represents a count of the number of times the reassembly buffer underflows.

6.4.4.4 Buffer-overflows

The buffer-overflow attribute in an IWF represents a count of the number of times the reassembly buffer overflows.

6.4.5 Echo control

If speech channels are carried in ATM cells and the end-to-end delay exceeds that specified in G.131, echo control measures such as echo cancellers are required (see also 8.1). If telephones are used with two-wire interfaces there are two solutions for the location of the echo canceller in scenario 3.

- One echo canceller is placed at the IWF and the other close to the CPE (Customer Premises Equipment).

  Both echo cancellers can be inserted in the non-ATM-Domain (TDM-based Echo Canceller) or the ATM-Domain (ATM-based echo canceller are for further study). If on both sides there are no ATM portions the echo canceller function is less complex to implement.
- Echo cancellers located at the IWF.

  If both echo cancellers are located at the IWF each echo canceller can be inserted in the non-ATM-Domain (TDM-based Echo Canceller) or the ATM-Domain (ATM-based echo canceller are for further study). The echo cancellation function is in this case more complex because of ATM in the tail circuit. One impact can be a degradation in the quality of service if cell loss occurs.

NOTE – The impact of misinserted cells, cell loss and compensated cell loss in the echo path of an echo canceller in relation to the performance of an echo canceller, is for further study. Uncorrected cell delay variations in an echo canceller tail path can be interpreted by the canceller as time varying changes in the echo path and cause the echo canceller to continually reconverge.

6.4.6 Traffic parameters and tolerances

For further study.

6.4.7 Management and fault control

For further study.

6.5 Scenario 4: PSTN/N-ISDN-ATM-PSTN/N-ISDN interconnection and interworking

The end-to-end interconnection between the PSTN/N-ISDN and an ATM island (Figure 6-5) will be through a pair of Interworking Functions (IWFs) having the functionality and interfaces described below.

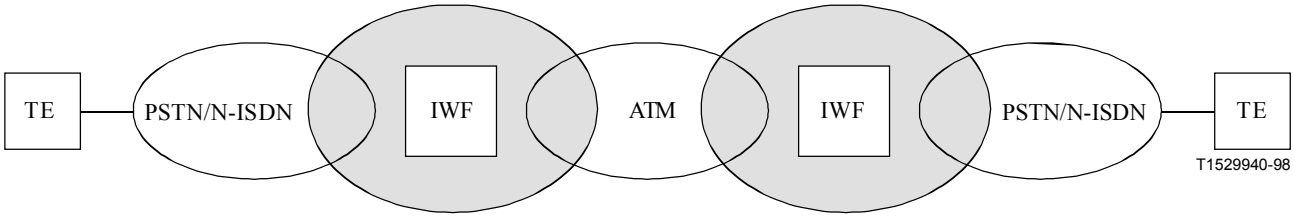


Figure 6-5/I.741 – PSTN/N-ISDN-ATM-PSTN/N-ISDN interconnection scenario

The physical and logical aspects of the PSTN/ATM Interworking Function (IWF) as well as specific performance limits are described below for an end-to-end connection between two PSTN/N-ISDN-based Terminal Equipment (TE) locations.

6.5.1 Physical interfaces

See 6.4.1.

6.5.2 Service-related criterias

6.5.2.1 Framing

For further study.

6.5.2.2 Synchronization

6.5.2.2.1 General points on synchronization

See 6.4.2.2, Synchronization.

6.5.2.2.2 Network interconnection

In this scenario the ATM network can be used simply to trunk voice services between narrow-band devices (e.g. PSTN/N-ISDN switches). The devices at either end can take network synchronization from the ATM network (Network Synchronous Operation) as recommended or have synchronization delivered to them via independent means. This could be achieved by providing additional connections to a public PSTN/N-ISDN network to provide timing to both ATM network connected devices.

6.5.2.3 Jitter and wander

See 6.4.2.3.

6.5.2.4 Alarms

See 6.4.2.4, Alarms.

6.5.2.5 Signalling

For this scenario, where B-ISDN/ATM is used as a backbone network for the transport of N-ISDN information, basically two realizations are possible:

- A transparent B-ISDN connection is used which emulates the PSTN/N-ISDN channels or accesses. For this case, only the protocol mapping of the user information is required. Mapping of signalling information is not needed. All PSTN/N-ISDN signalling information is transferred transparently through B-ISDN.
- For the second realization network interworking takes place. In this case, the interworking function provides for the mapping of the signalling and user information between PSTN/N-ISDN and B-ISDN. See 6.4.2.5.

6.5.2.6 Delay

See 6.4.2.6.

6.5.3 AAL requirements

See 6.4.3.

6.5.4 Lost and misinserted cells

See 6.4.4.

6.5.5 Echo control

If speech channels are carried in ATM cells and the end-to-end delay exceeds that specified in G.131, echo control measures such as echo cancellers are required (see also 8.1). For this scenario the echo cancellers at the IWF can be inserted in the non-ATM-Domain (TDM-based echo canceller) and the ATM-Domain (ATM-based echo canceller are for further study).

Multiple echo cancellers in the connection are for further study in this scenario.

NOTE – The impact of misinserted cells, cell loss and compensated cell loss in the echo path of an echo canceller in relation to the performance of an echo canceller, is for further study. Uncorrected cell delay variations in an echo canceller tail path can be interpreted by the canceller as time varying changes in the echo path and cause the echo canceller to continually reconverge.

6.5.6 Traffic parameters and tolerances

For further study.

6.5.7 Management and fault control

For further study.

6.6 Scenario 5: Mobile-ATM-Mobile interconnection and interworking

The end-to-end interconnection between the Mobile Network and an ATM island (Figure 6-6) will be through an Interworking Function (IWF) having the functionality and interfaces described below.

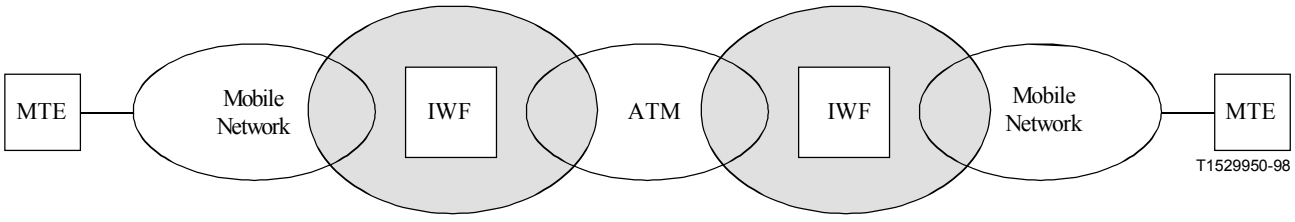


Figure 6-6/I.741 – Mobile-ATM-Mobile interconnection scenario

The physical and logical aspects of the Mobile Network/ATM Interworking Function (IWF) are described below for an end-to-end connection between two Mobile Terminal Equipment (MTE) locations.

6.6.1 Physical interfaces

See 6.4.1.

6.6.2 Service-related criterias

6.6.2.1 Framing

For further study.

6.6.2.2 Synchronization

6.6.2.2.1 General points on synchronization

See 6.4.2.2, Synchronization.

6.6.2.2.2 Network interconnection

For further study.

6.6.2.3 Jitter and wander

See 6.4.2.3.

6.6.2.4 Alarms

See 6.4.2.4.

6.6.2.5 Signalling

For this scenario, where B-ISDN/ATM is used as a backbone network for the transport of information from mobile networks, basically two realizations are possible:

- A transparent B-ISDN connection is used which emulates the mobile signalling channels or accesses. For this case, only the protocol mapping of the user information is required. Mapping of signalling information is not needed. All mobile signalling information is transferred transparently through the B-ISDN.
- For the second realization a network interworking takes place. In this case, the interworking function provides for the mapping of the signalling and user information between mobile networks and B-ISDN.

6.6.2.6 Delay

See 6.4.2.6.

6.6.3 AAL requirements

See 6.4.3.

6.6.4 Lost and misinserted cells

See 6.4.4.

6.6.5 Echo control

If speech channels are carried in ATM cells and the end-to-end delay exceeds that specified in G.131, echo control measures such as echo cancellers are required (see also 8.1). In this scenario the transmission is purely digital and therefore no electrical echo is produced. The control of acoustic echo is in the responsibility of the mobile network provider.

NOTE – The impact of misinserted cells, cell loss and compensated cell loss in the echo path of an echo canceller in relation to the performance of an echo canceller is for further study. Uncorrected cell delay variations in an echo canceller tail path can be interpreted by the canceller as time varying changes in the echo path and cause the echo canceller to continually reconverge.

6.6.6 Traffic parameters and tolerances

For further study.

6.6.7 Management and fault control

For further study.

7 Voiceband signals within the ATM networks

7.1 Cell fill

See 6.4.3.

7.2 Cell loss and recovery mechanism

Compensated cell loss results in a 5.875 ms segment of the transmitted signal being replaced by what is seen as a 6 ms interference burst at the receiving modem. The signal then continues with the same phase as before. The 5.875 ms of interference may be silent or filled with some kind of signal generated by the ATM receiver. Various possibilities exist for this fill including a repetition of the previous cell's contents or white noise at an amplitude that is fixed or equal to the average amplitude of the previous cell. It is believed that white noise will have the least disruptive effect on the modem, silence and last cell repeat being increasingly disturbing. For most modems it is unlikely that such a short interruption will cause the modem to retrain. The frequency of such events should be not greater than that of similarly disrupting events in existing networks. The actual effect on the application will depend on the protocol used. For some, the session will be terminated, for others, the effect will merely be a reduction in throughput.

Uncompensated cell loss will shorten the end-to-end delay by 6 ms (for full cells). This will cause a step change in the phase of the received signal together with a loss of optimality in the echo cancellation. The modem will almost certainly retrain, resulting in a loss of data for some 5-20 s. Such an event is clearly more disruptive than that of compensated loss. The frequency of occurrence should be significantly less than that of PCM timing slips.

For voice signals carried by G.711 and G.726/G.727 compliant signals, cells detected as lost do not need to be compensated because of the low probability of cell loss rate (CLR), which is guaranteed by the several QoS classes for voice. The adequacy of lost cell compensation mechanisms, such as cell repetition and interpolation is for further study.

7.3 Jitter

No figures for jitter tolerance are specified in the various modem Recommendations but modems are designed to give satisfactory performance over the PSTN/N-ISDN. ATM systems shall therefore be designed to perform no worse than existing transmission systems. In practice, it is believed that the complete transmission path will involve PCM and ATM segments and therefore any timing recovered from the ATM segment shall be constrained by what is acceptable to the PCM segment.

An effective technique to mask the jitter is by using build-out buffer to delay the playout of the packets/cells. The principle is to play the packets at regular intervals irrespective of the variation in the arrival times. This build-out delay can be set by the operator in accordance with I.356 to a value of between 300 µs and 3 ms in 100 µs steps. In any case, the value of the build-out delay depends on

the traffic mix as well as the characteristics of the links between the originating endpoint and the terminating endpoint.

7.4 Transcoding and gateway functions

When conveying voice across an ATM network it is likely that the A-law and μ-law coding schemes will be used extensively. The specification for AAL 1 contained in Recommendation I.363.1 identifies the need for A/μ-law conversion, but does not define the conversion function.

It is recommended that the conversion rules specified in Recommendation G.711 be used when conversion between A-law and μ-law is necessary. However, the place where the A-law/μ-law conversion is to take place is for further study.

8 Additional details of PSTN/ATM interworking

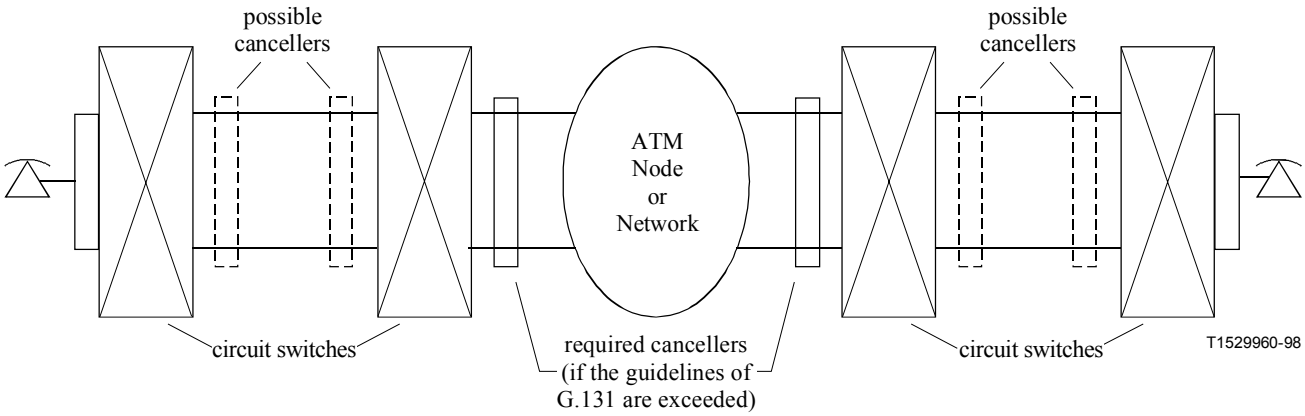


Figure 8-1/I.741 – Expanded detail of an PSTN/N-ISDN-ATM interworking example

8.1 Echo cancellation

Recommendation G.176 specifies guidelines for echo control for pure ATM network domains as well as for mixed PSTN/ATM networks. Echo control is responsibility of the ATM domain provider and should be provided at PSTN/ATM boundaries. Echo cancellation should be applied according to the rules of G.131 and maybe a function of the cell fill strategy deployed. All echo cancellers for use with ATM networks should generally meet the requirements in G.168. A general description of the applications of echo cancellers can be found in Appendix I/G.168 "Guidance for application of echo cancellers". In accordance with Q.115 "Logic for the control of echo control devices" signalling procedures and protocol carry information elements of echo control logic allows that echo cancellation may be placed in an exchange in either narrow-band or broadband network.

8.2 Congestion control and flow control

There may be a mismatch in capacity between the PSTN/N-ISDN and the ATM in terms of throughput. The regulation and bandwidth management can be used on the basis of Recommendation Q.50.

8.3 DCME/ATM interface consideration

There has been a significant effort in the past twenty-five years to develop circuit compression techniques for long-haul or bandwidth-limited voice speech interpolation. These include low-rate encoding techniques (32 and 16 kbit/s voice) as well as digital speech interpolation. Compression gains of 4 or 5 to one are typically realized in today's Digital Circuit Multiplication Equipment (DCME). DCME have been deployed extensively for international cable and satellite routes, and some carriers have found it economical to deploy such equipment in their national networks.

It has been relatively easy in the past to isolate those portions of the network that can economically benefit from additional signal processing and deploy special equipment there. This is because the voice and voiceband traffic is typically segregated from other traffic types, and because voice traffic can be easily detected and extracted from Time Division Multiplexing (TDM) circuits. This is not the case for ATM, where, for example, voice connections will be asynchronously multiplexed with hundreds or thousands of other connections on international routes. Stand-alone circuit multiplication equipment on bandwidth-limited routes will become much more challenging to design and deploy, for the following reasons:

– in order to achieve interpolation gains, current DCME are presented with bearers that the gateway switch has already filled with voice traffic. Service dependent routing is not a general design principal of ATM networks (for example, common routing requirements for connection groups may preclude separate routing by bearer type);

– on the other hand, if traffic types presented to the DCME are integrated, compression gains will be dependent on the mix of voice traffic with other traffic. The network operator, not knowing what amount of compression would be achievable, would need to plan for the worst case scenario: little or no compression. As a result, bandwidth saved by performing compression would end up being filled by idle cells anyway; and

– since ATM traffic is asynchronously multiplexed, circuit multiplication equipment would need access to ATM signalling to identify voice connections. It would need to extract and process voice connections, while leaving the QoS of other traffic (including cell delay variation) unchanged.

8.4 Interface to cellular networks

The interface of ATM networks to cellular networks depends on whether the link between the base station and the mobile switching centre is an ATM link. The main objective of this interface is to provide a bandwidth-efficient multiplexing scheme that would transport voiceband traffic. In this case, speech signals are arriving as low-bit rate compressed signals (bit rates of 16 kbit/s and lower).

There are two cases to be considered depending on whether the cellular transport is packet-based or is based on time division multiplexing.

• If the cellular traffic is in a packet mode, then the role of the interface is to provide a relaying function to reformat the packet so that the traffic can be transported on the ATM network. This avoids the delays due to packetization of the traffic and the potential degradation due to transcoding.

• If the cellular traffic is arriving in a time division multiplexed mode, the interface will provide the necessary packetization function. This function will introduce additional delays. In this case, there is a need to have echo cancellation function.

8.5 TDM/ATM compression interface

In this case the function of the interface at the originating endpoint is to provide speech detection, speech interpolation, speech encoding, multiplexing for the various functions, packetization (with partial or 100% cell fill) and echo cancellation. At the terminating endpoint, the function of the

interface is to provide for detection of cell loss, substituting for cell loss, masking the delay variations, speech decoding, comfort noise injection and demultiplexing.

ANNEX A

PSTN/N-ISDN-ATM interconnection using DCME

A.1 Background

Wide-area ATM networks will likely occur, at least in the early stages, by linking private local "islands" of ATM activity. As these private local islands develop, demand for wide area connectivity with other local ATM networks will grow. The voiceband signals that are flowing among the local ATM networks may include, for example, speech, voiceband modem traffic, and facsimile transmissions.

To achieve such wide area connectivity between separate local ATM networks an interworking function shall be added to existing DCME as shown in Figure A.1. The DCME provides the functions of speech detection and interpolation, speech compression, echo cancellation and packetization. With this new function, the DCMEs also act as gateways between the ATM networks and the PSTN/N-ISDN. The interworking function may be either externally to the DCME or incorporated in it.

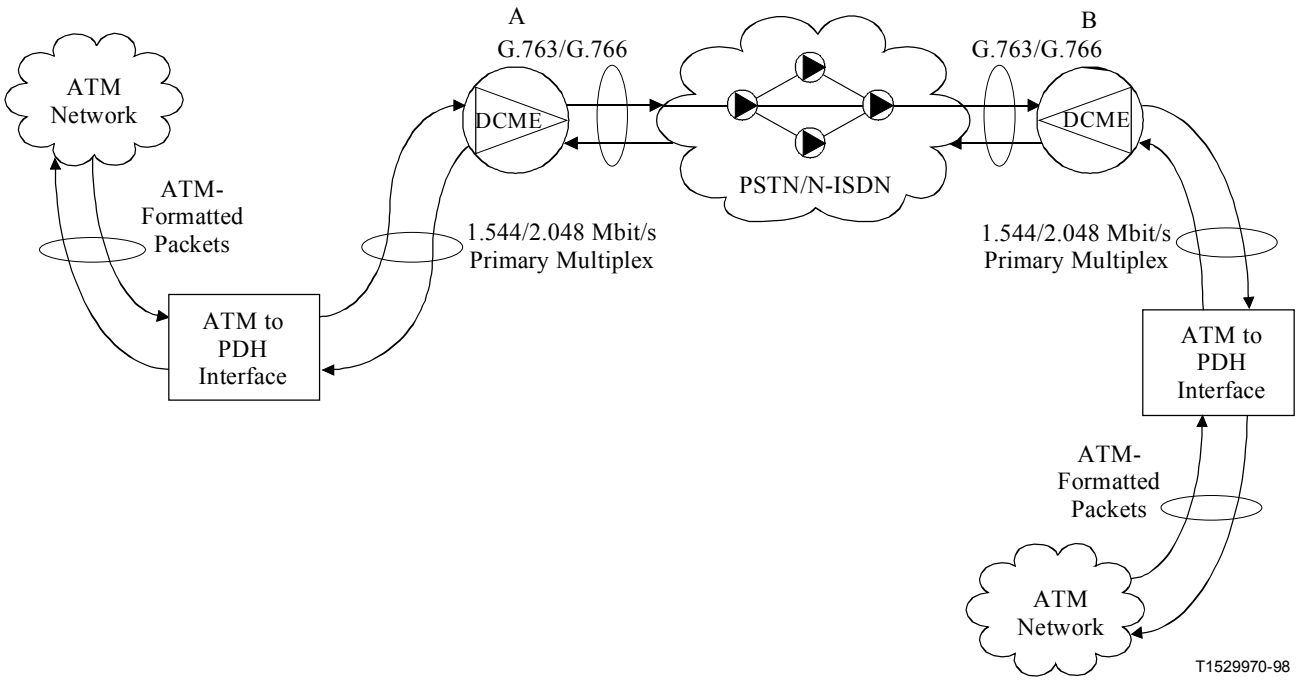


Figure A.1/I.741 – ATM-DCME interface

In this approach, there is no need to introduce a new AAL because all the necessary adjustments can occur at the DCME gateway. For example, congestion control, which is required in the PSTN environment because of its bandwidth limitations, will be the function of the DCME. In the future, the local ATM network could be equipped with congestion control mechanisms whenever the need arises.

The PSTN/N-ISDN network scenario shown above is a typical digital switched telephone network with bandwidth constraints. DCMEs A and B are connected on either end of the PSTN and transmit to, and receive from, the PSTN/N-ISDN voiceband signals. The PSTN/N-ISDN may also include

DCMEs to route the traffic from DCMEs A and B, thereby avoiding unnecessary successive encodings and decodings of the traffic.

DCME is used as a means of enhancing the capacity of digital transmission systems by providing circuit multiplication through the use of low bit rate speech coding and Digital Speech Interpolation (DSI). DCME is capable of accommodating speech, 3.1 kHz audio (voiceband data and speech), and 64 kbit/s unrestricted clear channel traffic. Facsimile traffic is processed by DCME in accordance with G.766 where demodulation and remodulation are likely to be used.

The use of DCME assumes that the interfaces to the ATM islands are conformed to G.703/G.704 at 1544 kbit/s or 2048 kbit/s. The use of DCME achieves:

- digital speech interpolation;
- low bit-rate coding using G.726/G.727 for ADPCM and in the future other ITU-T coding algorithms;
- congestion control mechanism that are adapted to the instantaneous traffic characteristics and the traffic mix either by local control (in the DCME) or by global control from the gateway switch through Q.50;
- facsimile demodulation/remodulation.

Facsimile demodulation/remodulation improves the performance of the transmission system with respect to burst errors. Synchronization and the echo cancellation at the destination DCME have to be considered for correct engineering of the DCME/ATM interface. The mapping between the ATM format into the G.763/G.766 format is for further study.

At the originating endpoint, the DCME determines the type of signal in the PCM stream. Accordingly, the PCM stream is analysed to determine if the channel is active and, if so, whether the signal is voice or other non-voice. For non-voice signals, the speed of transmission is determined to select the appropriate coding algorithm.

If the PCM stream is determined to carry Group 3 facsimile traffic, then the originating endpoint DCME will treat the signal as high-speed voiceband data if the modulation scheme is not recognized, or will demodulate the signal to extract the facsimile image data for transmission at the baseband rate. The compressor, packetizer and buffer/multiplexer perform the required functions in a conventional manner to compress and packetize the converted ATM header and payload into wideband packets for transmission over the PSTN/N-ISDN.

At the terminating endpoint, the DCME retrieves the original PCM and puts it in the payload field of the ATM packet. Signals are transmitted in the opposite direction in the same manner as described above.

A.2 Routing and tandeming issues

In an ATM cell header, the VPI consists of an 8-bit field that allows for 256 possible virtual channels. Similarly, the VCI is a 16-bit field that allows for 65 536 possible virtual channels. This large number of channels is possible at the broadband rates but at the primary rate, the number of channels is much smaller. Most of the traffic in a local ATM network will be internal to that network, rather than between separate local ATM networks. Therefore, the number of virtual channels that are used to interconnect local ATM networks will be a small percentage of the total number of channels.

The mapping function between the virtual channels in the local ATM network and the virtual channels in the wideband packet environment is accomplished as follows:

- For permanent virtual circuits, it can be done at provisioning time until all channels in the wideband packet network are exhausted.
- For switched virtual circuits, the mapping is done at call-establishment time.

If all channels in the wideband packet environment are exhausted, then the call shall be blocked by using appropriate protocols between the DCME and the ATM switch in the local ATM network. The use of extensions of Q.50 to cover that situation is for further study.

A.3 ATM-to-DCME interface

The ATM-to-DCME interface shall perform the following functions:

1) The ATM cell delay variation (CDV) has to be removed since a constant rate G.703/G.704 compliant bit stream must be provided to DCME at regular intervals. A possible way to remove/limit the CDV (i.e. jitter) is to buffer the ATM cells before they are converted to the G.703/G.704 format. The size of the buffer depends on the type of traffic and the network configuration. The buffer size should be specified while considering the amount of delay that will be introduced and the possibility that late cells will be declared lost and hence discarded. The method of cell replacement is for further study.

2) The CRC bits in each ATM cell shall be checked. If the check is valid, then the ATM-to-DCME interface shall extract the payload from the ATM cell and convert it to the G.703/G.704 format. If the check is invalid, then the cell should be discarded. The method of cell replacement is for further study.

3) The reconstituted G.703/G.704 bit stream is transmitted to the originating DCME for processing in accordance with G.763. The DCME bearer output frame is transmitted to the terminating DCME through the PSTN. The receiving DCME unit then decompresses the DCME bearer frame and converts the trunk signals into individual channelized G.703/G.704 bit streams.

4) The ATM-to-DCME interface at the receiving side converts the G.703/G.704 signals into ATM cells which are subsequently transmitted to the local ATM network.

5) In addition to the ATM cell payload, some ATM cell header fields and information used by the ATM adaptation layer may also need to be transmitted across the network. This can be done by assigning 64 kbit/s clear channels for signalling.

6) Special considerations for echo cancellation may be needed depending upon the ATM cell fill strategy and the overall propagation delay. Preferably, echo cancellation should be performed as close to the source as possible.

APPENDIX I

Timing issues related to echo cancellation in ATM networks

I.1 Introduction

This Recommendation is offered as a summary of the timing techniques that may be adopted to minimize the impact of ATM Cell Delay Variation on timing quality for constant bit rate services.

In essence it shows that when an ATM network falls inside the echo tail of a voice connection, as in Figure I.1, the CDV induced phase noise may be restricted to that of contemporary TDM networks by use of the appropriate synchronization technique [i.e. Network Synchronous operation or Synchronous Residual Time Stamp (SRTS)]. However, recognizing that both techniques require the delivery of a relatively pure reference clock to both ends of the ATM network, and that in some instances this may not be possible – the use of adaptive timing may be considered provided that the residual phase wander is within the bounds of the echo canceller's phase noise tolerance. Further work is needed to check whether adaptive clock recovery techniques and the resultant residual phase wander will be compatible with echo canceller operation.

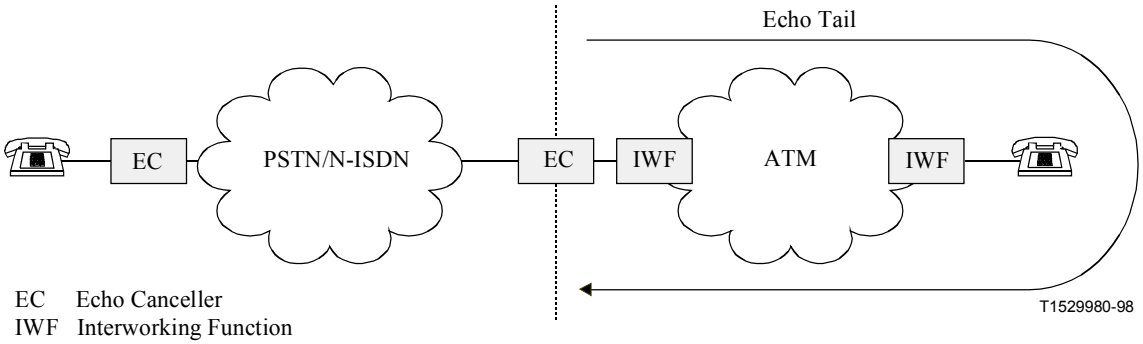


Figure I.1/I.741

I.2 Cell delay variation

When a constant bit rate stream is fed into an ATM network the stream is mapped into the ATM cell payload and the ATM cells passed to the physical layer at regular intervals (ignoring waiting time jitter etc.).

On traversing the ATM network, in the absence of cell delay variation, the cells would arrive with constant inter-interval time and could be played out immediately upon receipt on the constant bit rate interface. Just as the buffer is about to empty the next cell would arrive to replenish the buffer.

However, if each cell is subjected to a different delay through the network and, for example, if the second cell arrives late the buffer would empty and have no more bits to send. If the second cell arrives early, the 47 byte buffer would overflow. Therefore, the play-out buffer needs to be dimensioned and operated in such a way as to allow for late or early cell arrivals. The usual technique is to delay playout of the initial cell by the calculated maximum cell delay variation allowance. This has the effect of ensuring no buffer depletion even when the first cell arrives very early and the second cell arrives very late [Figure I.2 a)]. However, the buffer now needs to be enlarged to at least the payload size plus the number of cells that could be delivered in an interval equal to twice peak-to-peak CDV. This ensures that, if the first cell actually arrives very late and is additionally delayed by the peak-to-peak CDV before playout and subsequent cells arrive very early, there will still be space available for them in the buffer [Figure I.2 b)]. In this latter case the buffer level needs, ideally, to be optimized over a period of time to ensure the cells are delayed in the buffer for a period not in excess of the peak-to-peak cell delay variation.

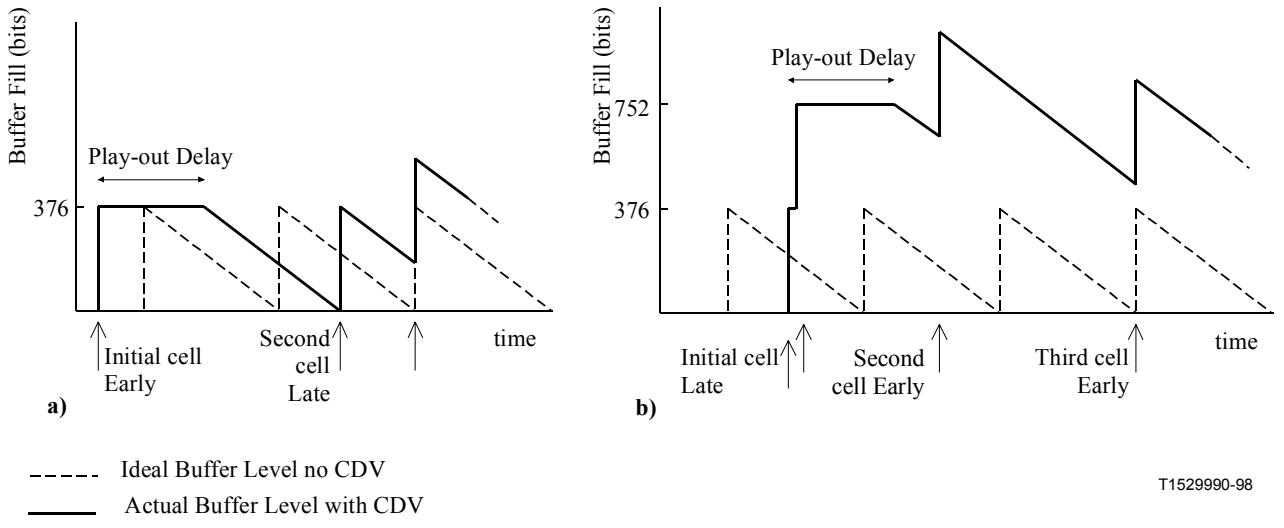


Figure I.2/I.741 – ATM Cell Arrivals with CDV

Where a receiver's clock takes time to lock to the transmitter, or where the receive clock varies in a time dependant fashion, the buffer level will vary beyond that influenced by CDV and the time taken to lock and the frequency difference over time should be taken into account when specifying the delay needed before initial playout and total buffer size. The delay in the buffer can be thought of as the elimination of variable delay by an increase in total fixed delay, the total fixed delay of the ATM network thus becomes the fixed transmission propagation delay plus the peak-to-peak CDV.

The main mechanism, among many, responsible for cell delay variation within an ATM network is output port contention. Given independent traffic streams on each input port (and given an output-port buffered, non-blocking, switch design) cells arriving at the switch at a regular rate will have to wait varying amounts of time in the output buffer dependant on the number of cells instantaneously contending for the same output port. The regularity of the input traffic stream is thus disrupted and cells arrive at their destination at irregular intervals. Other mechanisms that can contribute to CDV include that of waiting time jitter where the intercell period dictated by the transmitting service clock does not map exactly to the cell interval available on the physical transmission line, and variation in delay experienced through the switching fabric of an ATM switch.

The main parameter affecting buffer dimensioning at the receiver and initial play-out delay is thus peak-to-peak cell delay variation. However, when using an adaptive clock recovery synchronization technique the time dependence of CDV can adversely affect the purity of the recovered clock leading to larger play-out buffer dimensions (or in the absence of a larger play-out buffer, cell loss) and jitter and wander of the output bit stream.

Many published papers model the characteristics of cell delay variation for various network reference models, network loads and traffic characteristics. Many make use of analytical queuing models, such as N*D/D/1 or M/D/1 models for a single switch, as a basis for network evaluation, others use numerical simulation techniques, and yet others attempt to load prototype ATM switches with "real" traffic in an attempt to characterize the CDV likely to be incurred in a "real" network. No one technique can exactly predict the performance expected of real networks since the network's characteristics will be dynamic and strongly influenced by the network operator's traffic management policies. For example, such a policy may dictate the traffic loads allowed by Connection Admission Control (CAC), the service partitions, traffic shaping functions and the service dependant buffer management algorithms to be enacted for different services and differing qualities of service. For networks with switch output ports lightly loaded, little or no CDV would be incurred, whereas in networks where constant bit rate traffic is made to contend with large and varying switch loads, large cell delay variation can be expected. For each specific case the peak-to-peak CDV incurred by the service and its time-dependant characteristics will be very different. The onus is therefore on each network operator to ensure that its traffic management policy and simulation studies evolve towards a network design capable of meeting the requirements of each specific service that it offers on its ATM network.

For simulations attempting a worst case analysis, the M/D/1 queuing model, which assumes poisson arrivals and deterministic service time, is viewed by many as adequate for predicting worst case CDV.

As an example the waiting time distribution of an M/D/1 queue is given by:

$$Q(x) = \sum_{n>x}^{\infty} \frac{(\rho(n-x))^n}{n!} e^{-\rho(n-x)} (1-\rho)$$

and for $\rho = 0.9$ (i.e. a 90%) switch load the peak to peak CDV (defined here as the 10^{-3} quantile for comparison with Figure I.2 a) below which comprises ~1000 samples) is calculated as x = 34 cell times. For an STM-1 output port this equates to a peak to peak CDV of 96 μs.

Such pessimistic results can be used to engineer robust buffer management policies. However, such analytical techniques give little information on the expected time-dependence of CDV since by

default the models imply an essentially "white" frequency spectrum for a static load. Numerical simulation techniques and "real" measurements therefore provide the best opportunity to understand the frequency characteristics of CDV. The cell delay characteristics and CDV power spectral density resulting from a simulation of 2 Mbit/s CBR connection, multiplexed with 15 other Bernoulli traffic sources for a fixed total output buffer load of 90%, is shown in Figures I.3 a) and I.3 b) below:

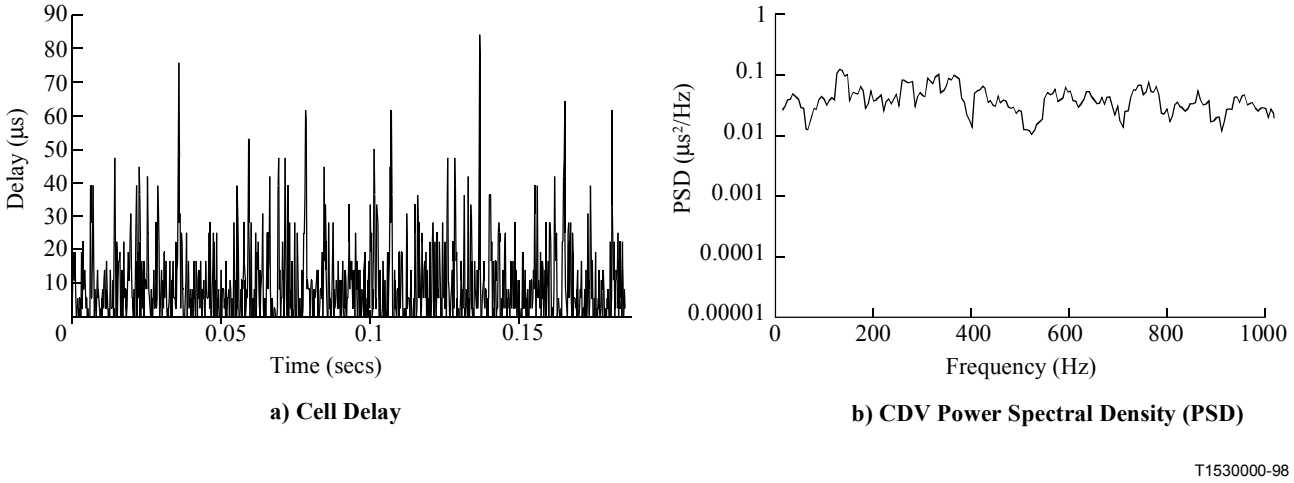


Figure I.3/I.741

The limited results of the simple numerical model support the analytical model results in that an essentially "white" power spectral density is predicted. However, caution has to be applied to such simplistic modelling. Models such as these again generally tend to evaluate the effects of a static load on the output buffer. Any slow changes in network load over the day could result in strong spectral lines at low frequencies. Any step changes in network load, contention of CBR streams with bursty variable bit rate streams or dissimilar rate CBR streams, or the effects of waiting time jitter can also result in strong spectral characteristics at both low and high frequencies. As an example Figures I.4 a) and I.4 b) show the effect of a step change in network load from 70% to 90% on the power spectral density. Low frequency components are now seen to dominate.

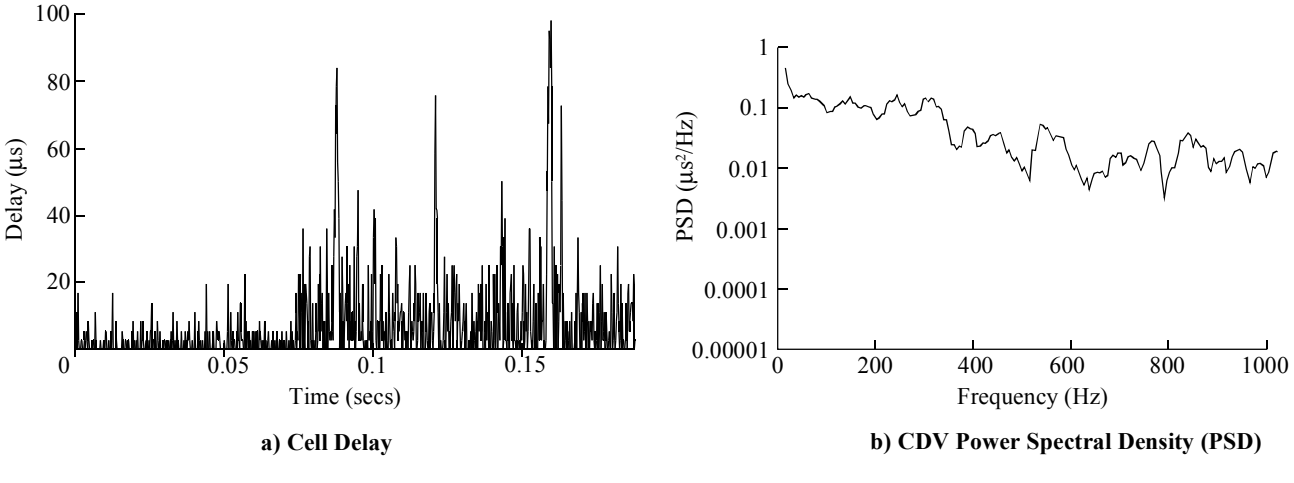


Figure I.4/I.741

It is important therefore that not only are the cell level effects at static load understood but equally important is an understanding of the effects of network load statistics. Such effects can restrict adaptive clock recovery techniques to only selected CBR services in which the higher levels of jitter and wander can be tolerated.

I.3 Eliminating or reducing the effects of CDV on timing

Three solutions exist at the ATM layer to eliminate the effects of CDV from constant bit rate connections these comprise: a) fully network-synchronous operation by using a network derived clock as the service clock, b) the use of Synchronous Residual Time Stamp (SRTS) to transmit service clock information, and finally c) adaptive clock recovery.

Additionally, where the network is solely responsible for transporting ATM cells, rather than delivering a constant bit stream to the user, the receiving higher level application layer can have the added responsibility for service clock derivation.

These aspects are reviewed in more detail below.

I.3.1 Network synchronous operation

In forcing an end-station to operate in synchronism with the network clock the effects of CDV can be completely eliminated. As shown in Figure I.5, the service clock is derived directly from the network clock. Given the presence of a network clock at both the transmitting and receiving end-stations, the service bit stream can simply be clocked out of the playout buffer at the service bit rate, fully independent of the cell delay variations caused by the ATM network. A playout buffer with correct dimensions and initial delay in playout is still required to ensure that CDV does not cause cell loss or padding bits to be required. In the event of network clock failure the buffer will also require either a buffer slip algorithm with the receive clock placed in hold-over mode or the receiver must revert to an adaptive clocking algorithm.

The network clock is distributed through the synchronization of the physical layer connecting the ATM network elements. These ATM network elements may themselves be synchronized via an external physical timing interface or as a slave of another ATM network element via the physical layer connection.

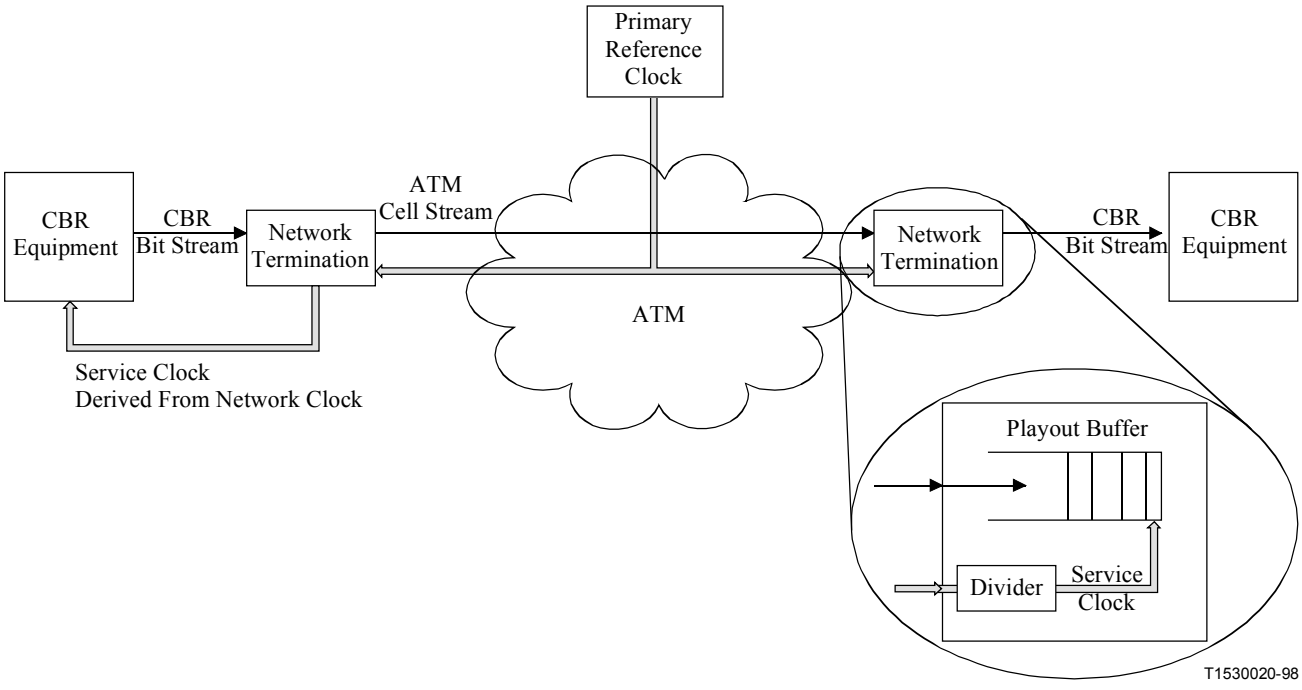


Figure I.5/I.741 – Network Synchronous Operation

I.3.2 Synchronous residual time stamp

The above network synchronous option has the drawback that not all end-stations and CBR sources would wish to synchronize to the network clock. In these instances one option is to transport information about the source clock across the ATM network to eliminate playout buffer depletion or overflow. The technique adopted for this is called the Synchronous Residual Time Stamp (SRTS) technique which is closely associated with the ATM Adaptation Layer Type 1 protocol. To allow SRTS to work accurately the network needs to distribute a good quality network clock to the network interface.

Its general implementation is shown pictorially in Figures I.6 a) and I.6 b).

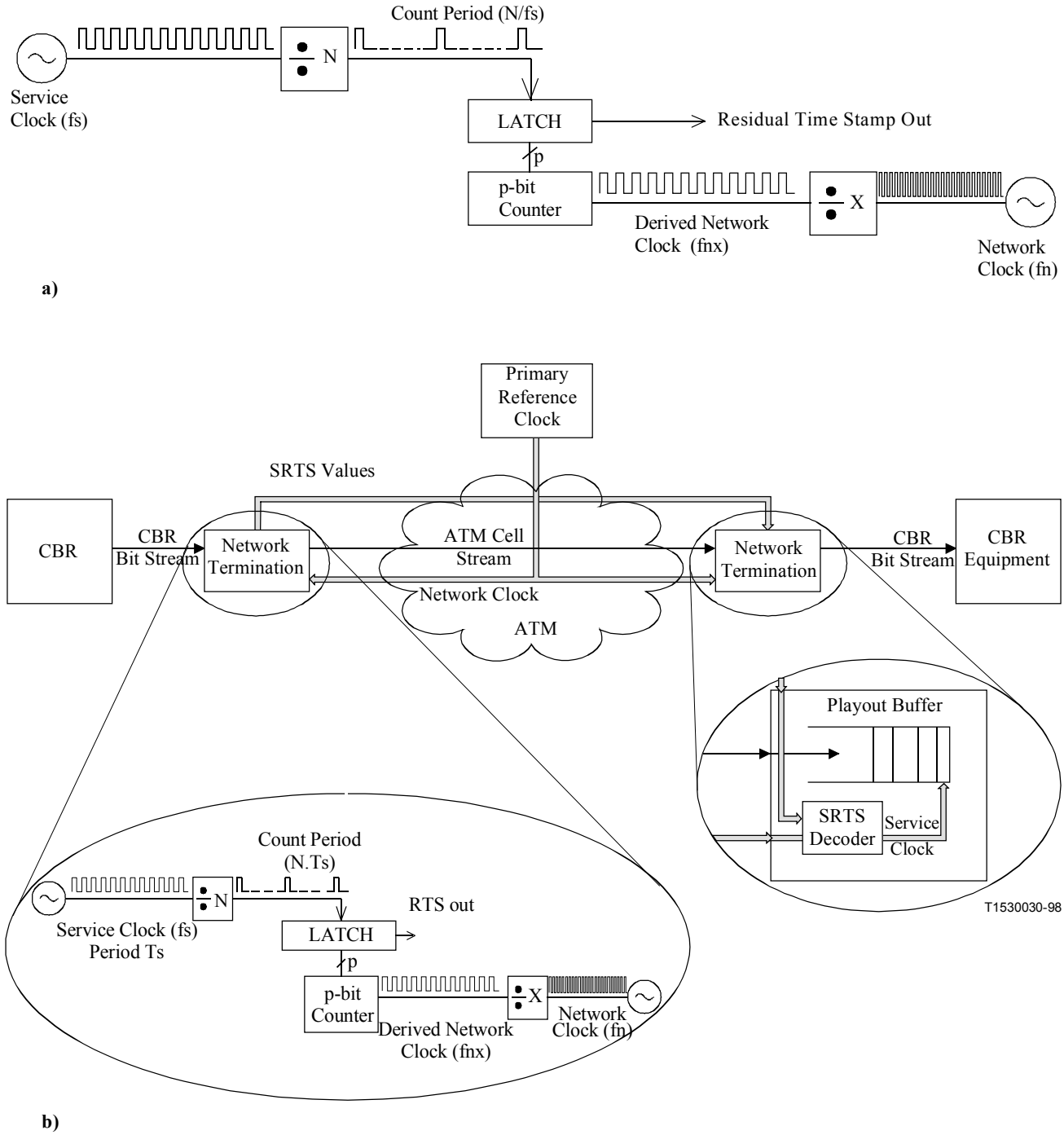


Figure I.6/I.741 – Synchronous Residual Time Stamp (SRTS) implementation

With SRTS the number of derived network clock cycles (fn/X) in N cycles of Service clock is counted in a p-bit counter and this p-bit SRTS value transmitted across the network to the receiving network terminating point. At the receiving terminal the local service clock can be adjusted against the reference network clock to ensure that the same number of derived network clock cycles are counted over the same N cycles of local service clock, thus locking the local service clock to the transmitter service clock by use of the received residual time stamps and the reference network clock.

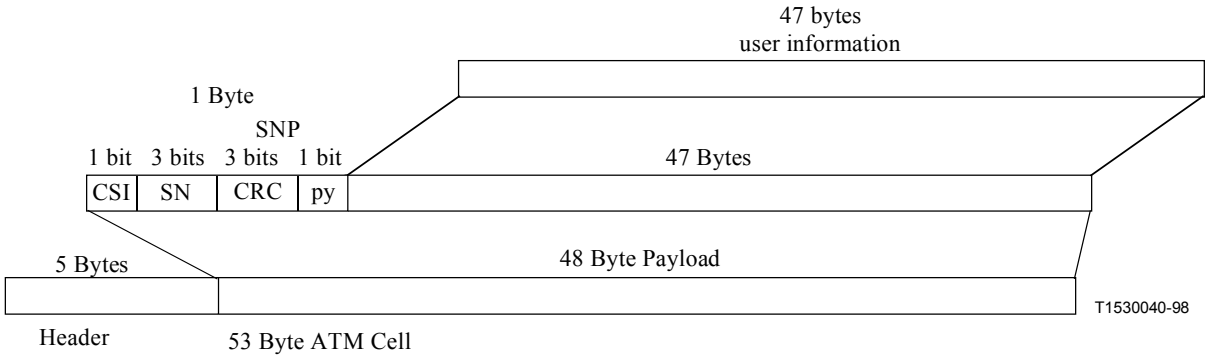
For G.702, 1.544 Mbit/s and 2.048 Mbit/s based CBR hierarchies the value of N = 3008 and a p = 4-bit SRTS value has been agreed and specified in I.363.1.

The derived network clock f_{nx} is specified uniquely by assuming the existence of an 8 kHz clock derived from the network frame rate and constraining f_{nx} by the following:

$$f_{nx} = 8\,\text{kHz} \times 19\,440/2^{k} \text{ where } k = 0, 1, 2.....11$$

$$1 \le f_{nx} / (fs) < 2$$

The 4-bit SRTS value is transported over the ATM network as Convergence Sublayer Indication (CSI) bits distributed alternately over 8 consecutive ATM cells using ATM Adaptation Layer Type 1 (Figure I.7).



CSI Convergence Sublayer Indication
SN Sequence Number
CRC Cyclic Redundancy Check
Py Even Parity bit
SNP Sequence Number Protection

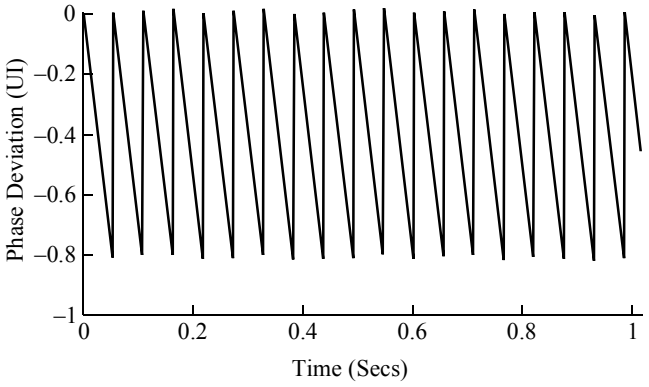
Figure I.7/I.741 – AAL type 1 – Non structured data format

The value of N = 3008 has been chosen which corresponds to the number of AAL-type 1 user information bits in 8 ATM cells.

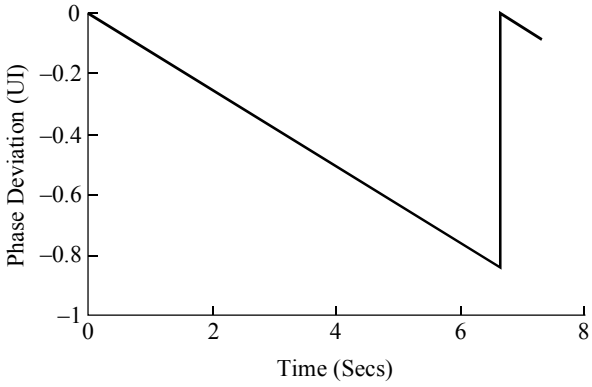
Since the nominal service clock frequency is known by both transmitter and receiver the full derived network clock count need not be sent. Hence the use of only 4 bits as a "residual", or off-set, rather than full count. This residual count gives an indication of offset from nominal clock frequency. The use of 4-bits allows up to a ±200 ppm offset from nominal clock frequency.

The quantized nature of the residual time stamp will lead to slight clock imperfections at the receiver. The effect of quantization may be visualized by examining the implementation details for a specific service such as a 2.048 Mbit/s CBR service. In this particular implementation the derived network clock is specified, from the constraints given above, as 2.43 MHz. The number of derived network clock cycles in 3008 service clock cycles is counted in 4-bit modulo 16 counter. For a 10 ppm offset service frequency the total count would be 3569.0268 derived network clock cycles.

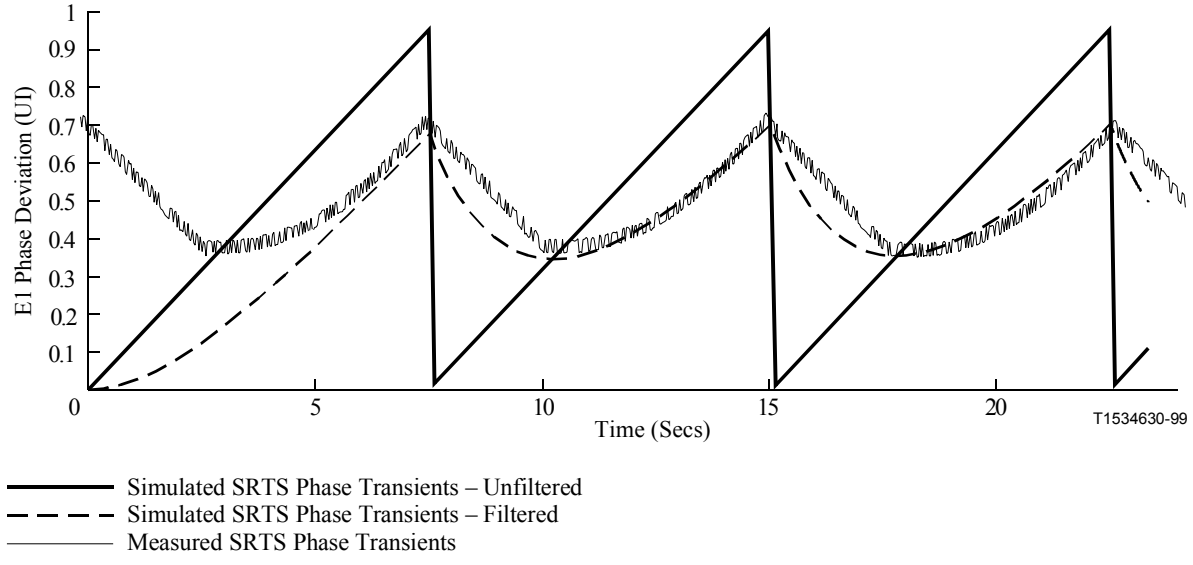
The 4-bit residual time stamp truncates this to 3569 and sends the residual modulo-16 count of 0001 binary. With knowledge of the nominal service frequency the truncated derived-network-clock count of 3569 can then be generated at the far end on reception of the RTS value 0001 binary. The service clock generated from this truncated value is given by 2.43 MHz*(3008/3569) = fs = 2.048 MHz + 17.5 ppm i.e. some 7.5 ppm in error due to the RTS quantization. This static frequency error and thus increasing phase error will continue until the partial clock counts of 0.0268 cycles per RTS period accumulate (over 1/0.0268 = 37 RTS periods) to greater than unity giving a 3570 clock count and implied service clock frequency for this RTS value of fs = 2.048 MHz – 262.6 ppm, this time – 272.6 ppm in error from the transmit service clock. However, in this case over the long term of 37 RTS periods the average frequency information given = (37 × 17.5 ppm) – 262.6 ppm = +10.128 ppm, which begins to close in the true transmit service frequency. Thus by taking the longer term average of the RTS values the true underlying transmitted service frequency can be determined and tracked. The overall effect is best viewed by looking at the time dependant phase difference of the received service clock implied by the RTS values to the actual transmit clock. This is shown in Figure I.8 a) below for the example just given. The induced phase transients in this particular case are sufficiently frequent that if necessary they could be reduced by a sufficiently long time constant in the phase locked loop being used to derive the receive service clock.



a) RTS phase transients +10ppm transmit clock offset



b) RTS phase transients +17.45ppm transmit clock offset



c) SRTS Phase Transients

Figure I.8/I.741 – RTS and SRTS phase transients

For certain values of service frequency, particularly where the derived network count is close to an integral number, the phase transients will become so infrequent that it becomes more difficult to filter them out, as shown in Figure I.8 b) and Figure I.8 c). It should be noted that Figure I.8 c) represents a simulation and measurement comparison for a commercial Data Service Unit (DSU) with an E3 ATM UNI and an E1 circuit emulation interface. This DSU utilizes an early I.363 implementation of SRTS.

In earlier versions of I.363 the derived network reference clock frequency was not fully specified and this unit appears use a now non-standard 34.368 MHz/16 = 2.148 MHz derived network reference clock. This gives rise to a slightly larger potential peak phase deviation of 0.9 UI which is exhibited by both the simulation and the measurement. The use of 2.148 MHz rather than the more recently defined 2.43 MHz for the derived network reference clock would make early I.363 SRTS circuit emulation implementations incompatible with their more recent counterparts.

Even for the case of the isolated phase transients the peak phase deviation falls inside of the G.823 Recommendation limits for wander and jitter on PDH interfaces. Therefore, provided a good quality network clock is delivered to the network interfaces the SRTS technique is capable of delivering third party timing across the ATM network within the jitter and wander constraints imposed by G.823. Such imperfections and the additive effect of service clock and network clock imperfections may however, make SRTS unsuitable for the transport of equipment clock quality signals – this is for further study. Also for further study is the actual specified quality level of the network clock needed at the ATM node responsible for circuit emulation timing.

I.3.3 Adaptive clock recovery

Where ATM cells traverse a number of different ATM networks, it may not be possible to provide a common network clock to the transmitting and receiving end-stations. Also, some services may not require the purity of clock available from the above network synchronous or SRTS schemes. In these instances it may only be possible or more cost effective to use an adaptive clock recovery technique.

The technique of adaptive clock recovery is depicted in Figures I.9 and I.10 which serve as an introduction to the basic theme.

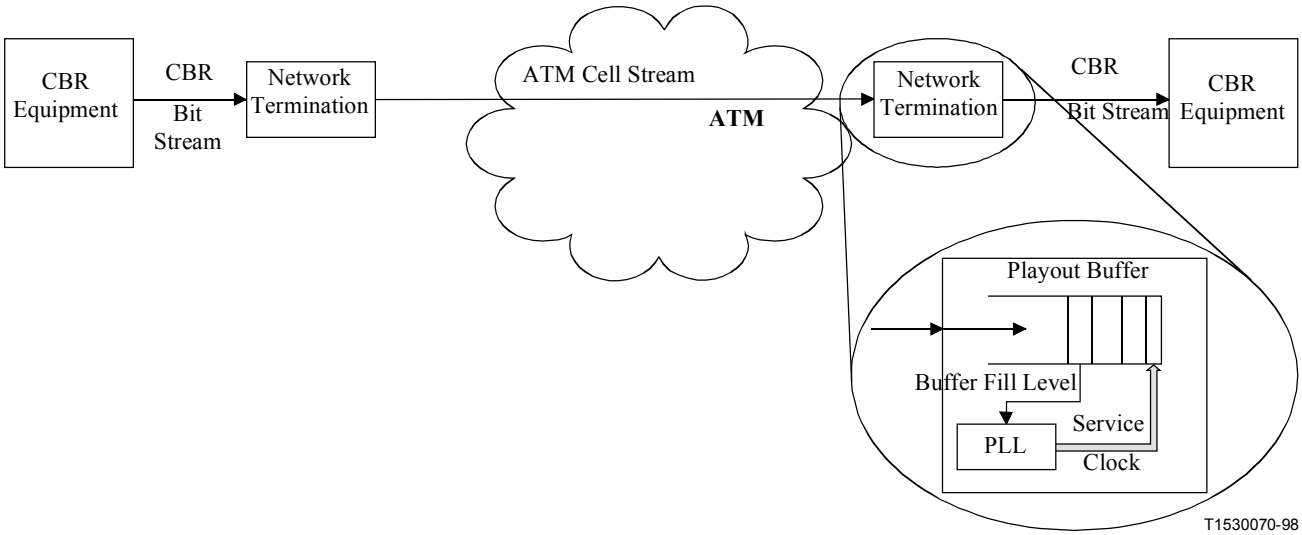


Figure I.9/I.741 – Adaptive Clock Recovery

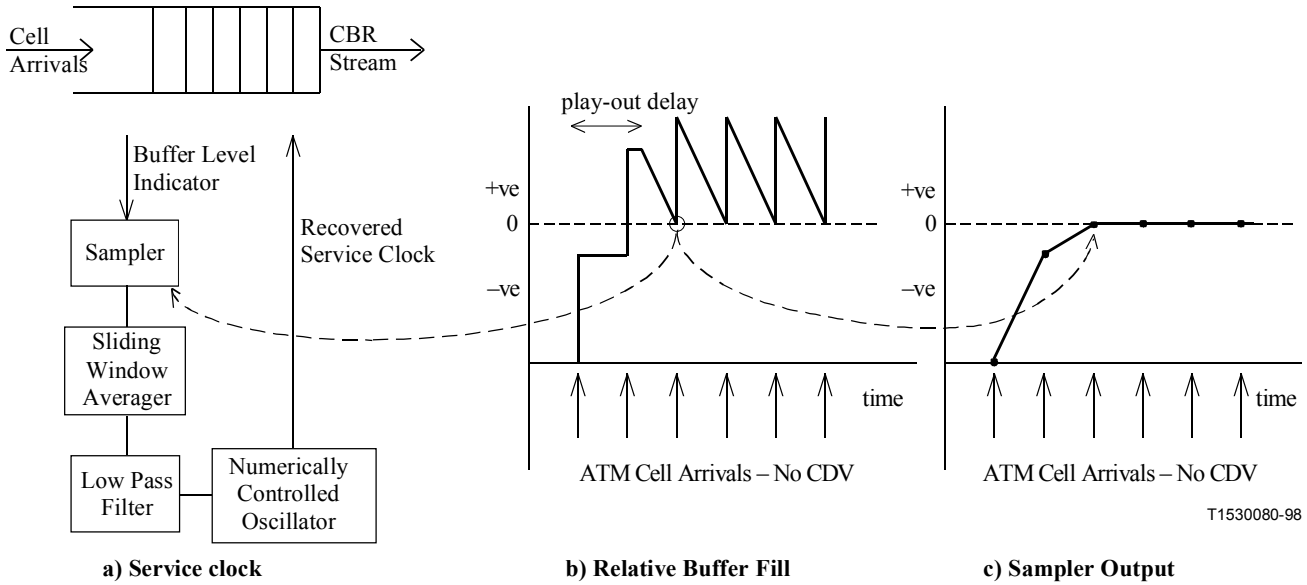


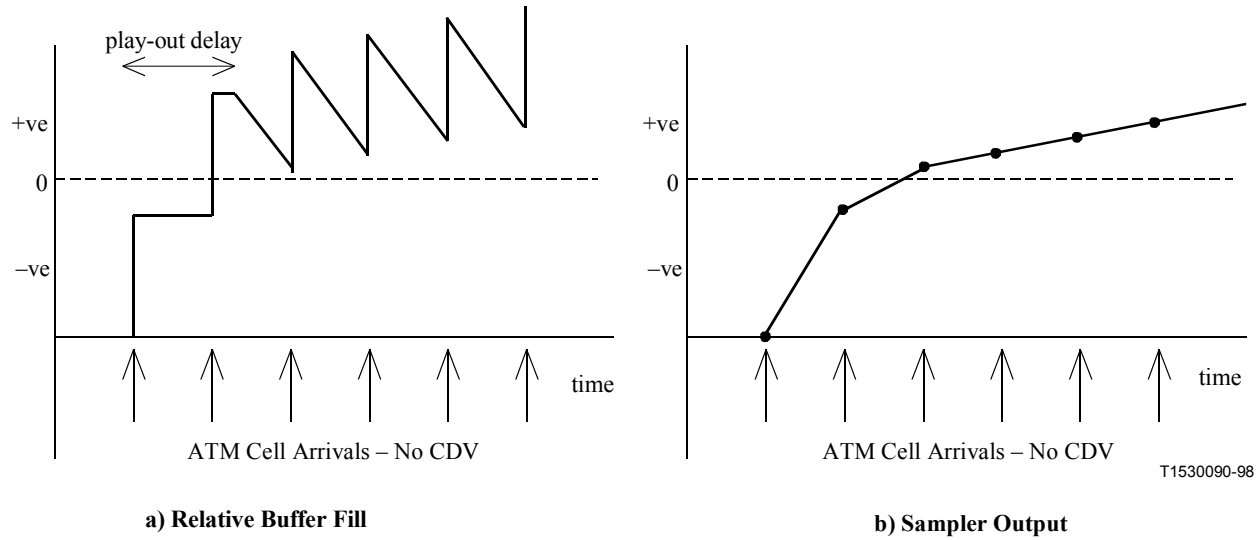
Figure I.10/I.741

In general, adaptive clock recovery relies on the fact that, irrespective of the amount of delay variation experienced in the network, the CBR cell stream has an underlying average inter-arrival time. The job of any adaptive clock recovery mechanism is to extract this longer term average inter-arrival time from the "noise" produced by both CDV and cell loss, and to use this as a basis for received service clock derivation.

The data buffer acts as phase comparator of the incoming cell stream and outgoing bit stream – the buffer fill level being the output of the phase comparison. Since on cell arrival the service bits are delivered "in bulk" by the ATM payload the buffer fill varies in a "saw-tooth" fashion as in Figure I.10 b), even in the absence of CDV.

If this waveform is sampled at the cell arrival rate, in the absence of CDV and/or waiting time jitter, and with the transmitting and receiving clocks locked the sampled values will be of constant value as in Figure I.10 c).

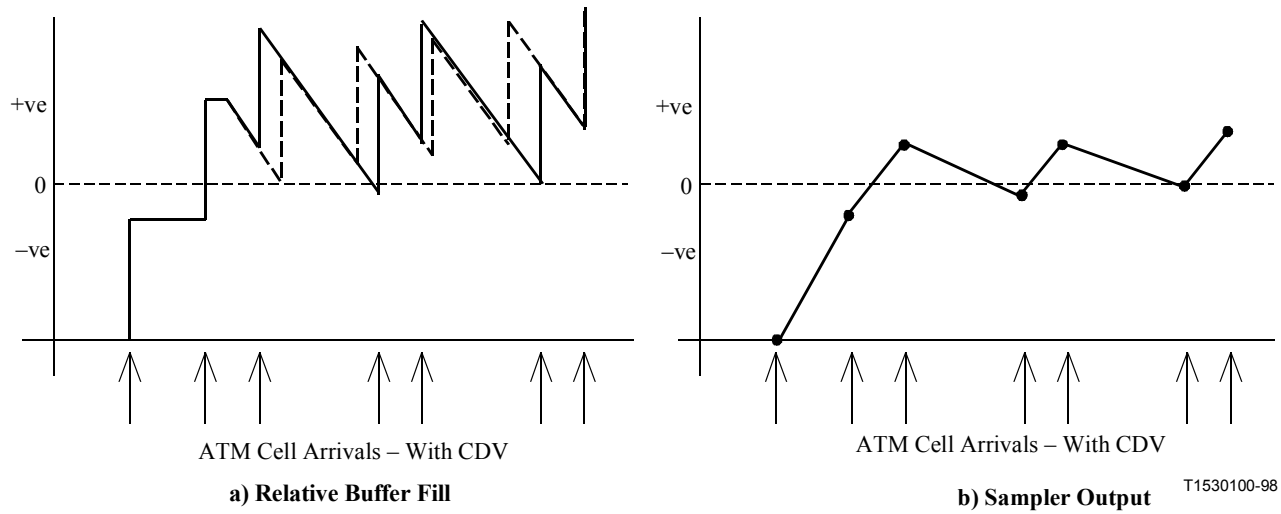
If the receiving clock is too slow compared to the transmitter the average buffer level will rise with time and the sample values would gradually increase in value as in Figure I.11.



a) Relative Buffer Fill **b) Sampler Output**

Figure I.11/I.741

This trend, once detected, can be used to increase the receive clock frequency to bring the buffer level back to a nominal value and lock-in the receiving clock to that of the transmitter. Unfortunately, the presence of CDV can obscure the underlying trend as shown in Figure I.12 below:



a) Relative Buffer Fill **b) Sampler Output**

Figure I.12/I.741

The buffer level sample values cannot therefore be used directly but must be filtered in such a way as to allow the recovered clock to react only to a mismatch of the transmitter to receiver clocks. In general such a mismatch would result in a continued increase or decrease in average buffer fill level over the averaging period. The adaptive recovery algorithm should ignore the relatively more rapid fluctuations around the longer term average due to CDV.

The adaptive clock recovery scheme therefore acts as a low pass filter. As a result low frequency CDV, as may occur due to a slowly cyclic or step change in network load, will be misinterpreted as a frequency mismatch, as shown in Figure I.13. With low frequency CDV the buffer level will

increase or decrease over the averaging period of the adaptive algorithm in much the same way as that due to transmitter-receiver mismatch. The adaptive recovery circuit will erroneously respond to low frequency CDV producing low frequency phase variation of the recovered clock in concert with the CDV.

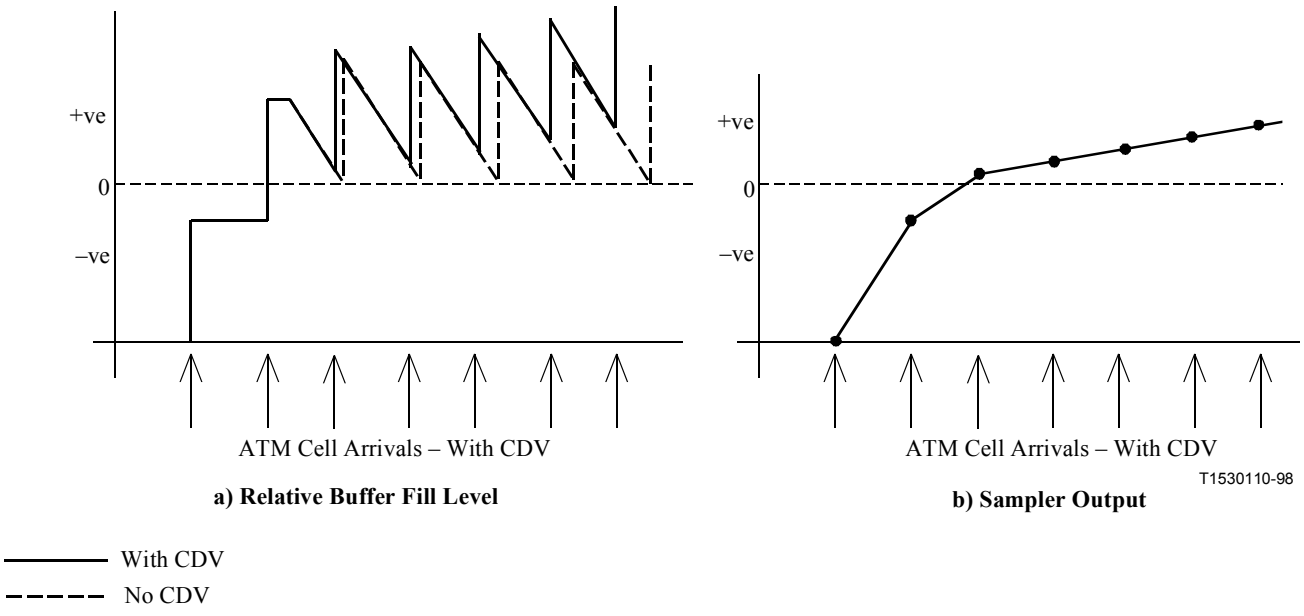


Figure I.13/I.741

To demonstrate this, the effect of the CDV characteristic of Figure I.4 a) (and reproduced over a longer time period in Figure I.14 a) on a simulated 2.048 MHz adaptive clock recovery scheme is shown below in Figures I.14 a) through I.15 c).

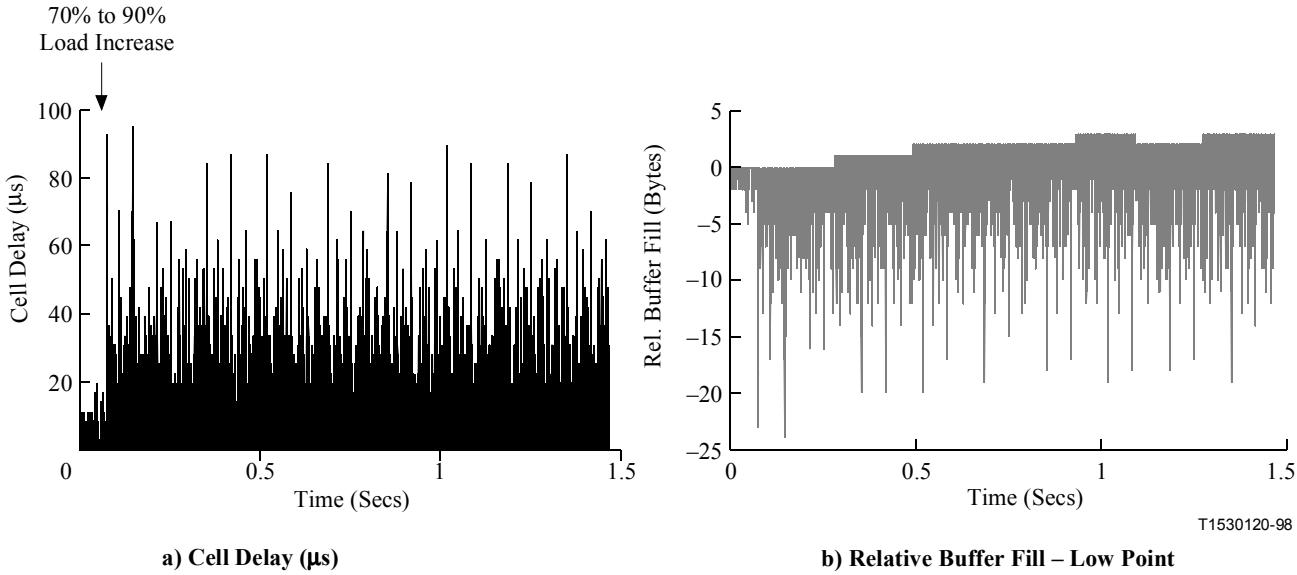
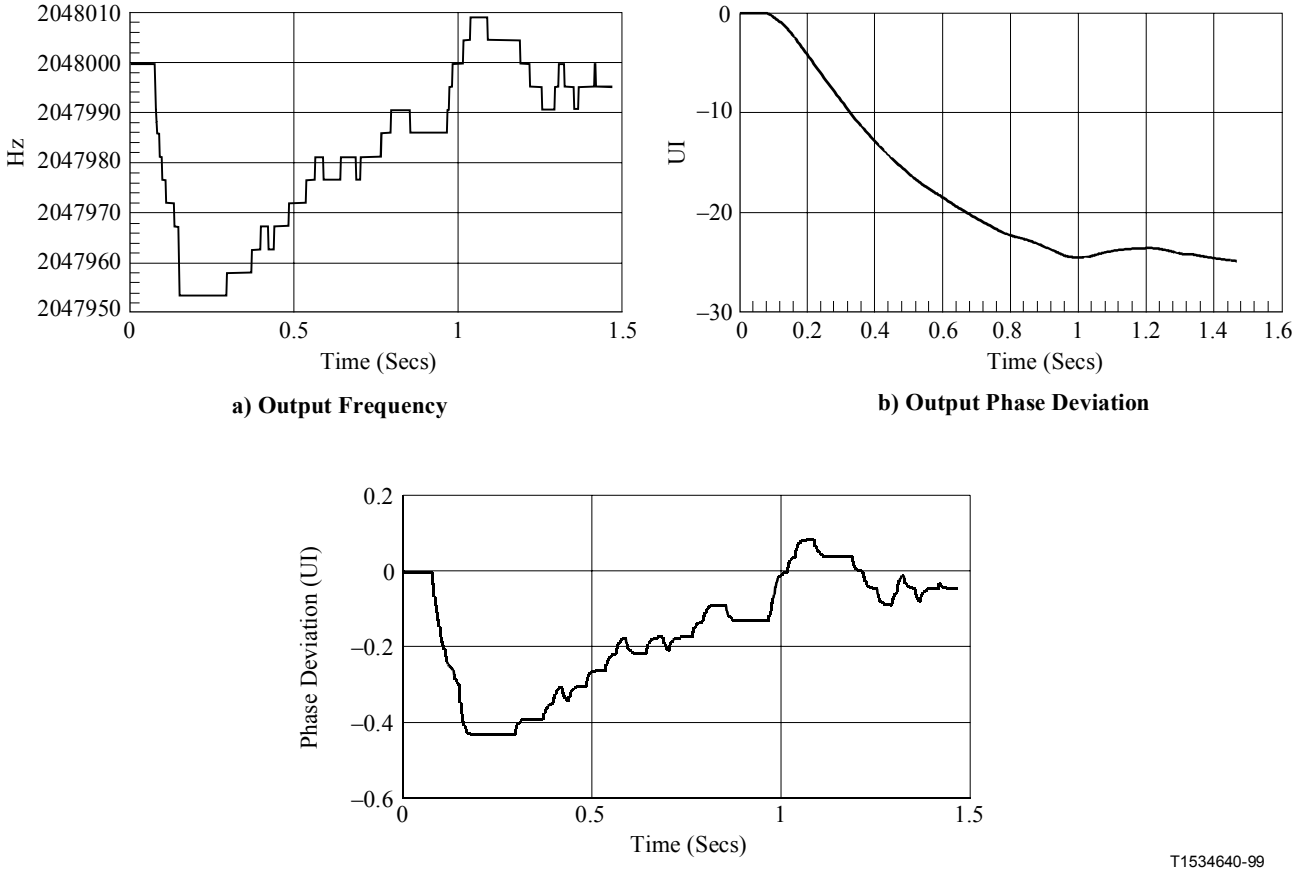


Figure I.14/I.741

The late cell arrivals in Figure I.14 a) are reflected as low buffer levels in Figure I.14 b).

The output frequency deviation, total output phase deviation (wander) and jitter above 20 Hz is shown in Figures I.15 a) through Figure I.15 c) respectively.



a) Output Frequency

b) Output Phase Deviation

c) Output Phase Deviation – After HPF

Figure I.15/I.741

The adaptive clock recovery mechanism can be seen to respond to the rms increase in cell delay when the switch load instantaneously increases from 70% to 90%. The rms increase in delay causes a general lowering of the buffer level and the output frequency is decreased momentarily to bring the mean buffer level back to normality. The frequency transient in this case causes a peak-peak jitter above 20 Hz of 0.5 Unit Intervals (UI) [Figure I.15 c)] and a total output phase deviation equivalent to the increase in rms transport delay of 24.4 UI = 11.9 µs [Figure I.15 b)]. These results are for a single switch, in general the load characteristics for all switches through which the CBR cell stream pass must be taken into account by the simulation and the peak to peak phase deviations due to network load variations will easily exceed the values shown here.

The numerical simulation model above had shown the 2 Mbit/s output clock to track the slow changes in switch delay due to changing network load. The model had shown that for an increase in output port load from 70% to 90% the rms switch delay, for an STM-1 output port, would increase by 11.9 µs and that the 2 Mbit/s output clock phase would track this increased rms delay as shown in Figures I.16 and I.17 respectively. [NOTE – 11.9 µs = 24.4 Unit Intervals (UI = Bit Periods) at 2.048 Mbit/s.]

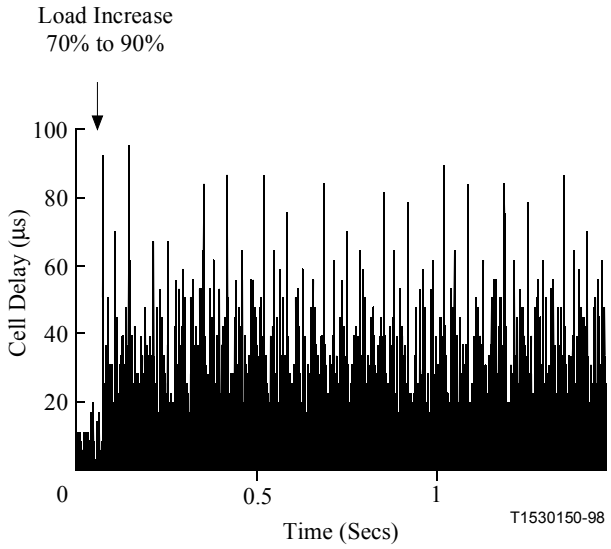


Figure I.16/I.741 – Cell Delay

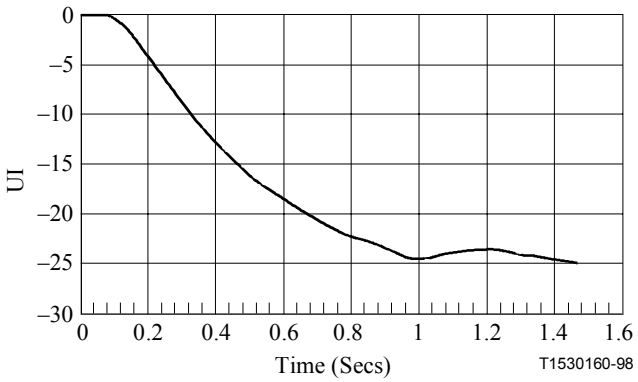


Figure I.17/I.741 – Output Phase Deviation

The mean (rather than rms) switch delay at 90% load exhibited by the numerical model in Figure I.16 was 10.1 µs. This result is supported by analytical analysis for an M/D/1 queue which gives the worst-case mean delay, $\lambda(\rho)$ in switch cell times, for a given load (ρ) as:

$$\lambda(\rho) = \frac{\rho}{2(1-\rho)} \qquad (1)$$

Thus by equation (1) the increase in mean delay expected from a load of 90% = $\lambda(0.9)$ = 4.5 cells = 4.5×2.83 µs for an STM-1 output port = 12.75 µs = 26 UI at 2.048 MHz.

It was expected therefore that if an output port of the ATM switch could be artificially loaded to, say 90%, phase tracking, similar to that shown in Figure I.2, ought to occur on the 2 Mbit/s CBR output of the adaptive clock recovery module thus causing the 2 Mbit/s output phase to wander in concert with longer term (sub 1 Hz) load variations.

I.3.3.1 Experimental configuration

In order to artificially load an output port on the ATM switch the technique of "tromboning" was used whereby the input load source is re-circulated through the switch with the relevant VP identity changes and physical patch cord links to cause "real" load-like contention at a designated output port. Although tromboning is thought to provide imprecise cell delay distributions it was expected that, for a given trombone induced load, roughly the same mean delay increase would be experienced as for "real" bursty traffic. The tromboning as implemented is shown in Figure I.18.

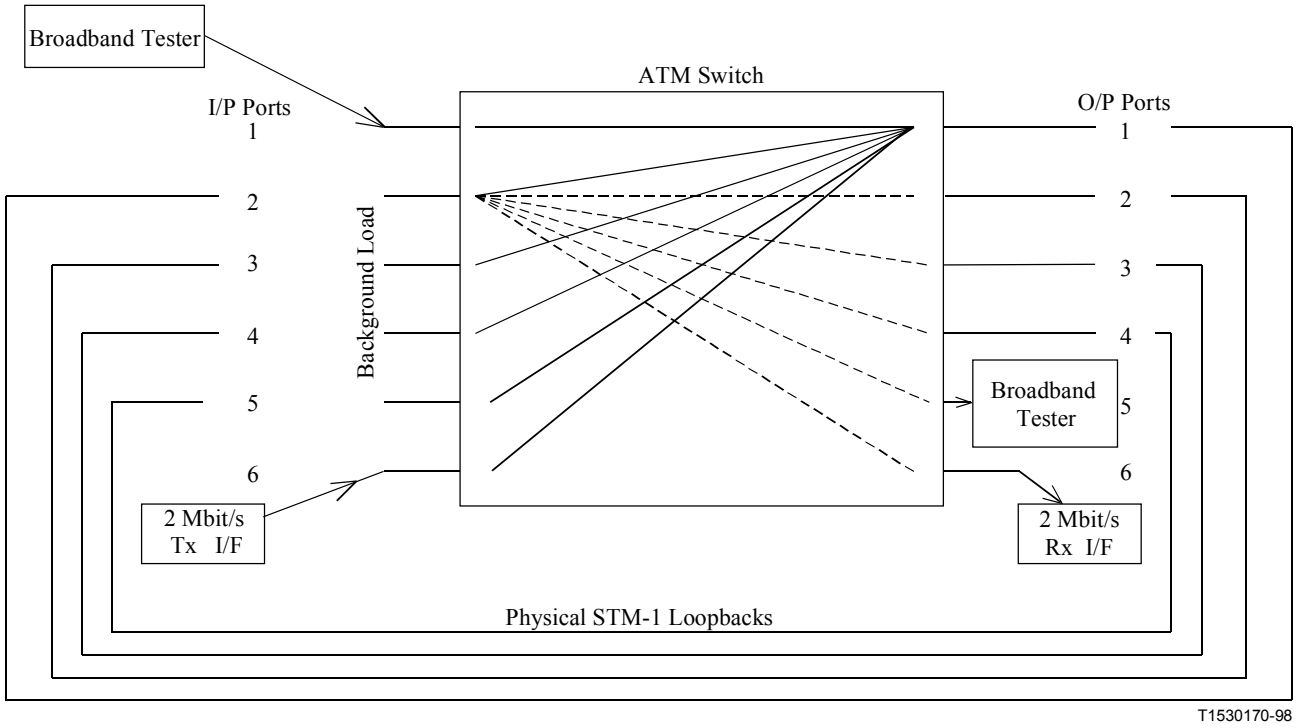


Figure I.18/I.741

The logical VP connectivity to provide load contention is shown in Figure I.19.

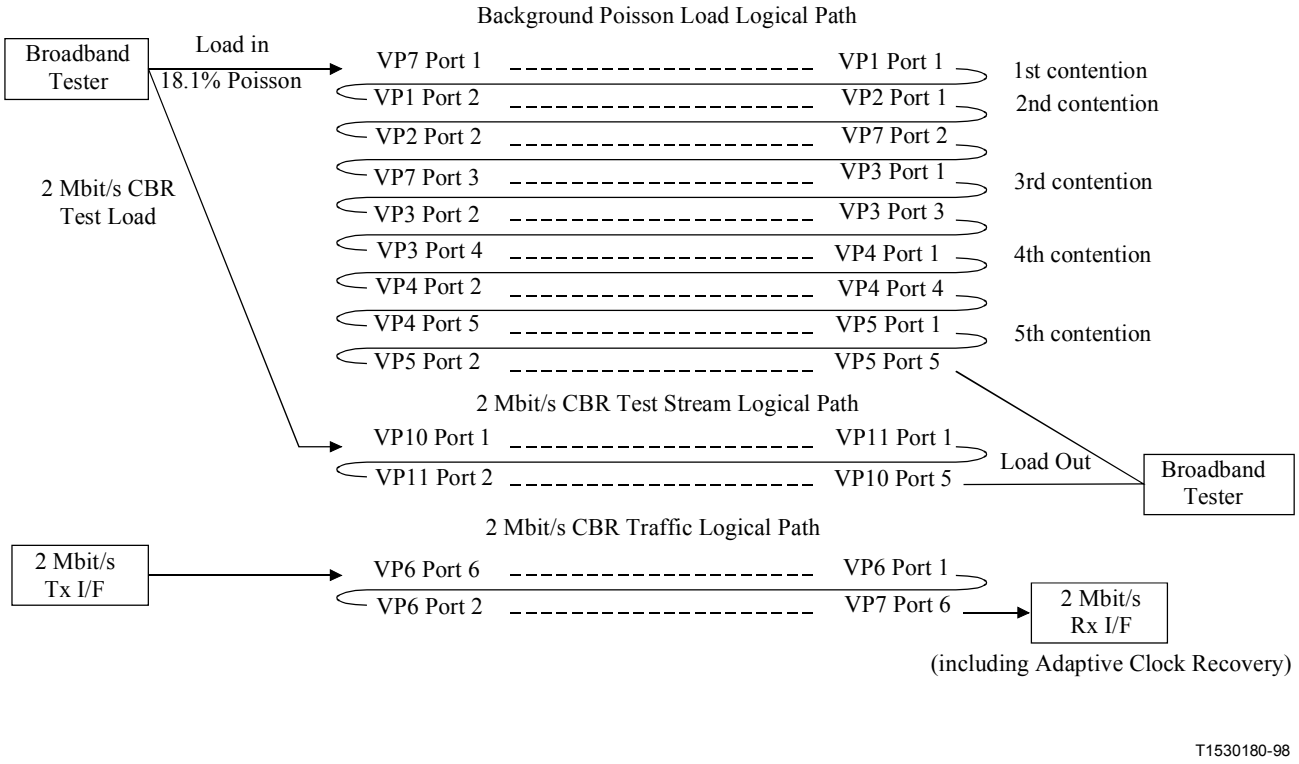


Figure I.19/I.741

As shown in Figure I.19 the background load comprised two components. The first was a bursty Poisson load generated by a broadband tester to give a mean load of 18.1% on its STM-1 output interface.

This load is tromboned through five separate input ports, ports 1 to 5, to give a total load contention at output port No. 1 of $5 \times 18.1 = 90.5\%$. The second component of the background load was a 2 Mbit/s CBR test stream also generated by a broadband tester concurrently with the Poisson load. This test stream was used to measure the mean delay change through the switch as the Poisson load component was turned on and off, for comparison with that predicted by equation (1) and the measured phase change of the 2 Mbit/s receive clock.

The two 2 Mbit/s cell streams from the Broadband tester and 2 Mbit/s Transmission interface constitute an additional load of $\sim (2 \times 2 \times 10^6/155.52 \times 10^6) \times (2430/2340) = 2.7\%$, accounting for STM-1 section and path overhead. Therefore, as the Poisson background load is turned on the total switch load becomes $90.5 + 2.7 = 93.2\%$.

The worst-case expected delay increase $\lambda(\rho)$ for $\rho = 0.932$ given by equation (1)

$= 6.85$ STM-1 cell times

$= 6.85 \times 2.8\ \mu s = 19.2\ \mu s$

$= 19.2 \times 10^{-6} \times 2.048 \times 10^6 = 39.3$ Unit Intervals.

It was therefore expected that the received 2 Mbit/s bit stream from the transmission interface would exhibit up to a 39 UI phase shift on load turn on. Figure I.20 shows the test set-up used to measure this.

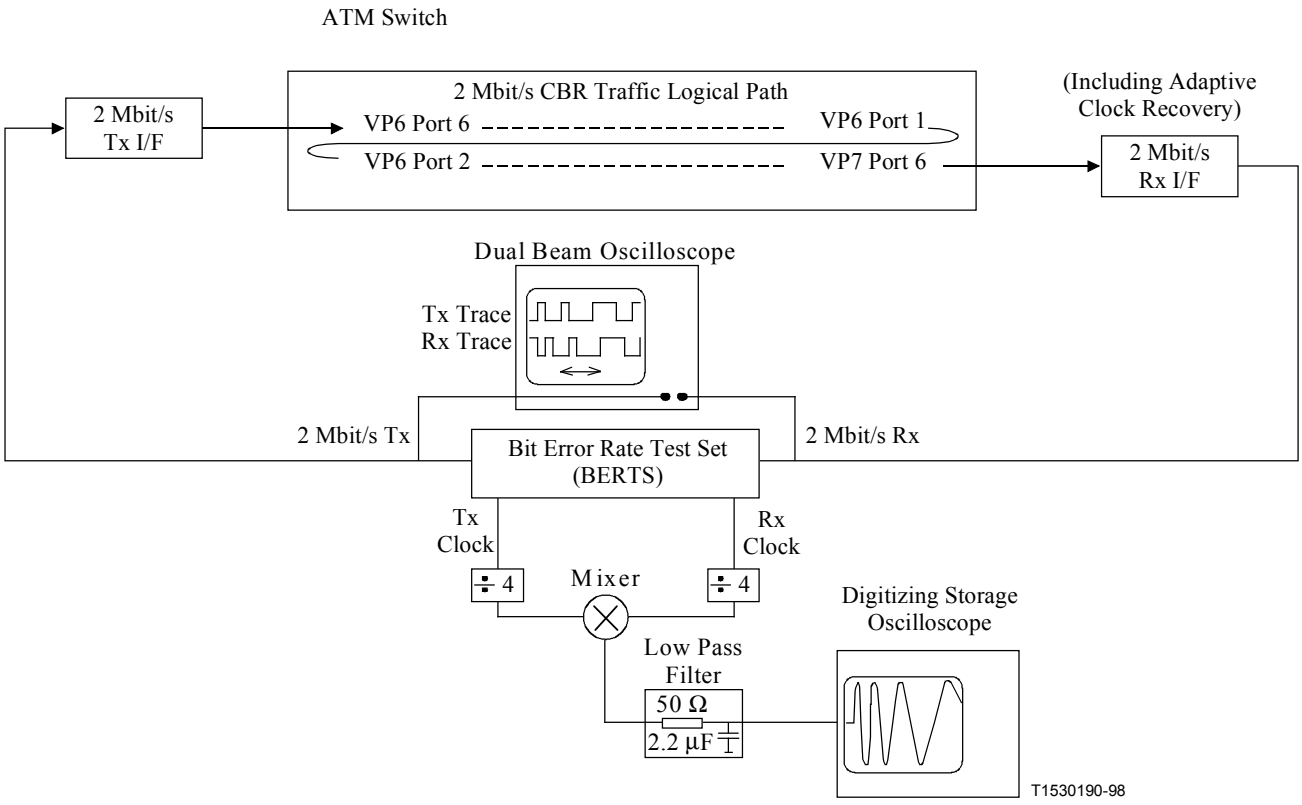


Figure I.20/I.741

The traces shown on the oscilloscopes in the block schematic of Figure I.20 and further depicted in Figures I.6 and I.7, discussed later, show the characteristics observed on load switching.

The "received data" trace on the dual beam oscilloscope (Figure I.20) was seen to track both right and left relative to the "transmit data" trace as the background Poisson load was turned on and off, highlighting the induced phase change in the receive clock. The question is how many clock cycles does the receive clock move by relative to the transmit clock? (i.e. what is the induced peak to peak phase wander due to network load change?).

In order to calculate the magnitude and rate of phase change induced by a changing network load the characteristic depicted on the lower digitizing storage oscilloscope (shown in Figure I.20) was measured. Here the reference transmit clock from a measurement equipment BERTS set is mixed with the received clock. The mixer produces a single output cycle for each clock cycle traversed by the receive clock relative to the reference transmit clock. Thus, the induced phase wander in the 2 Mbit/s receive clock can be measured simply by counting the number of cycles output from the mixer and measured on the oscilloscope on load switch-on. Better still, by plotting the increasing periodicity of the mixer output waveform the rate of change and thus time constant of the adaptive clock recovery mechanism can be estimated and compared with the predicted response in Figure I.15 b).

I.3.3.2 Measurement results

- **Embedded 2 Mbit/s CBR stream from the broadband tester**

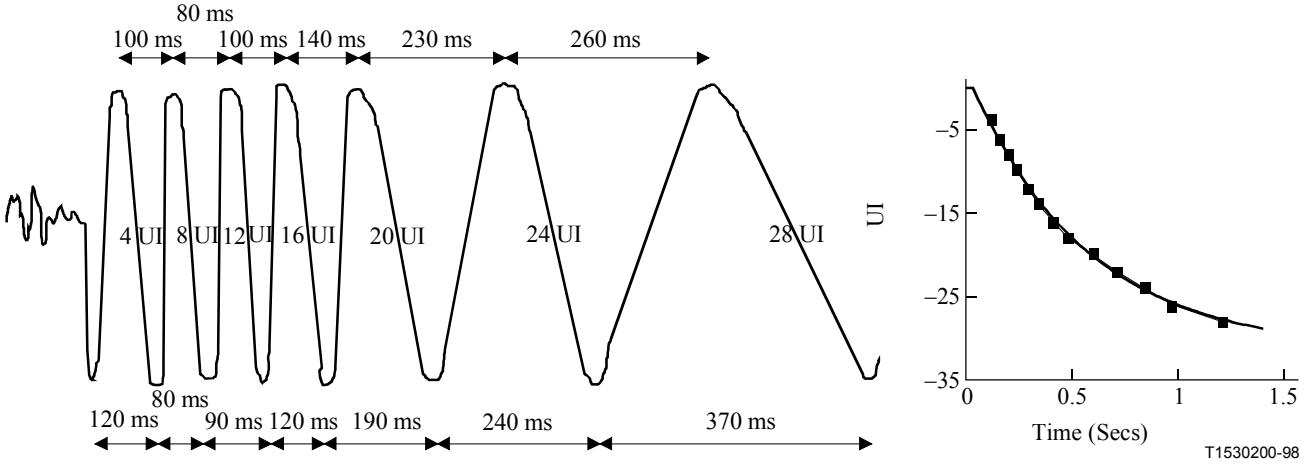
The delay characteristics of the embedded 2 Mbit/s CBR stream generated by the Broadband tester were measured using the broadband tester with the Poisson background load both on and off. The results were as follows:

	2 Mbit/s Delay (μs)		
	Min	**Mean**	**Max**
Poisson 18.1% Background load off	141.1	143.85	150.1
Poisson 18.1% Background load on	140.1	160.99	287.1
Difference in Mean Delay (μs)		17.14	

The difference in Mean Delay in clock cycles (Unit Intervals) at 2.048 MHz = $17.14 \times 10^{-6} \times 2.048 \times 10^{6} = 35$ UI which compares reasonably with that given by the worst case M/D/1 queuing model of 39 UI.

- **Direct measurement results of the 2 Mbit/s receive clock**

The dual beam oscilloscope traces of Figure I.20 were found to indicate clock wander in the order of 1 UI peak to peak from the 2 Mbit/s receive clock even in the absence of contending network load. This meant that the background phase noise itself would produce peak to peak output from the mixer which would obscure the expected mixer output measurement traces during load switching. It was therefore decided to include clock dividers (divide-by-four) prior to the mixer to reduce this background phase noise to below 1 UI/4 = 0.25 UI peak to peak thus ensuring a much lower "noise" output from the mixer. Given the presence of the dividers, for every 4 cycles (UI) of phase wander from the received network clock a single "sinusoidal" cycle should now be expected from the mixer output. The measurement trace resulting from switch on of the background load is depicted in Figure I.21.

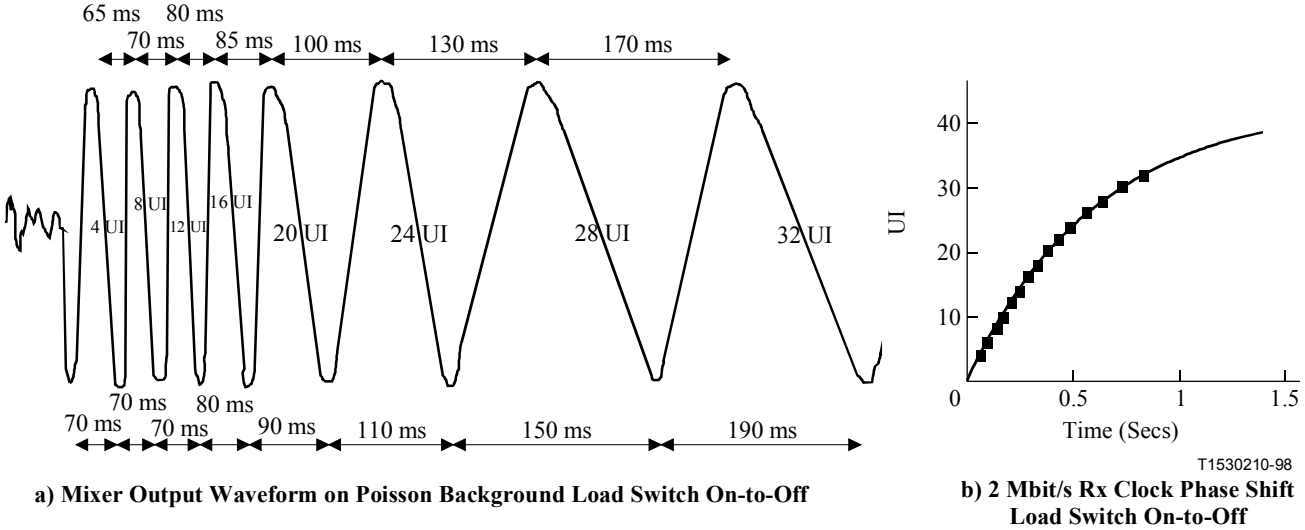


a) Mixer Output Waveform on Poisson Background Load Switch Off-to-On

b) 2 Mbit/s Rx Clock Phase Shift Load Switch Off-to-On

Figure I.21/I.741

The trace resulting from load switch off is depicted in Figure I.22.



a) Mixer Output Waveform on Poisson Background Load Switch On-to-Off

b) 2 Mbit/s Rx Clock Phase Shift Load Switch On-to-Off

Figure I.22/I.741

The total number of cycles in the mixer output waveform on load switch on was 7 and on load switch off was 8. We can therefore estimate that the increase in network load causes an approximately $8 \times 4 = 32$ UI phase wander. This compares well with the delay measurement of the 2 Mbit/s background load given the uncertainty of up to 8 UI caused by the use of the clock dividers and the response of the adaptive clock to rms rather than mean delay.

The time constant of the adaptive clock can be estimated from Figures I.21 b) and I.22 b) as approximately 0.8 s which compares well with the simulation result of Figure I.15 b).

This result shows that, as expected, the output phase of the 2 Mbit/s receive clock directly tracks slow delay changes due to network load. In the case measured the phase was shown to change by ~32 UI (clock cycles) for a load increase from ~zero to 93.2%.

I.3.3.3 Wander limits

The limit for long-term phase wander for a 2 Mbit/s PDH CBR stream, as defined by G.823, is 36.9 UI at 1.2×10^{-5} Hz (daily wander limit) down to 18 UI between 0.01 Hz and 1.667 Hz. Given any change in network load with periodicity greater than the time constant of the adaptive clock's phase locked loop the receive clock phase will directly track the rms switch delay. Thus, for example, assuming in the worst case the network load changes by 93.2% over a period of, say, one minute the receive clock phase would change by ~32 UI against a downstream equipment tolerance limit of only 18 UI. Worse still, not all of this tolerance limit could be apportioned to the ATM network. It seems likely therefore that for a network comprising a number of ATM switches passing through busy hours and idle periods that excessive wander, beyond the G.823 limits, will be exhibited by the exiting CBR cell stream.

I.3.3.4 Jitter limits

The jitter limit for a 2 Mbit/s PDH CBR stream, as defined by G.823, is 1.5 UI peak-to-peak between 20 Hz and 100 kHz. The amount of jitter above 20 Hz is limited by the rate of change allowed by the adaptive clock's phase locked loop. The amount of jitter that could be imparted by a network load step change from ~0 to 93.2% can be estimated by passing the measured responses of Figure I.21 b) and I.7 b) through a 20 Hz highpass filter. The results for Figures I.21 b) "Load Switched On" and I.22 b) "Load Switched off" are shown in Figure I.23.

Here the measured characteristic has been fitted to an exponential and the curve fit subjected to 20 Hz high pass filtering. The result is a peak to peak jitter of about 1.3 unit interval. While this is less than the limit of 1.5 unit interval, it is probably an excessive amount of jitter from a single source, since it will combine with jitter from other sources.

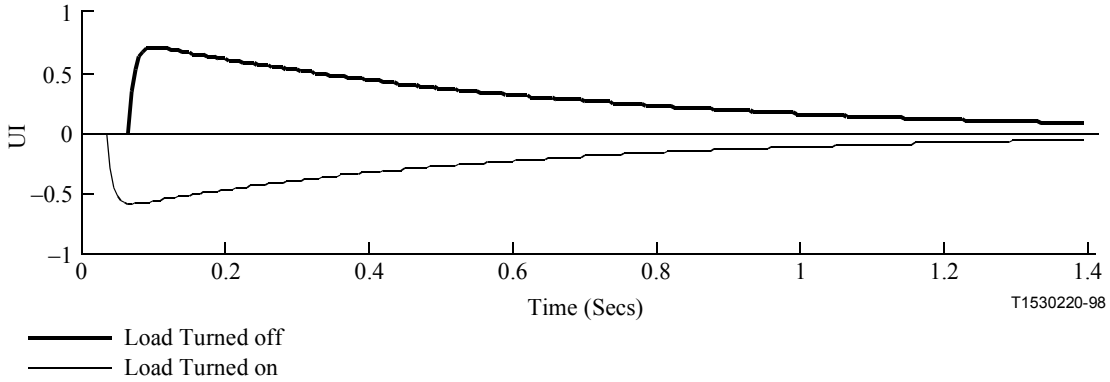


Figure I.23/I.741 – Jitter above 20 Hz

The measurements performed on the ATM switch and 2 Mbit/s CBR transmission interface show that, for a single priority queue output port switch, the long-term phase of the 2 Mbit/s CBR output stream will follow the slow delay changes of the switch queue caused by varying network load. Given that the limits in G.823 for 2 Mbit/s wander lie between 36.9 UI and 18 UI, it appears impossible to guarantee such limits when using a single priority queue in association with adaptive clock recovery. This is particularly so where the CBR streams are made to contend with large bursty data loads, and the fact that not all of the downstream equipment wander tolerance limit can be apportioned to the ATM network. Thus any downstream equipment which relies on the G.823 limits for wander being met could not be connected through such an ATM switch and adaptive clock recovery configuration and be guaranteed compliant wander behaviour.

It may be possible to reduce excessive wander by use of a separate priority queue for CBR cell streams. For example, in the case considered where only one CBR stream exists, if this were to be serviced by a separate priority output buffer it would suffer little CDV and thus cause virtually no wander at the output of the adaptive clock circuit. However, even here further study is required since the effects of waiting time jitter, effects of dissimilar CBR rate contention at higher CBR loads and contention with real time VBR video traffic, if placed in same buffer, would need to be studied.

In the absence of such studies the Synchronous Residual Time Stamp (SRTS) method of timing delivery or network synchronous operation remain the preferred options for timing delivery of CBR services which require compliance with G.823 jitter and wander requirements.

The recommendation here is that when single priority switch buffers are used in conjunction with adaptive clock recovery for delivering CBR streams that the CBR streams be used only for wander insensitive services.

When considering the use of adaptive clock recovery for any specific service the following characteristics need to be accounted for in the design.

a) The transmitting service clock parameters including frequency, tolerance and slew rate.

b) The CDV temporal and spectral characteristics which will be imposed on the service cell stream by the ATM network(s) it traverses. Including the effects of port contention and waiting time jitter.

c) The phase transfer function associated with the adaptive clock recovery mechanism.

d) The jitter/wander tolerance of the specific service being carried.

The adaptive clocking mechanism needs to be able to track any changes of the transmitting service clock within its given bounds of tolerance and slew rate, whilst at the same time not tracking changes implied erroneously by CDV within the network. By default CDV will impart some fluctuations to the recovered clock dependant on the magnitude of the CDV within the network and the CDV to received service clock jitter/wander transfer function of the adaptive clocking mechanism. However, the design must ensure that the ensuing phase variations are within the bounds of the service specific jitter/wander tolerance specifications.

I.4 Echo canceller phase noise requirements

More information is required on echo canceller tolerance to phase noise. However, it seems likely that, given either Network Synchronous or SRTS operation within the ATM echo tail, the performance of the echo canceller will remain unimpaired.

Further study is needed on the effects of adaptive clock recovery techniques and the resultant phase wander effects on echo cancellers. Until more work has been done in this area, it is difficult to say whether the performance of echo cancellers in the presence of adaptive clock recovery in the ATM echo tail will be impaired.

I.5 Conclusions

This appendix has briefly introduced the characteristics of cell delay variation within an ATM network and the effect of this on play-out buffer operation and dimensioning. It has also shown the effect of cell delay variation on relative clock quality when Network Synchronous or Synchronous Residual Time Stamp (SRTS) methods are used to synchronize the transmitter and receiver clocks.

It is recommended that where possible either of these two techniques are adopted to minimize phase noise effects when interworking with echo cancellers.

However, recognizing that both techniques require the delivery of a relatively pure reference clock to both ends of the ATM network, and that in some instances this may not be possible – the use of adaptive timing may be considered provided that the residual phase wander is within the bounds of the echo canceller's phase noise tolerance. Further work is needed to check whether adaptive clock recovery techniques and the resultant residual phase wander will be compatible with echo canceller operation.

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