INTERNATIONAL TELECOMMUNICATION UNION

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.826
(02/99)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital transmission systems – Digital networks – Quality and availability targets

---

Error performance parameters and objectives for international, constant bit rate digital paths at or above the primary rate

ITU-T Recommendation G.826

(Previously CCITT Recommendation)

ITU-T G-SERIES RECOMMENDATIONS

TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS	G.100–G.199
INTERNATIONAL ANALOGUE CARRIER SYSTEM	
GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS	G.200–G.299
INDIVIDUAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON METALLIC LINES	G.300–G.399
GENERAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON RADIO-RELAY OR SATELLITE LINKS AND INTERCONNECTION WITH METALLIC LINES	G.400–G.449
COORDINATION OF RADIOTELEPHONY AND LINE TELEPHONY	G.450–G.499
TESTING EQUIPMENTS	
TRANSMISSION MEDIA CHARACTERISTICS	G.600–G.699
DIGITAL TRANSMISSION SYSTEMS	
TERMINAL EQUIPMENTS	G.700–G.799
DIGITAL NETWORKS	G.800–G.899
General aspects	G.800–G.809
Design objectives for digital networks	G.810–G.819
Quality and availability targets	**G.820–G.829**
Network capabilities and functions	G.830–G.839
SDH network characteristics	G.840–G.849
Telecommunications management network	G.850–G.859
DIGITAL SECTIONS AND DIGITAL LINE SYSTEM	G.900–G.999

For further details, please refer to ITU-T List of Recommendations.

ITU-T RECOMMENDATION G.826

ERROR PERFORMANCE PARAMETERS AND OBJECTIVES FOR INTERNATIONAL, CONSTANT BIT RATE DIGITAL PATHS AT OR ABOVE THE PRIMARY RATE

Summary

This Recommendation defines error performance parameters and objectives for international digital paths which operate at or above the primary rate. The objectives given are independent of the physical network supporting the path. This Recommendation is based upon a block-based measurement concept using error detection codes inherent to the path under test. This simplifies in-service measurements. The parameters and objectives are defined accordingly.

Annexes A, B, C and D deal with the definition of availability of the path and give specific information concerning PDH, SDH and cell-based transmission paths.

Source

ITU-T Recommendation G.826 was revised by ITU-T Study Group 13 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 15th of February 1999.

Keywords

Background block error, block-based concept, digital path, error detection codes, error performance objectives, error performance parameters, errored second, in-service measurements, severely errored second.

FOREWORD

ITU (International Telecommunication Union) is the United Nations Specialized Agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the ITU. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation the term *recognized operating agency (ROA)* includes any individual, company, corporation or governmental organization that operates a public correspondence service. The terms *Administration*, *ROA* and *public correspondence* are defined in the *Constitution of the ITU (Geneva, 1992)*.

INTELLECTUAL PROPERTY RIGHTS

The ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. The ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, the ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

CONTENTS

Page

Page

Recommendation G.826

ERROR PERFORMANCE PARAMETERS AND OBJECTIVES FOR INTERNATIONAL, CONSTANT BIT RATE DIGITAL PATHS AT OR ABOVE THE PRIMARY RATE

(revised in 1999)

1 Scope

This Recommendation specifies error performance events, parameters and objectives for digital paths operating at bit rates at or above the primary rate. Subclauses 1.1 to 1.3 give further details.

1.1 Application of this Recommendation

This Recommendation is applicable to international, constant bit rate digital paths at or above the primary rate. These paths may be based on a Plesiochronous Digital Hierarchy, Synchronous Digital Hierarchy or some other transport network such as cell-based. This Recommendation is generic, in that it defines the parameters and objectives for paths independent of the physical transport network providing the paths. Compliance with the performance specification of this Recommendation will, in most cases, also ensure that a 64 kbit/s connection will meet the requirements laid out in Recommendation G.821 [14]. Therefore, this Recommendation is currently the only Recommendation required for designing the error performance of digital paths at or above the primary rate[1]. The performance parameters and definitions applied to paths provided using the ATM layer and the AAL for CBR services (class A, Recommendation I.362 [17]) are for further study. In accordance with the definition of a digital path, path end points may be located at user's premises.

Since the performance objectives are intended to satisfy the needs of the digital network, it must be recognised that such objectives cannot be readily achieved by all of today's digital equipment and systems. The intent, however, is to encourage equipment design such that digital paths will satisfy the objectives in this Recommendation.

Paths are used to support services such as circuit switched, packet switched and leased circuit services. The quality of such services, as well as the performance of the network elements belonging to the service layer, is outside of the scope of this Recommendation.

The performance objectives are applicable to a single direction of the path. The values apply end-to-end over a 27 500 km Hypothetical Reference Path (see Figure 3) which may include optical fibre, digital radio relay, metallic cable and satellite transmission systems. The performance of multiplex and cross-connect functions employing ATM techniques is not included in these values.

The parameter definitions are block-based, making in-service measurement convenient. In some cases, the network fabric is not able to provide the basic events necessary to directly obtain the performance parameters. In these cases, compliance with this Recommendation can be assessed using out-of-service measurements or estimated by measures compatible with this Recommendation, such as those specified in Annexes B, C and D.

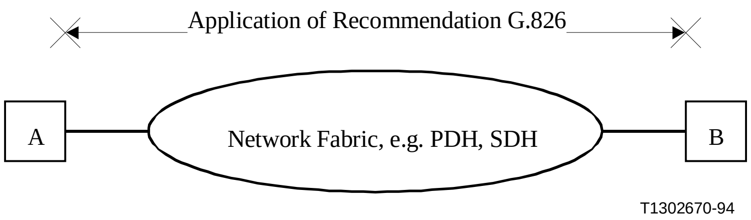
[1] A new Recommendation dealing specifically with performance of SDH paths is currently under development.

1.2 Transport network layers

This Recommendation specifies the error performance of paths in a given transport network layer. Two cases have to be considered:

1.2.1 PDH and SDH transport networks

Figure 1 gives the intended scope where ATM does not form part of the end-to-end path. It should be noted that end-to-end performance monitoring is only possible if the monitored blocks together with the accompanying overhead are transmitted transparently to the path end points.

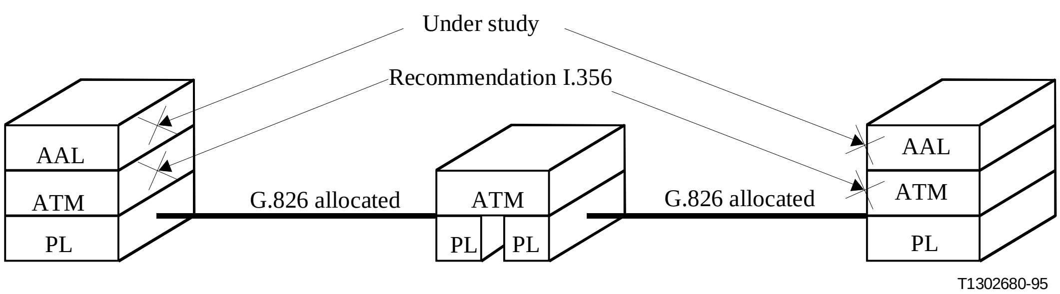


NOTE – A and B are path end points located at physical interfaces, e.g. in accordance with Recommendation G.703 [1].

Figure 1/G.826 – Application of Recommendation G.826 for a non-ATM end-to-end transmission path

1.2.2 ATM connections

Where the path forms the physical part of an ATM connection (see Figure 2), the overall end-to-end performance of the ATM connection is defined by Recommendation I.356 [16]. In this case, this Recommendation can be applied with an appropriate allocation to the performance between the path end points where the physical layer of the ATM protocol reference model (see Recommendation I.321 [15]) is terminated by ATM cross-connects or switches. ATM transmission paths in the physical layer correspond to a stream of cells mapped either into a cell-based format or into SDH or PDH-based frame structures.



AAL ATM Adapatation Layer
ATM ATM Layer
PL Physical Layer

Figure 2/G.826 – Architectural relationship between Recommendations G.826 and I.356 [16]

1.3 Allocation of end-to-end performance

Allocations of end-to-end performance of CBR paths are derived using the rules laid out in 7.2 which are length- and complexity-based. Detailed allocations of G.826 performance to the individual components (lines, sections, multiplexers and cross-connects, etc.) are outside the scope of this Recommendation, but when such allocations are performed, the national and international allocations as given in 7.2 shall be achieved.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation G.703 (1998), *Physical/electrical characteristics of hierarchical digital interfaces*.

[2] ITU-T Recommendation G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels.*

[3] ITU-T Recommendation G.707 (1996), *Network node interface for the Synchronous Digital Hierarchy (SDH).*

[4] CCITT Recommendation G.732 (1988), *Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s*.

[5] CCITT Recommendation G.733 (1988), *Characteristics of primary PCM multiplex equipment operating at 1544 kbit/s*.

[6] CCITT Recommendation G.734 (1988), *Characteristics of synchronous digital multiplex equipment operating at 1544 kbit/s*.

[7] CCITT Recommendation G.742 (1988), *Second order digital multiplex equipment operating at 8448 kbit/s and using positive justification*.

[8] CCITT Recommendation G.743 (1988), *Second order digital multiplex equipment operating at 6312 kbit/s and using positive justification*.

[9] CCITT Recommendation G.751 (1988), *Digital multiplex equipments operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification*.

[10] CCITT Recommendation G.752 (1980), *Characteristics of digital multiplex equipments based on a second order bit rate of 6312 kbit/s and using positive justification*.

[11] CCITT Recommendation G.755 (1988), *Digital multiplex equipment operating at 139 264 kbit/s and multiplexing three tributaries at 44 736 kbit/s*.

[12] ITU-T Recommendation G.775 (1998), *Loss of Signal (LOS), Alarm Indication Signal (AIS) and Remote Defect Indication (RDI) defect detection and clearance criteria for PDH signals*.

[13] ITU-T Recommendation G.783 (1997), *Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks.*

[14] ITU-T Recommendation G.821 (1996), *Error performance of an international digital connection operating at a bit rate below the primary rate and forming part of an integrated services digital network*.

[15] CCITT Recommendation I.321 (1991), *B-ISDN protocol reference model and its application*.

[16] ITU-T Recommendation I.356 (1996), *B-ISDN ATM layer cell transfer performance*.

[17] ITU-T Recommendation I.362[2], *B-ISDN ATM Adaptation Layer (AAL) functional description*.

[18] ITU-T Recommendations I.432.x series, *B-ISDN User-network interface – Physical layer specification*.

[19] ITU-T Recommendation I.610 (1995), *B-ISDN operation and maintenance principles and functions*.

[20] ITU-T Recommendation M.60 (1993), *Maintenance terminology and definitions*.

[21] ITU-T Recommendation M.2100 (1995), *Performance limits for bringing-into-service and maintenance of international PDH paths, sections and transmission systems*.

[22] ITU-T Recommendation M.2101 (1997), *Performance limits for bringing-into-service and maintenance of international SDH paths and multiplex sections*.

3 Abbreviations

This Recommendation uses the following abbreviations:

AAL	ATM Adaptation Layer
AIS	Alarm Indication Signal
ATM	Asynchronous Transfer Mode
AU	Administrative Unit
BBE	Background Block Error
BBER	Background Block Error Ratio
B-ISDN	Broadband ISDN
BIP	Bit Interleaved Parity
CBR	Constant Bit Rate
CEC	Cell Error Control
CRC	Cyclic Redundancy Check
EB	Errored Block
EDC	Error Detection Code
ES	Errored Second
ESR	Errored Second Ratio
FAS	Frame Alignment Signal
HEC	Header Error Check
HP	Higher Order Path

[2] Withdrawn in June 1997.

HRP	Hypothetical Reference Path
IG	International Gateway
ISM	In-Service Monitoring
ISDN	Integrated Services Digital Network
LOF	Loss of Frame Alignment
LOM	Loss of Multiframe Alignment
LOP	Loss Of Pointer
LOS	Loss Of Signal
LP	Lower order Path
MS	Multiplex Section
N-ISDN	Narrow Band ISDN
NTE	Network Terminal Equipment
OAM	Operation and Maintenance
OOS	Out-of-Service
PDH	Plesiochronous Digital Hierarchy
PEP	Path End Point
PL	Physical Layer
RDI	Remote Defect Indication
REI	Remote Error Indication
SDH	Synchronous Digital Hierarchy
SES	Severely Errored Second
SESR	Severely Errored Second Ratio
STM	Synchronous Transport Module
TE	Terminal Equipment
TIM	Trace Identifier Mismatch
TP	Transmission Path
TU	Tributary Unit
UAS	Unavailable Second
UNEQ	Unequipped (defect)
VC	Virtual Container

4 Terms and Definitions

This Recommendation defines the following terms:

4.1 hypothetical reference path: A Hypothetical Reference Path (HRP) is defined as the whole means of digital transmission of a digital signal of specified rate including the path overhead (where it exists) between equipment at which the signal originates and terminates. An end-to-end Hypothetical Reference Path spans a distance of 27 500 km.

4.2 digital paths: A digital path may be bidirectional or unidirectional and may comprise both customer owned portions and network operator owned portions.

4.2.1 PDH digital paths: With regard to PDH digital paths, Recommendation M.60 applies [20].

4.2.2 SDH digital paths: An SDH digital path is a trail carrying the SDH payload and associated overhead through the layered transport network between the terminating equipment.

4.2.3 Cell-based digital paths

Under study.

4.3 Generic definition of the block

This Recommendation is based upon the error performance measurement of blocks. This subclause offers a generic definition of the term "block" as follows[3]:

A block is a set of consecutive bits associated with the path; each bit belongs to one and only one block. Consecutive bits may not be contiguous in time.

Table 1 specifies the recommended range of the number of bits within each block for the various bit rate ranges. Annexes B, C and D contain information on block sizes of existing system designs.

4.4 Error performance events[4]

- **Errored Block (EB)**: A block in which one or more bits are in error.
- **Errored Second (ES)**: A one-second period with one or more errored blocks or at least one defect.
- **Severely Errored Second (SES)**: A one-second period which contains ≥30% errored blocks or at least one defect. SES is a subset of ES.

  Consecutive Severely Errored Seconds may be precursors to periods of unavailability, especially when there are no restoration/protection procedures in use. Periods of consecutive Severely Errored Seconds persisting for T seconds, where $2 \leq T < 10$ (some Network Operators refer to these events as "failures"), can have a severe impact on service, such as the disconnection of switched services. The only way this Recommendation limits the frequency of these events is through the limit for the SESR. (See Notes 1 and 2.)

  NOTE 1 – The defects and related performance criteria are listed in the relevant Annexes (B, C or D) for the different network fabrics PDH, SDH or cell-based.

  NOTE 2 – To simplify measurement processes, the defect is used in the definition of SES instead of defining SES directly in terms of severe errors affecting the path. While this approach simplifies the measurement of SES, it should be noted that there may exist error patterns of severe intensity that would not trigger a defect as defined in Annexes B, C and D. Thus, these would not be considered as an SES under this definition. If in the future such severe user-affecting events were found, this definition will have to be studied again.
- **Background Block Error (BBE)**: An errored block not occurring as part of an SES.

4.5 Error performance parameters

Error performance should only be evaluated whilst the path is in the available state. For a definition of the entry/exit criteria for the unavailable state, see Annex A.

- **Errored Second Ratio (ESR)**: The ratio of ES to total seconds in available time during a fixed measurement interval.

---

[3] Appendix II contains information on block error versus bit error measurements.

[4] See Appendix I, which contains a flow chart illustrating the recognition of anomalies, defects, errored blocks, ES and SES.

- **Severely Errored Second Ratio (SESR)**: The ratio of SES to total seconds in available time during a fixed measurement interval.
- **Background Block Error Ratio (BBER)**: The ratio of Background Block Errors (BBE) to total blocks in available time during a fixed measurement interval. The count of total blocks excludes all blocks during SESs.

5 The measurement of the block

5.1 In-service monitoring of blocks

Each block is monitored by means of an inherent Error Detection Code (EDC), e.g. Bit Interleaved Parity or Cyclic Redundancy Check. The EDC bits are physically separated from the block to which they apply. It is not normally possible to determine whether a block or its controlling EDC bits are in error. If there is a discrepancy between the EDC and its controlled block, it is always assumed that the controlled block is in error.

No specific EDC is given in this generic definition but it is recommended that for in-service monitoring purposes, future designs should be equipped with an EDC capability such that the probability to detect an error event is ≥90%, assuming Poisson error distribution. CRC-4 and BIP-8 are examples of EDCs currently used which fulfil this requirement.

Estimation of errored blocks on an in-service basis is dependent upon the network fabric employed and the type of EDC available. Annexes B, C and D offer guidance on how in-service estimates of errored blocks can be obtained from the ISM facilities of the PDH, SDH and cell-based network fabrics respectively.

5.2 Out-of-service measurements of blocks

Out-of-service measurements shall also be block-based. It is expected that the out-of-service error detection capability will be superior to the in-service capability described in 5.1.

6 Performance assessment

6.1 Implications for error performance measuring devices

There is a large number of devices (test equipment, transmission systems, collecting devices, operating systems, software applications) currently designed to estimate the G.821 [14] or M.2100 [21] parameters ESR and SESR at bit rates up to the fourth level of the PDH. For such devices, the G.826 parameters ESR and SESR may be approximated using the G.821 criteria, but an approximation of BBER is not possible from measurements based on Recommendation G.821. As the block-based concept and the BBER parameter are not defined for Recommendation G.821, converting those devices to measure the parameters of this Recommendation is not required.

Maintenance on specific systems and transport paths may require other parameters. Parameters and values can be found in the M-series Recommendations. See, for example, Recommendations M.2100 [21] and M.2101 [22].

6.2 Performance monitoring at the near end and far end of a path

By monitoring SES events for both directions at a single path end point, a network provider is able to determine the unavailable state of the path (see Annex A). In some cases, it is also possible to monitor the full set of error performance parameters in both directions from one end of the path.

Specific in-service indicators for deriving far end performance of a path are listed in Annexes B, C and D.

7 Error performance objectives

7.1 End-to-end objectives

Table 1 specifies the end-to-end objectives for a 27 500 km HRP in terms of the parameters defined in 4.5. The actual objectives applicable to a real path are derived from Table 1 using the allocation principles detailed in 7.2. Each direction of the path shall concurrently satisfy the allocated objectives for all parameters. In other words, a path fails to satisfy this Recommendation if any parameter exceeds the allocated objective in either direction at the end of the given evaluation period. The suggested evaluation period is one month.

NOTE 1 – For the purpose of this Recommendation, a month is understood to be any period of 28 to 31 consecutive 24-hour intervals. To be able to compare measurement results taken by different parties on the same path, start time and duration of the performance evaluation period need to be agreed between the parties concerned.

Table 1/G.826 – End-to-end error performance objectives for a 27 500 km international digital HRP at or above the primary rate

Rate Mbit/s	1.5 to 5	> 5 to 15	> 15 to 55	> 55 to 160	> 160 to 3500
Bits/block	800-5000	2000-8000	4000-20 000	6000-20 000	15 000-30 000 (Note 2)
ESR	0.04	0.05	0.075	0.16	(Note 3)
SESR	0.002	0.002	0.002	0.002	0.002
BBER	2×10^{-4} (Note 1)	2×10^{-4}	2×10^{-4}	2×10^{-4}	10^{-4}

NOTE 1 – For systems designed prior to 1996, the BBER objective 3×10^{-4}.

NOTE 2 – As currently defined, VC-4-4c (Recommendation G.707 [3]) is a 601 Mbit/s path with a block size of 75 168 bits/block. Since this is outside the recommended range for 160-3500 Mbit/s paths, performance on VC-4-4c paths should not be estimated in-service using this table. The BBER objective for VC-4-4c using the 75 168 bit block size is taken to be 4×10^{-4}.

Digital sections are defined for higher bit rates and guidance on evaluating the performance of digital sections can be found in 7.1 and in a Recommendation dealing with multiplex section error performance.

NOTE 3 – ESR objectives tend to lose significance for applications at high bit rates and are therefore not specified for paths operating at bit rates above 160 Mbit/s. Nevertheless, it is recognised that the observed performance of SDH paths is essentially error-free for long periods of time, even at Gigabit rates. Significant ESR indicates a degraded transmission system. Therefore, for maintenance purposes, ES monitoring should be implemented within any error performance measuring devices operating at these rates.

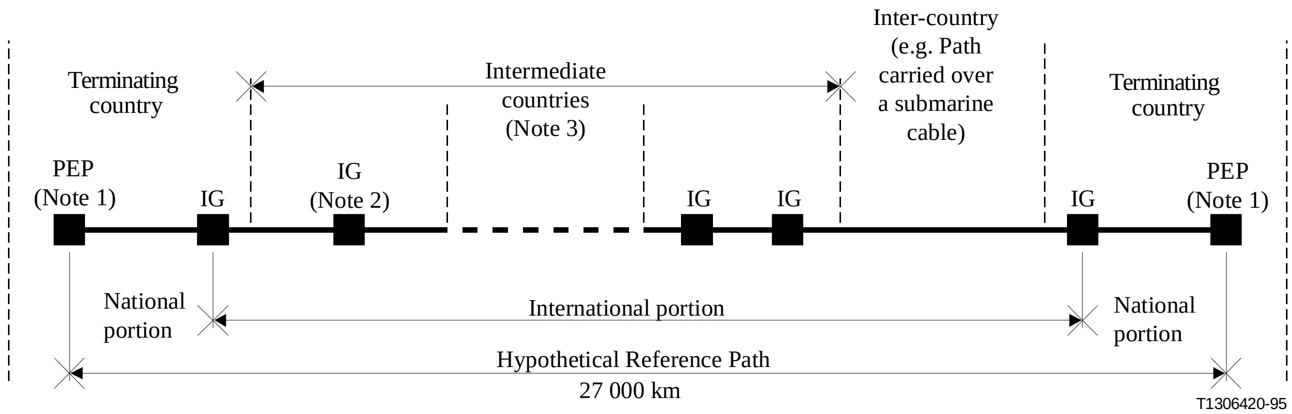
It is noted that SES events may occur in clusters, not always as isolated events. A sequence of "n" contiguous SES may have a very different impact on performance from "n" isolated SES events.

Digital paths operating at bit rates covered by this Recommendation are carried by transmission systems (digital sections) operating at equal or higher bit rates. Such systems must meet their allocations of the end-to-end objectives for the highest bit rate paths which are foreseen to be carried. Meeting the allocated objectives for this highest bit rate path should be sufficient to ensure that all paths through the system are achieving their objective. For example, in SDH, an STM-1 section may carry a VC-4 path and therefore the STM-1 section should be designed such that it will ensure that the objectives as specified in this Recommendation for the bit rate corresponding to a VC-4 path are met.

NOTE 2 – Objectives are allocated in this Recommendation to the national and international portions of a path. In the above example, if the STM-1 section does not form a complete national or international portion, the corresponding national/international allocation must be subdivided to determine the appropriate allocation for the digital section. This is outside the scope of this Recommendation and is covered in a separate Recommendation.

7.2 Apportionment of end-to-end objectives

The following apportionment methodology specifies the levels of performance expected from the national and international portions of an HRP. Further subdivision of these objectives is beyond the scope of this Recommendation. (See Figure 3.)



NOTE 1 – If a path is considered to terminate at the IG, only the international portion allocation applies.
NOTE 2 – One or two international Gateways (entry or exit) may be defined per intermediate country.
NOTE 3 – Four intermediate countries are assumed.

Figure 3/G.826 – Hypothetical Reference Path

For the purposes of this Recommendation, the boundary between the national and international portions is defined to be at an International Gateway which usually corresponds to a cross-connect, a higher-order multiplexer or a switch (N-ISDN or B-ISDN). IGs are always terrestrially based equipment physically resident in the terminating (or intermediate) country. Higher-order paths (relative to the HRP under consideration) may be used between IGs. Such paths receive only the allocation corresponding to the international portion between the IGs. In intermediate countries, the IGs are only located in order to calculate the overall length of the international portion of the path in order to deduce the overall allocation.

The following allocation methodology applies to each parameter defined in 4.5 and takes into account both the length and complexity of the international path. All paths should be engineered to meet their allocated objectives as described in 7.2.1 and 7.2.2. If the overall allocation exceeds 100%, then the performance of the path may not fulfil the objectives of Table 1. Network Operators should note that if performance could be improved in practical implementations to be superior to allocated objectives, the occurrence of paths exceeding the objectives of Table 1 can be minimised.

7.2.1 Allocation to the national portion of the end-to-end path

Each national portion is allocated a fixed block allowance of 17.5% of the end-to-end objective. Furthermore, a distance-based allocation is added to the block allowance. The actual route length between the PEP and IG should first be calculated if known. The air route distance between the PEP and IG should also be determined and multiplied by an appropriate routing factor. This routing factor is specified as follows:

- if the air route distance is <1000 km, the routing factor is 1.5;
- if the air route distance is ≥1000 km and <1200 km, the calculated route length is taken to be 1500 km;
- if the air route distance is ≥1200 km, the routing factor is 1.25.

When both actual and calculated route lengths are known, the smaller value is retained. This distance should be rounded up to the nearest 500 km (i.e. the two national portions comprise at least 500 km each). An allocation of 1% per 500 km is then applied to the resulting distance.

When a national portion includes a satellite hop, a total allowance of 42% of the end-to-end objectives in Table 1 is allocated to this national portion. The 42% allowance completely replaces both the distance-based allowance and the 17.5% block allowance otherwise given to national portions.

NOTE – If a path comprises portions that are privately owned (private in this context means that the network portion is customer owned and not available to the public), end-to-end performance objectives apply to the portion situated between the two Network Terminal Equipment (NTE). Between the NTE and the Terminal Equipment (TE), no specific requirements are given. However, careful attention should be paid concerning this portion because overall performance depends on it. Appendix III contains details for the case of Leased Circuits.

7.2.2 Allocation to the international portion of the end-to-end path

The international portion is allocated a block allowance of 2% per intermediate country plus 1% for each terminating country. Furthermore, a distance-based allocation is added to the block allowance. As the international path may pass through intermediate countries, the actual route length between consecutive IGs (one or two for each intermediate country) should be added to calculate the overall length of the international portion. The air route distance between consecutive IGs should also be determined and multiplied by an appropriate routing factor. This routing factor is specified as follows for each element between IGs:

- if the air route distance between two IGs is <1000 km, the routing factor is 1.5;
- if the air route distance is ≥1000 km and <1200 km, the calculated route length is taken to be 1500 km;
- if the air route distance between two IGs is ≥1200 km, the routing factor is 1.25.

When both actual and calculated route lengths are known, the smaller value is retained for each element between IGs for the calculation of the overall length of the international portion. This overall distance should be rounded up to the nearest 500 km but shall not exceed 26 500 km. An allocation of 1% per 500 km is then applied to the resulting distance.

In the case where the allocation to the international portion is less than 6%, then 6% shall be used as the allocation.

Independent of the distance spanned, any satellite hop in the international portion receives a 35% allocation of the objectives in Table 1. The 35% allowance completely replaces all distance-based and block allowances otherwise given to parts of the international portion spanned by the satellite hop.

ANNEX A

Criteria for entry and exit for the unavailable state

A.1 Criteria for a single direction

A period of unavailable time begins at the onset of ten consecutive SES events. These ten seconds are considered to be part of unavailable time. A new period of available time begins at the onset of ten consecutive non-SES events. These ten seconds are considered to be part of available time. Figure A.1 illustrates this definition.

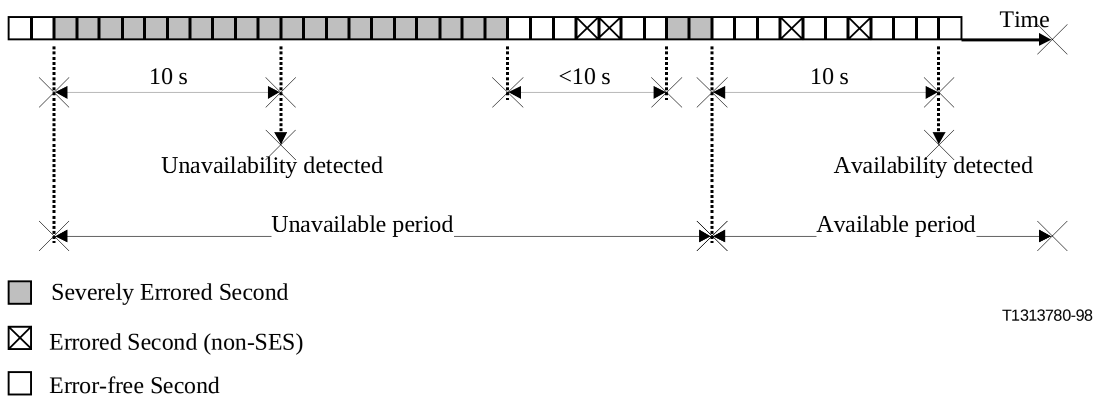


Figure A.1/G.826 – Example of unavailability determination

A.2 Criterion for a bidirectional path

A bidirectional path is in the unavailable state if either one or both directions are in the unavailable state. This is shown in Figure A.2.

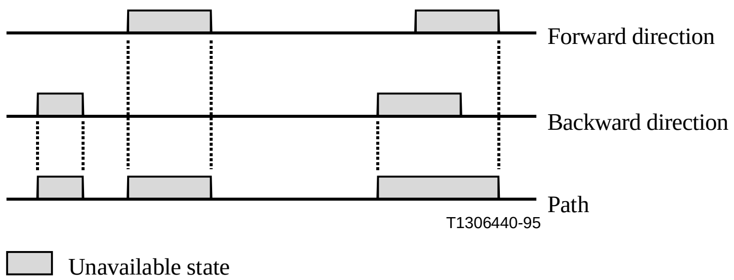


Figure A.2/G.826 – Example of the unavailable state of a path

A.3 Criterion for a unidirectional path

The criterion for a unidirectional path is defined in A.1 above.

A.4 Consequences on error performance measurements

When a bidirectional path is in the unavailable state, ES, SES and BBE counts may be collected in both directions and may be helpful in the analysis of the trouble. However, it is recommended that these ES, SES and BBE counts are not included in estimates of ESR, SESR and BBER performance (see 4.5).

Some existing systems cannot support this requirement to exclude ES, SES and BBE counts. For these systems, the performance of a bidirectional path can be approximated by evaluating the parameters in each direction, independently of the state of availability of the other direction. It should be noted that this approximation method may result in a worse estimate of performance in the event that only on direction of a bidirectional path becomes unavailable.

NOTE – This is not an issue for unidirectional paths.

ANNEX B

Relationship between PDH path performance monitoring and the block-based parameters

B.1 General

B.1.1 Block size for monitoring PDH paths

The block sizes for in-service performance monitoring of PDH paths are given in Table B.1.

Table B.1/G.826 – Block sizes for PDH path performance monitoring

Bit rate of PDH path	Block size according to Table 1	PDH block size used in Rec. G.826	EDC	Reference
1 544 kbit/s	800-5 000 bits	4632 bits	CRC-6	2.1/G.704 [2]
2 048 kbit/s	800-5 000 bits	2048 bits	CRC-4	2.3/G.704
6 312 kbit/s	2 000-8 000 bits	3156 bits	CRC-5	2.2/G.704
44 736 kbit/s	4 000-20 000 bits	4760 bits	Single bit parity check (Note)	1.3/G.752 [10]
NOTE – It shall be noted that single bit parity check does not satisfy the error detection probability of ≥90%.				

B.1.2 Anomalies

In-service anomaly conditions are used to determine the error performance of a PDH path when the path is not in a defect state. The two following categories of anomalies related to the incoming signal are defined:

a_1 an errored frame alignment signal;

a_2 an EB as indicated by an EDC.

B.1.3 Defects

In-service defect conditions are used in the G.730 to G.750 series of Recommendations relevant to PDH multiplex equipment to determine the change of performance state which may occur on a path. The three following categories of defects related to the incoming signal are defined:

d_1 loss of signal;

d_2 alarm indication signal;

d_3 loss of frame alignment.

For the 2 Mbit/s hierarchy, the definition of the LOF defect condition is given in the G.730 to G.750 series of Recommendations.

For some formats of the 1.5 Mbit/s hierarchy, the definition of the LOF defect condition requires further study

For both hierarchies, the definitions of LOS and AIS defect detection criteria are given in Recommendation G.775 [12].

B.2 Types of paths

Depending on the type of in-service monitoring "ISM" facility associated with the PDH path under consideration, it may not be possible to derive the full set of performance parameters. Four types of paths are identified:

Type 1: Frame and block structured paths

The full set of defect indications d_1 to d_3 and anomaly indications a_1 and a_2 are provided by the ISM facilities. Examples of this type of path are:

– Primary rate and second order paths with CRC (4 to 6) as defined in Recommendation G.704 [2].

– Fourth order paths with a parity bit per frame as defined in Recommendation G.755 [11].

Type 2: Frame structured paths

The full set of defect indications d_1 to d_3 and the anomaly indication a_1 are provided by the ISM facilities. Examples of this type of path are:

– Primary rate up to the fourth order paths in the 2 Mbit/s hierarchy as defined in Recommendations G.732 [4], G.742 [7] and G.751 [9].

– Primary rate paths in the 1.5 Mbit/s hierarchy as defined in Recommendations G.733 [5] and G.734 [6].

Type 3: Other frame structured paths

A limited set of defect indications d_1 and d_2 and the anomaly indication a_1 are provided by the ISM facilities. In addition, the number of consecutive errored FAS per second is available. An example of this type of path is:

– Second up to the fourth order paths in the 1.5 Mbit/s hierarchy as defined in Recommendations G.743 [8] and G.752 [10].

Type 4: Unframed paths

A limited set of defect indications d_1 and d_2 is provided by the ISM facilities which do not include any error check. No FAS control is available. An example of this type of path is:

– End-to-end path (e.g. for a leased circuit) carried over several higher order paths placed in tandem.

B.3 Estimation of the performance parameters

Table B.2 gives information on which set of parameters should be estimated and the related measurement criteria according to the type of path considered.

Table B.2/G.826 – Set of parameters and measurement criteria

Type	Set of parameters	Measurement criteria
1	ESR	An ES is observed when, during one second, at least one anomaly a_1 or a_2, or one defect d_1 to d_3 occurs
	SESR	An SES is observed when, during one second, at least "x" anomalies a_1 or a_2, or one defect d_1 to d_3 occurs (Notes 1 and 2)
	BBER	A BBE is observed when an anomaly a_1 or a_2 occurs in a block not being part of an SES
2	ESR	An ES is observed when, during one second, at least one anomaly a_1 or one defect d_1 to d_3 occurs
	SESR	An SES is observed when, during one second, at least "x" anomalies a_1 or one defect d_1 to d_3 occurs (Note 2)
3	ESR	An ES is observed when, during one second, at least one anomaly a_1 or one defect d_1 or d_2 occurs
	SESR	An SES is observed when, during one second, at least "x" anomalies a_1 or one defect d_1 or d_2 occurs (Note 2)
4	SESR	An SES is observed when, during one second, at least one defect d_1 or d_2 occurs (Note 3)
NOTE 1 – If more than one anomaly a_1 or a_2 occur during the block interval, then only one anomaly has to be counted. NOTE 2 – Values of "x" can be found in B.4. NOTE 3 – The estimates of the ESR and SESR will be identical since the SES event is a subset of the ES event.		

B.4 In-service monitoring capabilities and criteria for declaration of the performance parameters

Table B.3 is provided for guidance on the criteria for declaration of an SES event on PDH paths.

The capabilities for the detection of anomalies and defects for the various PDH signal formats are described in Tables B.2/M.2100 to B.6/M.2100 [21]. These tables also indicate the criteria for declaring the occurrence of an ES or a SES condition in accordance with Recommendation G.821 [14] criteria.

While it is recommended that ISM capabilities of future systems be designed to permit performance measurements in accordance with this Recommendation, it is recognised that it may not be practical to change equipment already installed and/or designed in accordance with Recommendation G.821 [14] or the 1996 version of Recommendation G.826.

Table B.3 lists examples of the ISM SES criteria x, for signal formats with EDC capabilities, implemented prior to this Recommendation.

Table B.3/G.826 – Criteria for declaration of an SES event on PDH paths

Bit rate (kbit/s)	1544	2048	44 736
Recommendation	G.704 [2]	G.704 [2]	G.752 [10]
EDC type	CRC-6	CRC-4	Single bit parity check
Blocks/second	333	1000	9398
Bits/block	4632	2048	4760
SES threshold used on equipment developed prior to the acceptance of Recommendation G.826	x = 320 (Note 2)	x = 805 (Note 2)	x = 45 or x = 2444 as suggested in Rec. M.2100 [21]
ISM threshold based on Recommendation G.826 SES (30% errored blocks)	x = 100 (Note 3)	x = 300 (Note 3)	x = 2444 (Note 4)

NOTE 1 – It is recognised that there are discrepancies between the figures above and those given in Table B.1. This requires further study.

NOTE 2 – Applicable to installations in accordance with Recommendation G.821 [14] or the 1996 version of Recommendation G.826 and where compatibility with these installations is required.

NOTE 3 – Preferred option for new installations.

NOTE 4 – This figure takes into account the fact that, although 30% of the blocks could contain errors, a smaller value will be detected by the EDC due to the inability of the simple parity code to detect even numbers of errors in a block. It should be noted that such a simple EDC is non-compliant with the intent of Recommendation G.826.

NOTE 5 – Completion of this table for other bit rates is for further study.

B.5 Estimation of performance events at the far end of a path

The available remote in-service indications such as RDI or, if provided, REI are used at the near end to estimate the number of SES occurring at the far end.

B.6 Differences between Recommendations G.826 and M.2100 concerning path performance

B.6.1 General

When looking at the differences between Recommendations G.826 and M.2100 [21], it shall be taken into account that the two Recommendations serve a different purpose and can therefore not be compatible in all respects. Recommendation M.2100 [21] is a maintenance Recommendation which also allows short-term measurements. It can be used to indicate that the long-term requirements of Recommendation G.826 are met.

B.6.2 Allocation methodology

The allocation methodology used in Recommendation G.826 differs from the methods applied in Recommendation M.2100 [21]. Though there are differences, in most cases the requirements of Recommendation G.826 are satisfied if the objectives of Recommendation M.2100 [21] are met.

With regard to the purpose of the intermediate IGs depicted in Figure 3, it shall be noted that they are required to calculate route length.

ANNEX C

Relationship between SDH path performance monitoring and the block-based parameters

C.1 General

C.1.1 Converting BIP measurements into errored blocks

Subclause 4.4 describes error performance events used in defining performance parameters. The method of converting BIP measurements into errored blocks is described below.

Since this Recommendation defines a block as consecutive bits associated with a path, each BIP-n (Bit Interleaved Parity, order "n") in the SDH path overhead pertains to a single defined block. For the purpose of this Annex, a BIP-n corresponds to a G.826 block. The BIP-n is NOT interpreted as checking "n" separate interleaved parity check blocks. If any of the "n" separate parity checks fails, the block is assumed to be in error.

NOTE – It shall be noted that BIP-2 does not satisfy the error detection probability of ≥90%.

C.1.2 Block size for monitoring SDH paths

The block sizes for in-service performance monitoring of SDH paths as specified in Recommendation G.707 [3] are given in Table C.1.

Table C.1/G.826 – Block sizes for SDH path performance monitoring

Bit rate of SDH path	Path type	Block size according to Table 1	SDH block size used in G.826	EDC
1664 kbit/s	VC-11	800-5 000 bits	832 bits	BIP-2
2240 kbit/s	VC-12	800-5 000 bits	1 120 bits	BIP-2
6848 kbit/s	VC-2	2 000-8 000 bits	3 424 bits	BIP-2
48 960 kbit/s	VC-3	4 000-20 000 bits	6 120 bits	BIP-8
150 336 kbit/s	VC-4	6 000-20 000 bits	18 792 bits	BIP-8
$m \times 6848$ kbit/s	VC-2-mc (Note 1)		3 424 bits	$m \times$ BIP-2
34 240 kbit/s	VC-2-5c (Note 2)	6 000-20 000 bits	17 120 bits	BIP-2
601 344 kbit/s	VC-4-4c	15 000-30 000 bits	75 168 bits	BIP-8

NOTE 1 – Applies to virtual concatenation.

NOTE 2 – Applies to contiguous concatenation.

C.1.3 Anomalies

In-service anomaly conditions are used to determine the error performance of an SDH path when the path is not in a defect state. The following anomaly is defined:

a_1 an EB as indicated by an EDC (see C.1.1).

C.1.4 Defects

In-service defect conditions are used in Recommendations G.707 [3] and G.783 [13] relevant to SDH equipment to determine the change of performance state which may occur on a path. Tables C.2 and C.3 show the defects used in this Recommendation.

Table C.2/G.826 – Defects resulting in a near-end severely errored second

<table>
<tr><th>Near end defects</th><th>Kind of path</th></tr>
<tr><td>LP UNEQ</td><td rowspan="6">Applicable to
lower order paths</td></tr>
<tr><td>LP TIM</td></tr>
<tr><td>TU LOP</td></tr>
<tr><td>TU AIS</td></tr>
<tr><td>HP LOM (Note 1)</td></tr>
<tr><td>HP PLM</td></tr>
<tr><td>HP UNEQ</td><td rowspan="4">Applicable to
higher order paths</td></tr>
<tr><td>HP TIM</td></tr>
<tr><td>AU LOP</td></tr>
<tr><td>AU AIS</td></tr>
<tr><td colspan="2">NOTE 1 – This defect is not related to VC-3.
NOTE 2 – VC AIS defect is not included above as it only applies to a segment of a path.
NOTE 3 – The above defects are path defects only. Section defects such as MS AIS, RS TIM, STM LOF and STM LOS give rise to an AIS defect in the path layers.
NOTE 4 – When a near-end SES is caused by a near-end defect as defined above, the far-end performance event counters are not incremented, i.e. an error-free period is assumed. When a near-end SES is resulting from ≥30% errored blocks, the far-end performance evaluation continues during the near-end SES.
This approach does not allow reliable evaluation of far-end data if the near-end SES is caused by a defect. It should be noted in particular, that the evaluation of far-end events (such as SES or Unavailability) can be inaccurate in the case where far-end SESs occur in coincidence with near-end SESs caused by a defect. Such inaccuracies cannot be avoided, but are negligible in practice because of the low probability of the occurrence of such phenomena.</td></tr>
</table>

Table C.3/G.826 – Defects resulting in a far-end severely errored second

Far-end defects	Kind of path
LP RDI	Applicable to lower order paths
HP RDI	Applicable to higher order paths

C.1.5 Measurement of performance events using aggregate parity error counts

This subclause offers guidance for equipment designed to sum individual Bit Interleaved Parity violations over the entire second instead of using the BIP-n block to detect and count errored blocks as recommended in C.1.1. The following text should not be interpreted as a basis for future equipment design.

Aggregate counts of Bit Interleaved Parity (BIP) violations can be used to estimate the number of G.826 errored blocks. As a simplifying assumption, the aggregate count of individual Bit Interleaved Parity violations in a second can be taken to be roughly equivalent to the number of G.826 errored blocks in that second. The following relationship is recommended for both BIP-2 and BIP-8, even though it may tend to overestimate errored blocks in case of BIP-8:

$$E \approx P$$

where:

E = number of errored blocks in the measurement period

P = number of individual parity violations in the measurement period

C.2 Estimation of the performance parameters

For SDH transmission paths, the full set of performance parameters shall be estimated using the following events:

ES: An ES is observed when, during one second, at least one anomaly a_1, or one defect according to Tables C.2 and C.3 occurs. For the ES event, the actual count of EBs is irrelevant, it is only the fact that an EB has occurred in a second which is significant.

SES: An SES is observed when, during one second, at least 30% EBs – derived from anomaly a_1 or one defect according to Tables C.2 and C.3 occur (see Note).

BBE: A BBE is observed when an anomaly a_1 occurs in a block not being part of an SES.

NOTE – The errored block threshold resulting in an SES is shown in Table C.4 for each SDH path type.

Table C.4/G.826 – Threshold for the declaration of a severely errored second

Path type	Threshold for SES (Number of errored blocks in one second)
VC-11	600
VC-12	600
VC-2	600
VC-3	2400
VC-4	2400
VC-2-5c	600
VC-4-4c	2400
NOTE – It is recognised that there are discrepancies between the figures above and those given in Table B.3. This requires further study.	

C.3 Estimation of performance events at the far end of a path

The following indications available at the near end are used to estimate the performance events (occurring at the far end) for the reverse direction:

Higher and lower order path RDI and REI (Recommendation G.707 [3]).

Higher or lower order path REIs are anomalies which are used to determine the occurrence of ES, BBE and SES at the far end.

Higher or lower order path RDIs are defects which estimate the occurrence of SES at the far end.

ANNEX D

Relationship between cell-based network performance monitoring and the block-based parameters

D.1 General

D.1.1 Block size for monitoring cell-based paths

The block sizes for in-service performance monitoring of cell-based paths are given in Table D.1.

Table D.1/G.826 – Block sizes for cell-based path performance monitoring

Bit rate for cell-based path	Block size according to Table 1	Number of cells/block (as defined in I.432) [18]	Cell-based block size used in G.826
51 Mbit/s	4 000-20 000	15	6 360 bits
155 Mbit/s	6 000-20 000	27	11 448 bits
622 Mbit/s	15 000-30 000	54	22 896 bits

The operation and maintenance function for the transmission path is provided by the F3 flow as defined in Recommendation I.610 [19] which deals with the general OAM principles for B-ISDN.

The F3 maintenance flow corresponds to the ISM facilities and is defined in Recommendation I.432 [18]. For the 51 Mbit/s cell-based path, each F3 OAM cell monitors 15 cells. For the 155 Mbit/s and the 622 Mbit/s cell-based paths, each F3 OAM cell monitors 8 blocks of 27 (or 54) contiguous cells. The block – as defined in this Recommendation – corresponds to a set of contiguous cells monitored by a BIP-8 EDC. For the purpose of Recommendation G.826, the BIP-8 is not interpreted as checking 8 separate interleaved parity check blocks. One BIP-8 interleaved parity check cannot lead to more than one errored block. Within one BIP-8 check, if any of the 8 separate parity checks fails, the overall block is assumed to be in error.

D.1.2 Anomalies

The following categories of anomalies related to the incoming signal on an ATM transmission path are defined:

a_1 errored payload of an idle or ATM cell (detected by an EDC in the F3 OAM cell) (see Note 1);

a_2 errored or corrected header of an idle or ATM cell;

a_3 corrected F3 cell header;

a_4 loss of a single F3 cell (Note 2) or error detected by the cell error control of a valid F3 cell.

NOTE 1 – An ATM cell is provided by the ATM layer.

NOTE 2 – Loss of a single F3 cell is declared when no valid F3 OAM cell is received x cells after the last valid F3 OAM cells. The value of x is given below.

Applicable bit rate	Value of x
51.840 Mbit/s	14
155.520 Mbit/s	215
622.080 Mbit/s	431

When at least one anomaly a_1 to a_3 occurs in a given block, an Errored Block should be counted. If more than one anomaly occurs for a given block, only one EB is counted. When an a_4 anomaly occurs, all blocks monitored by the F3 OAM cell are errored (1 block for 51 Mbit/s and 8 blocks for the bit rates of 155 and 622 Mbit/s respectively).

D.1.3 Defects

The following categories of defects related to the incoming signal on an ATM transmission path are defined:

d_1 loss of two consecutive OAM cells, in accordance with Recommendation I.432 [18];

d_2 transmission path alarm indication signal (TP-AIS);

d_3 loss of cell delineation;

d_4 loss of signal.

D.2 Types of paths

Two types of ATM transmission paths are identified:

– Type 1: Paths corresponding to a stream of cells mapped in a cell-based format.

– Type 2: Paths corresponding to a stream of cells mapped into SDH or PDH-based frame structures.

The full set of performance parameters of this Recommendation and corresponding objectives is applicable to the ATM transmission path of type 1.

The performance parameters and corresponding objectives are applied to underlying SDH or PDH paths which support ATM transmission paths of type 2.

The applicability of the performance parameters for type 2 ATM transmission paths requires further study.

D.3 Estimation of the performance parameters

For type 1 ATM transmission paths, the full set of G.826 performance parameters should be estimated using the following events:

ES: An ES is observed when, during one second, at least one anomaly a_1 to a_4, or one defect d_1 to d_4 occurs.

SES: An SES is observed when, during one second, at least 30% EBs – derived from anomalies a_1 to a_4 – or one defect d_1 to d_4 occur.

BBE: A BBE is observed when one anomaly a_1 to a_4 occurs in a block not being part of an SES.

D.4 Estimation of performance events at the far end of the path

The TP-RDI defect (see Recommendation I.432 [18]) and REI indications are used at the near end to estimate the G.826 performance events occurring at the far end.

REIs are anomalies which are used to determine the occurrence of ES, BBE and SES at the far end of the path.

TP-RDIs are defects which estimate the occurrence of SES at the far end of the path.

APPENDIX I

Flow chart illustrating the recognition of anomalies, defects, errored blocks, ES and SES

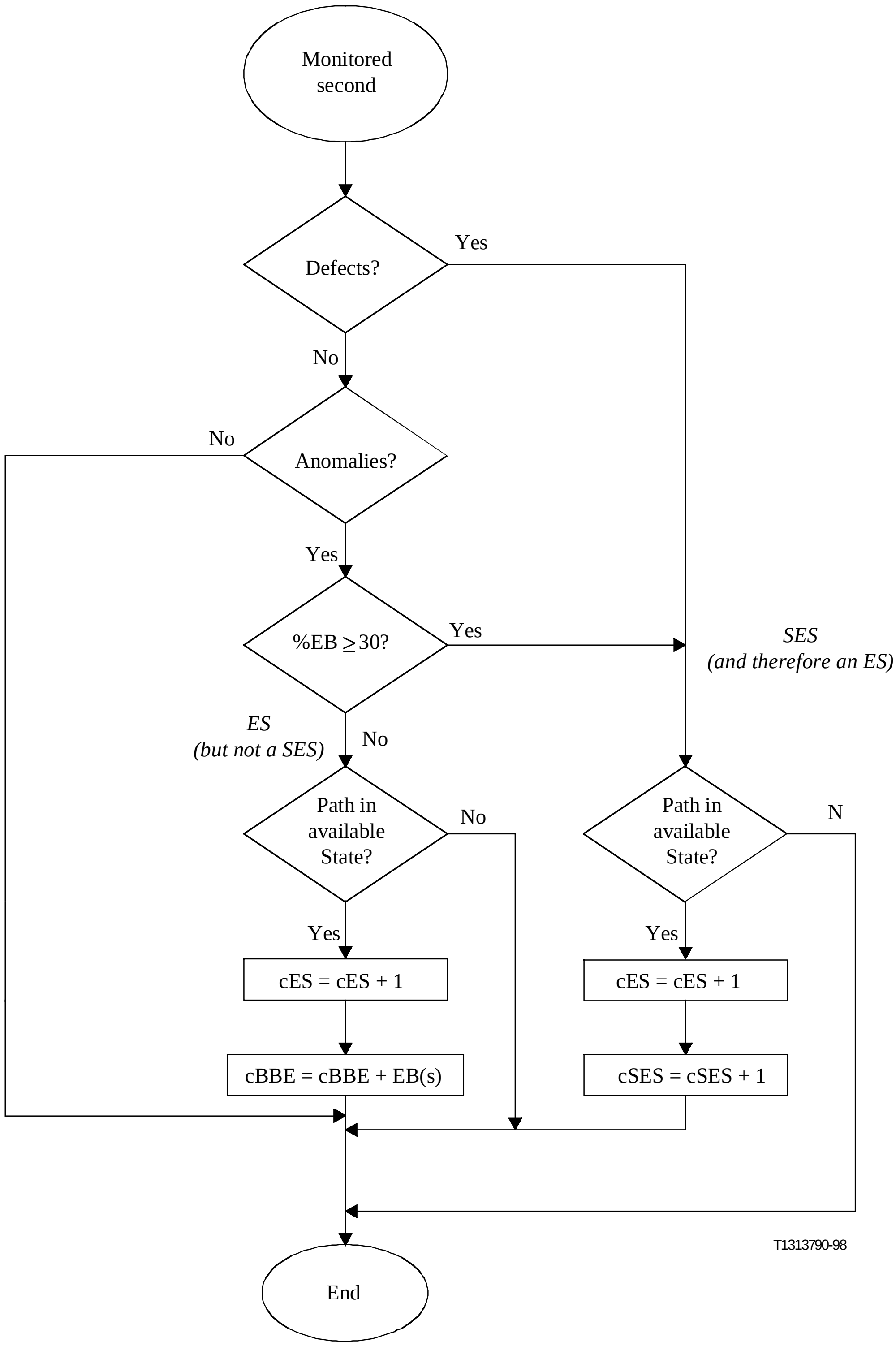


Figure I.1/G.826 – Flow chart illustrating the recognition of anomalies, defects, errored blocks, ES, SES and BBE

Notes to Figure I.1

NOTE 1 – The determination of unavailability time introduces a delay of ten seconds. This delay should be considered when counting BBE, ES and SES.

NOTE 2 – cES, cSES and cBBE represent counts of ES, SES, BBE respectively. These counts are reset at the start of a measurement period.

NOTE 3 – EB is the count of errored blocks within an ES whilst %EB represents the proportion of errored blocks within an ES compared to the number of blocks per second.

NOTE 4 – G.826 parameters can be evaluated during, or at the end of, a measurement period P as follows, taking into account Unavailable Seconds (UAS):

$BBER = cBBE/[(P - UAS - cSES) \times \text{blocks per second}]$

$ESR = cES/(P - UAS)$

$SESR = cSES/(P - UAS)$

NOTE 5 – In the simplified diagram, no action is taken if the path is in the unavailable state. This is because the diagram does not consider the transition between availability states when, in fact, event counters must be modified retrospectively. In practice, the status of a second (i.e. error-free, ES or SES) must always be determined before a test is made on the status of path availability. In other words, error events are always detected regardless of whether the path is available or not – only the *counting* of events is inhibited during unavailability periods for the purposes of long-term performance monitoring. This process is reflected in the flow chart although consequent actions on changes of availability state are not.

APPENDIX II

Bit errors and block errors, merits and limitations

In digital transmission technology, any bit received in error – a Bit Error – may deteriorate transmission quality. It is obvious that quality will decrease with an increasing number of erroneous bits. Therefore, the ratio of the number of errored bits referred to the total number of bits transmitted in a given time interval is a quantity which can be used to describe digital transmission performance.

The quantity is called Bit Error Ratio (BER) and is a well-known error performance parameter (see definition in Fascicle I.3 of the CCITT *Blue Book*).

Bit Error Ratio can only be measured if the bit structure of the evaluated sequence is known. For this reason, bit error ratio measurements are mostly carried out using well-defined Pseudo-Random Bit Sequences (PRBSs). In practice, the PRBS replaces the information sent in-service. This means that BER can only be measured correctly out-of-service because the bit structure of an arbitrary message is normally unknown.

It was one of the prime objectives of this Recommendation to define all performance parameters in such a way that in-service estimation is possible. Thus, parameter definitions based upon Bit Error Ratios were not chosen in spite of their merits.

In-service detection of errors in digital transmission is possible, however, using special error detection mechanisms (Error Detection Code, EDC) which are inherent to certain transmission systems.

Examples of those inherent EDCs are Cyclic Redundancy Check (CRC), Parity Check and observation of Bit Interleaved Parity (BIP). EDCs are capable to detect whether one or more errors have occurred in a given sequence of bits – the block. It is normally not possible to determine the exact number of errored bits within the block.

Block Errors are processed in a similar way as Bit Errors, i.e. the term "Block Error Ratio" is defined as the ratio of the number of errored blocks referred to the total number of blocks transmitted in a given time interval.

The basic philosophy of this Recommendation is based upon the measurement of errored blocks, thus making in-service error estimation possible.

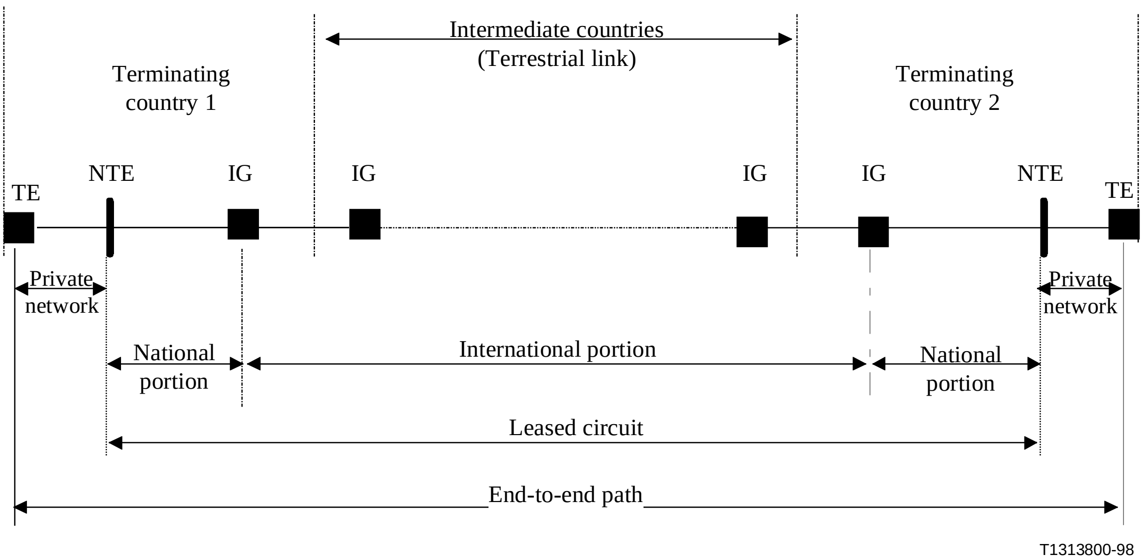
It should be noted that the measurement of Bit Error Ratio and Block Error Ratio yields comparable results for small Bit Error Ratios.

It should also be noted that for some specific error models it is possible to calculate Bit Error Ratio from a Block Error Ratio. It is the drawback of this procedure that error models describe the situation found in practice only imperfectly and may be strongly media-dependent. Therefore, the result of such a calculation is not very reliable

APPENDIX III

Applicability of Recommendation G.826 to non-public networks

Figure III.1 depicts a typical leased circuit situation where a path is composed of three independent networks: two private networks at both path ends and a public network connecting them.



IG International Gateway
NTE Network Terminal Equipment
TE Terminal Equipment

Figure III.1/G.826 – Digital path composed of two private networks and a leased circuit provided by a public network operator

The public network provides a leased circuit to connect the two private networks. However, the problem is not restricted to the case shown in Figure III.1 but is of more general nature. For instance, similar considerations are applicable if only one side of the path ends in a private network.

Taking into account that a public operator can only control the public network from NTE to NTE (Network Terminal Equipment), no performance objectives can be given for the portion between NTE and TE.

It may also be that the public network operator provides the connection by other means than a leased circuit.

ITU-T RECOMMENDATIONS SERIES

Series A	Organization of the work of the ITU-T
Series B	Means of expression: definitions, symbols, classification
Series C	General telecommunication statistics
Series D	General tariff principles
Series E	Overall network operation, telephone service, service operation and human factors
Series F	Non-telephone telecommunication services
Series G	**Transmission systems and media, digital systems and networks**
Series H	Audiovisual and multimedia systems
Series I	Integrated services digital network
Series J	Transmission of television, sound programme and other multimedia signals
Series K	Protection against interference
Series L	Construction, installation and protection of cables and other elements of outside plant
Series M	TMN and network maintenance: international transmission systems, telephone circuits, telegraphy, facsimile and leased circuits
Series N	Maintenance: international sound programme and television transmission circuits
Series O	Specifications of measuring equipment
Series P	Telephone transmission quality, telephone installations, local line networks
Series Q	Switching and signalling
Series R	Telegraph transmission
Series S	Telegraph services terminal equipment
Series T	Terminals for telematic services
Series U	Telegraph switching
Series V	Data communication over the telephone network
Series X	Data networks and open system communications
Series Y	Global information infrastructure
Series Z	Languages and general software aspects for telecommunication systems