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DIGITAL NETWORKS

THE CONTROL OF JITTER AND WANDER WITHIN DIGITAL NETWORKS WHICH ARE BASED ON THE 2048 kbit/s HIERARCHY

ITU-T Recommendation G.823

(Previously "CCITT Recommendation")

FOREWORD

The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the International Telecommunication Union. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, established the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

ITU-T Recommendation G.823 was revised by the ITU-T Study Group XVIII (1988-1993) and was approved by the WTSC (Helsinki, March 1-12, 1993).

NOTES

1 As a consequence of a reform process within the International Telecommunication Union (ITU), the CCITT ceased to exist as of 28 February 1993. In its place, the ITU Telecommunication Standardization Sector (ITU-T) was created as of 1 March 1993. Similarly, in this reform process, the CCIR and the IFRB have been replaced by the Radiocommunication Sector.

In order not to delay publication of this Recommendation, no change has been made in the text to references containing the acronyms “CCITT, CCIR or IFRB” or their associated entities such as Plenary Assembly, Secretariat, etc. Future editions of this Recommendation will contain the proper terminology related to the new ITU structure.

2 In this Recommendation, the expression “Administration” is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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THE CONTROL OF JITTER AND WANDER WITHIN DIGITAL NETWORKS WHICH ARE BASED ON THE 2048 kbit/s HIERARCHY

(Melbourne, 1988; revised at Helsinki, 1993)

1 Scope of the Recommendation

In a transmission network jitter and wander accumulate according to the jitter and wander generation and transfer characteristics of each equipment interconnected. These equipments may be different types of multiplexers/demultiplexers and line systems.

An excessive amount of jitter and wander can adversely affects both digital (generation of bit errors, uncontrolled slips) and analogue signals (unwanted phase modulation of the transmitted signal). It Is therefore necessary to set limits to the presence of jitter and wander at the network interfaces, in order to guarantee a proper quality of the transmitted signals.

The scope of this Recommendation is to define the parameters and the relevant values that are able to control satisfactorily the amount of jitter and wander present at plesiochronous digital hierarchies (PDH) network interfaces.

The Recommendation is applicable to networks adopting the digital hierarchy based on the first level bit rate of 2048 kbit/s. The electrical characteristics of the relevant network interfaces are described in Recommendation G.703

The jitter control philosophy is based on the need:

– to recommend a maximum network limit that should not be exceeded at any hierarchical interface;

– to recommend a consistent framework for the specification of individual digital equipments;

– to provide sufficient information and guidelines for organizations to measure and study jitter accumulation in any network configuration.

2 Network limits for the maximum output jitter and wander at any hierarchical interface

2.1 Network limit for jitter

The limits given in Table 1 represent the maximum permissible levels of jitter at hierarchical interfaces within a digital network. The limits should be met for all operating conditions and regardless of the amount of equipment preceding the interface. These network limits are compatible with the minimum tolerance to jitter that all equipment input ports are required to provide.

In operational networks, to compensate for the progressive accumulation and onward transfer of jitter in and through cascaded network elements (such as regenerators, etc.), it will generally be necessary to control the jitter at a suitably *lower* level than the maximum permissible limit. Furthermore, on long transmission routes incorporating a large number of cascaded sections, equipment providing jitter reduction may be necessary to avoid exceeding the network limit and the jitter tolerance of individual equipments. In circumstances where the maximum permissible jitter amplitude occurs at an interface between two countries, it is left to the discretion of national Administrations to take the appropriate remedial action. This situation is unlikely to occur very often.

The arrangements for measuring output jitter at a digital interface are illustrated in Figure 1. The specific jitter limits and values of filter cut-off frequencies for the different hierarchical levels are given in Table 1. The frequency response of the filters associated with the measurement apparatus should have a roll-off of 20 dB/decade. Suitable test apparatus is described in Recommendation O.171.

TABLE 1/G.823

Maximum permissible jitter at a hierarchical interface

Parameter value → / Digit rate (kbit/s) ↓	Network limit		Measurement filter bandwidth		
	B_1 unit interval peak-to-peak	B_2 unit interval peak-to-peak	Band-pass filter having a lower cut-off frequency f_1 or f_3 and an upper cut-off frequency f_4		
			f_1	f_3	f_4
64 (Note 1)	0.25	0.05	20 Hz	3 kHz	20 kHz
2 048	1.5	0.2	20 Hz	18 kHz (700 Hz)	100 kHz
8 448	1.5	0.2	20 Hz	3 kHz (80 kHz)	400 kHz
34 368	1.5	0.15	100 Hz	10 kHz	800 kHz
139 264	1.5	0.075	200 Hz	10 kHz	3500 kHz

NOTES

1 For the codirectional interface only.

2 The frequency values shown in parenthesis only apply to certain national interfaces.

3 UI Unit Interval:

for 64 kbit/s 1 UI = 15.6 µs

for 2048 kbit/s 1 UI = 488 ns

for 8448 kbit/s 1 UI = 118 ns

for 34 368 kbit/s 1 UI = 29.1 ns

for 139 264 kbit/s 1 UI = 7.18 ns

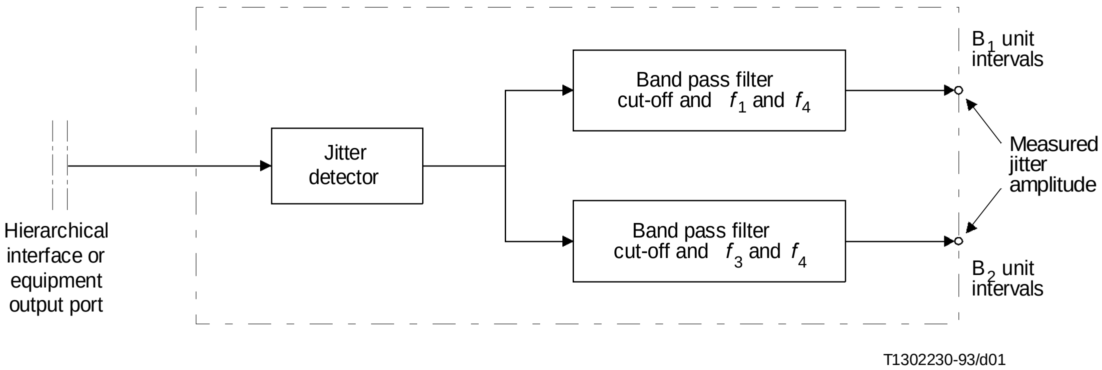


FIGURE 1/G.823

Measurement arrangements for output jitter from a hierarchical interface or an equipment output port

It is assumed that, within a synchronized network, digital equipment provided at nodes win accomodate permitted phase deviations on the incoming signal, together with jitter and wander from the transmission plant, i.e., under normal synchronized conditions, slips will not occur. However, it should be recognized that, as a result of some performance degradations, failure conditions, maintenance actions and other events, the relative time interval error (TIE) between the incoming signal and the internal timing signal of the terminating equipment may exceed the wander and jitter tolerance of the equipment which will result in a controlled slip.

At nodes terminating links interconnecting independently synchronized networks (or where plesiochronous operation is used in national networks), the relative TIE between the incoming signal and the internal timing signal of the terminating equipment may eventually exceed the wander and jitter tolerance of the equipment in which case slip will occur. The maximum permissible long-term mean controlled slip rate resulting from this mechanism is given by Recommendation G.811, i.e. one slip in 70 days.

For equipments which are not controlled by a network synchronizing system, but by an autonomous clock (e.g. quartz oscillator) more stringent output jitter values may be defined in the relevant equipment specifications. Examples are the muldex in Recommendation G.735, and concerning the primary rate access in Recommendation I.431

2.2 Network limits for wander

A maximum network limit for wander at all hierarchical interfaces has not been defined. Actual magnitudes of wander, being largely dependent on the fundamental propagation characteristics of transmission media and the ageing of clock circuitry (see 3/G.811), can be predicted. Studies have shown that, provided input ports can tolerate wander in accordance with the input tolerance requirements of 3.1.1, then slips introduced as a result of exceeding the input tolerance, will be rare. For interfaces to network nodes the following limits apply.

The MTIE (see Recommendation G.811) over a period of *S* seconds shall not exceed the following:

1) $S < 10^4$, this region requires further study;

2) $(10^{-2} S + 10\,000)$ ns, Applicable to values of *S* greater than 10^4.

NOTES

1 The resultant overall specification is illustrated in Figure 2.

2 The full MTIE of 10 μs, superimposed on the average timing, as specified above, may only occur ay the output of the last node in a chain of nodes. This must be ensured by applying appropriate planning rules.

3 Jitter limits appropriate to digital equipments

3.1 Basic specification philosophy

For individual digital equipments it is necessary to specify their jitter performance in three ways.

3.1.1 jitter and wander tolerance of digital input ports

ln order to ensure that any equipment can be connected to any recommended hierarchical interface within a network, it is necessary to arrange that the input ports of all equipments are capable of accomodating levels of jitter up to the maximum network limit defined in Table 1.

For convenience of testing, the required tolerance is defined in terms of the amplitude and frequency of sinusoidal jitter which, when modulating a test pattern, should not cause any significant degradation in the operation of the equipment. It is important to recognize that the test condition is not, in itself, intended to be representative of the type of jitter to be found in practice in a network. However, the test does ensure that the “Q” factor associated with the timing signal recovery of the equipments input circuitry is not excessive and, where necessary, that an adequate amount of buffer storage has been provided.

Thus, all digital input ports of equipment should be able to tolerate a digital signal having electrical characteristics in accordance with the requirements of Recommendation G.703 but modulated by sinusoidal wander and jitter having an amplitude-frequency relationship defined in Figure 3. Table 2 indicates the appropriate limits for the different hierarchical levels.

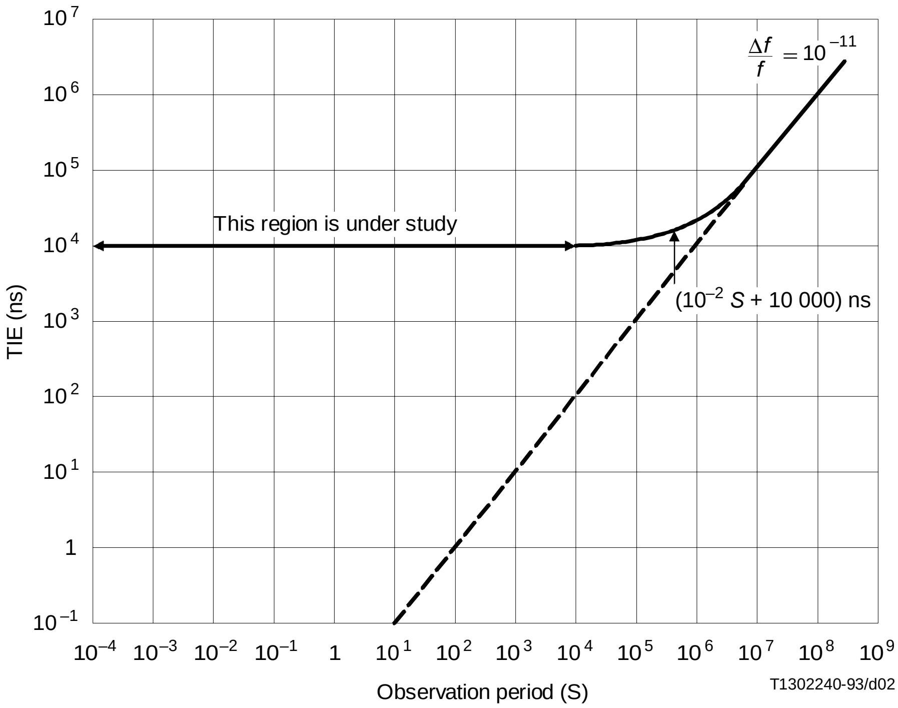


FIGURE 2/G.823

Permissible maximum time interval error (MTIE)
versus observation period *S* for the output of a network node

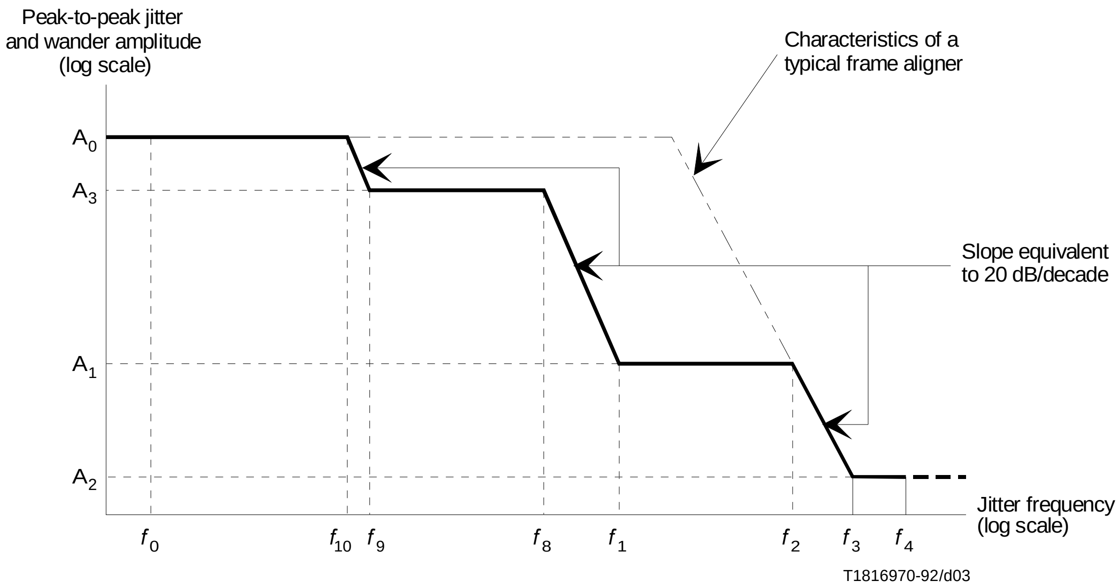


FIGURE 3/G.823

Lower limit of maximum tolerable input jitter and wander

The wander/jitter is superimposed upon a timing signal which is ideally synchronous with a reference clock, and in practice reasonably stable. Instrumentation in accordance with Recommendation O.171 is appropriate for measurement at wander/jitter frequencies above 2 Hz.

In principle, these requirements should be met regardless of the information content of the digital signal. For test purposes, the equivalent binary content o f the signal with jitter modulation should be a pseudo-random bit sequence as defined in Table 2.

In deriving these limits, the wander effects are considered to be predominant at frequencies below f_l, and many transmission equipments, such as digital line systems and asynchronous muldexes using justification techniques, are effectively transparent to these very low frequency changes in phase. Notwithstanding this, it does not need to be accomodated at the input of certain equipment (e.g. digital switches and synchronous muldexes). The requirement below f_l is not amenable to simple practical evaluation but account should be taken of the requirement at the design stage of the equipment.

Unlike that part of the mask between frequencies f_l and f_4, which reflect the maximum permissible jitter magnitude in a digital network, that part of the mask below the frequency f_l does not aim to represent the maximum permissible wander that might occur in practice. Below the frequency f_l, the mask is derived such that where necessary, the provision of this level of buffer storage at the input of an equipment facilitates the accomodation of wander generated in a large proportion of real connections.

An input synchronizing a node and another not synchronizing the node may derive their respective timing from the same reference clock, but over different paths, and may therefore, in an extreme case, have opposite phase deviation. The expected maximum relative phase deviation is 18 μs which must be accomodated by the equipment.

A short-term reversal of the relative TIE between the incoming signal, and the internal timing signal of the terminating equipment shortly after the occurrence of a controlled slip should not cause another slip. In order to prevent such a slip, the equipment should be designed with a suitable hysteresis for this phenomenon. This hysteresis should be at least 18 μs.

3.1.2 Maximum output jitter in the absence of input jitter

It is necessary to restrict the amount of jitter generated within individual equipments. Recommendation dealing with specific systems define the maximum levels of jitter that may be generated in the absence of input jitter. The actual limits applied depend upon the type of equipment. They should be met regardless of the information content of the digital signal. In all cases the limits never exceed the maximum permitted network limit. The arrangement for measuring output jitter is illustrated in Figure 1.

3.1.3 Jitter and wander transfer characteristics

Jitter transfer characteristics define the ratio of output jitter to input Jitter amplitude versus jitter frequency for a given bit rate. When jitter is present at the digital input port of digital equipment, in many cases some portion of the jitter is transmitted to the corresponding digital output port. Many tvpes of digital equipment inherent attenuate the higher frequency jitter components present at the input. To control jitter in cascaded homogeneous digital equipment, it is important to restrict the value of jitter gain. The jitter transfer for a particular digital equipment can be measured using a digital signal modulated by sinusoidal jitter.

Figure 4 indicates the general shape of a typical jitter transfer characteristics. The appropriate values for the levels x and $-y$ dB and the frequencies f, f_5, f_6 and f_7 can be obtained from the relevant Recommendation.

Because the bandwidth of phase smoothing circuits in asynchronous digital equipment is generally above 10 Hz, wander on the input signal may appear virtually unattenuated on the output. However, in certain particular digital equipments (e.g. nodal clocks) it is necessary that wander be sufficiently attenuated from output to output. Recommendations dealing with synchronous equipment will ultimately define limiting values for particular wander transfer characteristics.

3.2 Digital sections

To ensure that the maximum network limit (clause 2) is not exceeded within a digital network, it is necessary to control the jitter contributed by transmission systems.

The jitter limits for digital sections are found in Recommendation G.921.

TABLE 2/G.823

Parameter values for input jitter and wander tolerance

Digit rate (kbit/s)	Peak-to-peak amplitude unit interval				Frequency								Pseudo-random test-signal
	A_0	A_1	A_2	A_3	f_0	f_{10}	f_9	f_8	f_1	f_2	f_3	f_4	
64 (Note 1)	1.15 (18 µs)	[a]	0.25	0.05	1.2×10^{-5} Hz	[a]	[a]	[a]	20 Hz	600 Hz	3 kHz	20 kHz	$2^{11} - 1$
2 048	36.9 (18 µs)	18 (Note 7)	1.5	0.2	1.2×10^{-5} Hz	4.88×10^{-3} Hz (Note 7)	0.01 Hz (Note 7)	1.667 Hz (Note 7)	20 Hz	2.4 kHz (93 Hz)	18 kHz (700 Hz)	100 kHz	$2^{15} - 1$ (Rec. O.151)
8 448	152 (18 µs)	[a]	1.5	0.2	1.2×10^{-5} Hz	[a]	[a]	[a]	20 Hz	400 Hz (10.7 kHz)	3 kHz (80 kHz)	400 kHz	$2^{15} - 1$ (Rec. O.151)
34 368	618.6 (18 µs)	[a]	1.5	0.15	[a]	[a]	[a]	[a]	100 Hz	1 kHz	10 kHz	800 kHz	$2^{23} - 1$ (Rec. O.151)
139 264	2506.6 (18 µs)	[a]	1.5	0.075	[a]	[a]	[a]	[a]	200 Hz	500 Hz	10 kHz	3500 kHz	$2^{23} - 1$ (Rec. O.151)

[a] Values under study.

NOTES

1 For the codirectional interface only.

2 For interfaces within national networks the frequency values (f_2 and f_3) shown in parenthesis may be used.

3 UI Unit Interval:

for 64 kbit/s 1 UI = 15.6 µs

for 2048 kbit/s 1 UI = 488 ns

for 8448 kbit/s 1 UI = 118 ns

for 34 368 kbit/s 1 UI = 29.1 ns

for 139 264 kbit/s 1 UI = 7.18 ns

4 The value for A_0 (18 µs) represents a relative phase deviation between the incoming signal and the internal timing local signal derived from the reference clock.

5 The absolute phase deviation requires further study.

6 An example of reference configuration explaining the A_0 values is given in Annex C.

7 These values refer to 2048 kbit/s interfaces which are not used for carrying synchronization signals. Specifications for synchronization signals are under study.

3.3 Digital muldexes

The jitter limits for digital multiplexers and demultiplexers are found in the appropriate equipment Recommendations.

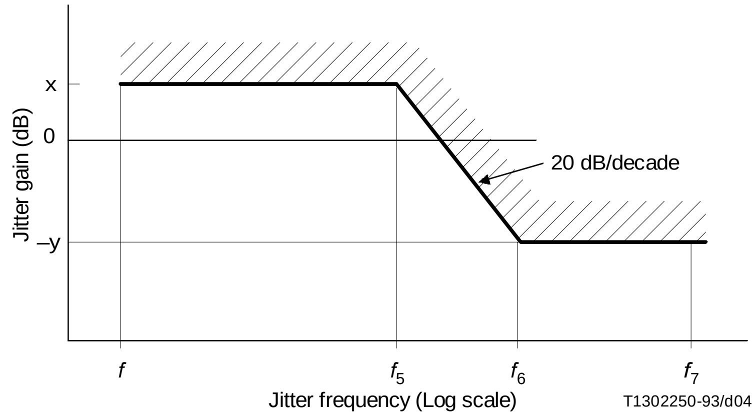


FIGURE 4/G.823

Typical jitter transfer characteristics

4 Guidelines concerning the measurement of jitter

There are two clearly identifiable categories under which jitter measurement may be classified:

- measurements using an undefined traffic signal which may generally be considered as quasi-random (generally applicable under operational circumstances);
- measurements using specific test sequencies (generally applicable during laboratory, factory and commissioning circumstances).

4.1 Measurements using an undefined traffic signal

Because of the quasi-random nature of jitter and its possible dependency on traffic loading, accurate peak-to-peak measurements in operational networks need to be made over long periods of time. In practice it is expected that, with experience of particular systems, it will be possible to identify abnormalities measured over a shorter measurement period which would indicate that the maximum permissible limit might be exceeded over a longer measurement interval.

The network limits recommended in 2 are so derived that the probability of exceeding such levels is very small. The practical observation of such a magnitude with a high degree of confidence requires an unacceptable measurement interval. To take account of such an effect it may be necessary to introduce a smaller, but related, limit which has a greater probability of occurrence, facilitating its measurement over a reasonably short measurement interval. These aspects are the subject of further study.

4.2 Measurements using a specific test sequence

Given that it is advantageous to assess the jitter performance of digital line equipment using a specific pseudo-random binary sequence (PRBS), it is necessary to derive limits appropriate to this unique test condition. Although the use of such deterministic test signals is extremely useful for factory acceptance tests and commissioning tests, the results need to relate to an operational situation in which the information content of the signal is likely to be more random (e.g. a telephony type signal). Based on practical experience, it is usually possible to relate a traffic-based measurement to a PRBS-based measurement by the application of an appropriate correction factor (Annex A).

The use of a PRBS in the measurement of jitter may have shortcomings in that for the measurement to be valid the PRBS must have adequate spectral content within the jitter bandwidth of the system being measured. In circumstances where the spectral content is insufficient, a suitable correction must be applied if a measured value is to be meaningfully compared with specified limits. This aspect is the subject of further study (Annex A).

4.3 Test signal interaction with signal processing devices integral to transmission systems

The inclusion of additional signal processing devices integral to a transmission system often influences the observed jitter performance. Studies have shown that the transmitted signal, particularly if it is pseudo-random or highly structured, interacts with digital scramblers and line code converters to produce interesting effects which are observed as changes in the performance of such equipments. All interaction effects result in a modification to the statistics of the transmitted signal causing a consequential change in the pattern-sensitive jitter generated within each repeater. A typical manifestation is that successive measurements on a transmission system incorporating these devices, using an identical test signal on each occasion, yield a widely varying range of peak-to-peak and r.m.s. jitter amplitudes.

Studies have shown that the following factors influence the observed jitter performance:

- the feedback connections on both the PRBS test signal generator and the transmission system's scrambler;
- the number of stages on the PRBS test signal generator and the transmission system's scrambler;
- the presence of a code converter in the transmission system.

Consequently, considerations concerning the choice of test signal for equipment validation purposes should take account of the following points:

a) It is inadvisable to use a PRBS test signal generator with a cycle length that has common factors with the scrambler incorporated in the transmission system;

b) The equal configuration of the PRBS test signal generator and the transmission system's scrambler should be avoided if a random signal is required.

5 Jitter accumulation in digital networks

The variability of network configurations prevents the consideration of every possible case. To analyse a particular network configuration, it is necessary to use the information about the jitter characteristics of individual equipments in conjunction with appropriate jitter accumulation models. Annex B aims to provide sufficient information to enable organizations to carry out such evaluations.

Annex A

The use of a pseudo-random binary sequence (PRBS) for jitter measurements on digital line, radio and optical fibre systems

(This annex forms an integral part of this Recommendation)

A.1 The relationship between a random traffic-based measurement and a PRBS-based measurement

It is often convenient to emulate a random type traffic signal using a pseudo-random binary sequence (PRBS). However, jitter measurements using such a test signal tend to give optimistic values when compared with an identical measurement using a traffic signal in which the information content is more random. This disparity arises because the traffic signal, which is generally non-deterministic in nature, is able to cause the generation of an almost unrestricted range of jitter amplitudes, whereas the quasi-random nature of a PRBS means that it is only able to cause the generation of a finite range of jitter amplitudes. Based on operational experience to date, a correction factor relating the two types of measurement has been determined, but it is extremely difficult to establish an accurate value for every conceivable practical situation. Its actual value is dependent on many interrelated aspects such as the measurement period, system length, the value of the timing recovery circuit *Q*, the sequence length, and the presence of scramblers. To relate a random traffic-based measurement (made over a relatively short interval) to a specific PRBS, it is necessary to use the following correction factors which are believed to represent a good practical choice for most circumstances:

– 1.5 at 2048 kbit/s and 8448 kbit/s (based on the use of a $2^{15} – 1$ PRBS generated in accordance with Recommendation O.151);

– 1.3 at 34 368 kbit/s and 139 264 kbit/s (based on the use of a $2^{23} – 1$ PRBS generated in accordance with Recommendation O.151).

Therefore:

$$\begin{bmatrix}\text{Estimated jitter amplitude}\\ \text{when transmitting random}\\ \text{signal (traffic)}\end{bmatrix} = \text{Correction factor} \times \begin{bmatrix}\text{Measured jitter}\\ \text{amplitude using}\\ \text{a specific PRBS}\end{bmatrix}$$

A.2 Spectral content of the PRBS

By its very nature, the PRBS is cyclical and is therefore characterized by a power spectrum with spectral lines occurring at regularly spaced intervals. For the achievement of a meaningful result, in which the measurement error is acceptable, it is necessary to ensure that the PRBS used when measuring output jitter, has adequate spectral content within the jitter bandwidth of the system being measured. The bandwidth of the jitter spectrum at the output of a chain of digital regenerators is shown to be a function of the *Q* factor of the timing recovery circuit and the number of generators in tandem [1].

Now:

$$\text{Jitter bandwidth} = \frac{f_1}{Q \times n} \text{ [Hz] for large } n$$

where

f_1 is the frequency of the timing signal that is extracted from the incoming signal by the timing recovery circuit;

Q is the Q factor of one repeater;

n is the number of cascaded repeaters;

and

$$\text{PRBS repetition rate} = \frac{f}{L} \text{ [Hz]}$$

where

f is the bit rate; and

L is the sequence length.

For adequate spectral content, the pattern repetition frequency should be less than $\frac{1}{y}$ of the jitter bandwidth of the system under test. (The value for *y* requires further study).

Thus

$$\frac{f}{L} \leq \frac{f_1}{y \times Q \times n}$$

and

$$L \geq y \times n \times Q \times \frac{f}{f_1}$$

Examples

For line code B6ZS $f = f_1$ and $L \geq y \times n \times Q$

For a Non-Redundant Quaternary line code $\frac{f}{f_1} = \frac{2}{1}$ and $L \geq y \times n \times Q \times 2$

If the system uses a scrambler or a code translation technique (e.g. 4B3T), this may be taken into account in order to reduce the length of the test sequence.

Annex B

Jitter accumulation in digital networks and related guidelines

(This annex forms an integral part of this Recommendation)

B.1 Jitter accumulation in digital networks

B.1.1 Jitter accumulation relationships for cascaded homogeneous digital equipments

B.1.1.1 Digital line, radio and optical fibre systems

With this type of equipment, the relationship applicable is critically dependent on the content of the transmitted signal, the physical implementation of timing recovery, the inclusion of a scrambler/descrambler combination, etc. A number of relationships are identified.

B.1.1.1.1 Cascaded homogeneous regenerators

Most digital repeaters currently in use are fully regenerative and self-timed; that is, the output signal is retimed under the control of a timing signal derived from the incoming signal. The most significant form of jitter arises from imperfections in the circuitry, which cause jitter that is dependent on the sequence of pulses in the digital signal being transmitted, termed pattern-dependent jitter. The mechanisms that generate jitter within a regenerator, that have been extensively studied, are principally related to imperfections in the timing-recovery circuit [2], [3] and [4].

Since pattern-dependent jitter from regenerated sections is the dominant type of jitter in a network, the manner in which it accumulates must be considered. For jitter purposes, a regenerative repeater acts as a low-pass filter to the jitter present on the input signal, but it also generates jitter, which can be represented by an additional jitter source at the input. If this added jitter were truly random, as distinct from pattern dependent, then the total r.m.s. jitter, J_N, present on the digital signal after N regenerators would be given by the approximate relationship:

$$J_N \approx J \times \sqrt[4]{N} \qquad \text{(B-1)}$$

where J is the r.m.s. jitter from a single regenerator due to uncorrelated jitter sources. This equation assumes that the jitter added at each regenerator is uncorrelated.

However, most of the jitter added is pattern dependent and, since the pattern is the same at each regenerator, it can be assumed that the same jitter is added at each regenerator in a chain of similar regenerators. In this case, it can be shown that the low-frequency components of the jitter add linearly, whereas the higher-frequency components are increasingly attenuated by the low-pass filtering effect of successive regenerators. If a random signal is being transmitted, the r.m.s. jitter J_N, present on the signal after N regenerators would be given by the approximate relationship.

$$J_N \approx J_1 \times \sqrt{2N} \text{ for large values of } N \qquad \text{(B-2)}$$

where J_1 is the r.m.s. jitter from a single regenerator due to pattern-dependent mechanisms [1].

NOTES

1 Based on operational experience to date, values for J_1 in the range 0.4 to 1.5% of a unit interval are achievable using cost-effective designs.

2 The implementation of timing recovery using a phase-locked loop causes the rate of accumulation to be marginally greater, as given by the approximate relationship:

$$J_N = J_1 \times \sqrt{2NA} \qquad \text{(B-3)}$$

where A is a factor dependent upon both the number of regenerators and the phase-locked loops damping factor. The latter parameter is generally chosen, in this application, such that A has an amplitude marginally greater than unity.

3 The implementation of timing recovery using a transversal surface acoustic filter produces a rate of accumulation approaching that obtained for uncorrelated jitter sources. This favourable jitter accumulation arises because of the large inherent delay which reduces the correlation between the recovered timing signal and the data stream. Systematic pattern-dependent jitter is therefore effectively randomized and tends to accumulate in a manner similar to that obtained from uncorrelated jitter sources. The only noticeable side-effect is a marginal degradation in the alignment jitter. This favourable jitter accumulation is not exhibited by surface acoustic wave resonators due to their different mode of operation [9].

4 Repeaters incorporating circuitry involving pattern transformations effectively represent uncorrelated jitter sources causing a non-systematic jitter accumulation. For example, a pattern transformation based on the modulo 2 addition of a signal and its delayed version (Huffman sequence) causes the r.m.s. jitter to accumulate approximately with the fourth root of the number of repeaters [8].

Equations (B-1) and (B-2) demonstrate two important results:

a) pattern-dependent jitter accumulates more rapidly than non-pattern-dependent jitter, as the number of regenerators is increased; and

b) the amplitude of jitter produced by a chain of regenerators increases without limit, as the number of regenerators is increased.

The jitter produced by a random pattern is itself random in nature, the amplitude probability distribution function of which is considered to be close to gaussian. Hence, for a given r.m.s. amplitude (standard deviation), the probability of exceeding any chosen peak-to-peak amplitude can be calculated. A peak-to-peak to r.m.s. ratio of between 12 and 15 is often assumed for specification purposes, which has a very low probability of being exceeded.

In contrast, when the signal being transmitted is composed of two repetitive patterns, alternating at low frequency, the jitter appears as a low-frequency repetitive wave, having an amplitude proportional to the number of regenerators. This could lead to very large amplitudes of jitter. In such instances, the maximum peak-to-peak jitter amplitude (J_{NP}) is described by the following relationship:

$$J_{NP} = d \times N \qquad \text{(B-4)}$$

where d is the pattern sensitive jitter (PSJ) produced by a single regenerator when subjected to alternating repetitive patterns. This relationship assumes that the repetition rate is sufficiently low so that steady states are attained. The actual value is dependent on the pattern used.

This situation is very unlikely in normal operation because the signal transmitted is generally made up of traffic from a number of different sources, although not necessarily so at the primary line rate, together with a frame alignment signal and justification control digits, etc. Furthermore, the probability of fixed patterns occurring can be reduced still further by the use of digital scramblers, which tend to randomize the signal.

B.1.1.1.2 Cascaded homogeneous digital line, radio and optical fibre systems incorporating scramblers and jitter reducers

The inclusion of a scrambler/descrambler combination in a digital line, radio or optical fibre system needs to be considered when such homogeneous systems are connected in cascade. In such situations, the jitter contributed to each system is uncorrelated and is therefore found to accumulate in accordance with the fourth root of the number of cascaded systems. Therefore, the r.m.s. jitter, J_M, present on the digital signal after M digital line, radio or optical fibres systems is given by the approximate relationship:

$$J_M \approx J_S \times \sqrt[4]{KM} \qquad \text{(B-5)}$$

where J_S is the r.m.s. jitter from a single system and K is a constant with a value between 1 and 2. For large values of M, $K = 2$.

Where jitter reducers are provided in addition to scramblers, the same accumulation relationship may apply, except that the value for J_S is then significantly reduced. In such circumstances, the r.m.s. jitter, J_S, is given by the following approximate relationship:

$$J_S \approx 2N\ J \sqrt{\frac{f_c}{B}} \ \text{for large}\ \ N \qquad \text{(B-6)}$$

where J is the r.m.s. jitter from a single repeater, N is the number of cascaded repeaters, f_c is the cut-off frequency of the jitter reducer and B is the half bandwidth of a single repeater:

$$\left(B = \frac{W_0}{2Q} \right)$$

NOTE – The validity of the relationships given in this subclause requires further study. Particularly in the case where jitter reducers are incorporated, as the degree of randomization, produced by the length of scrambler commonly considered acceptable, may not be sufficient to ensure that the jitter contributions, within the bandwidth of the jitter transfer functions expected, are uncorrelated to the extent that fourth root accumulation is dominant.

B.1.1.2 Muldex equipments

With this type of equipment, the only type of jitter that is likely to accumulate to any significant extent is the variable low frequency waiting time jitter which may have components at frequencies within the passband of the demultiplexers phase-locked loop. The expectations are that the accumulation of waiting time jitter will be at a rate between:

$$\sqrt[4]{N} \text{ and } \sqrt[2]{N},$$

where N is the number of cascaded multiplexer/demultiplexer pairs [5], [6] and [7].

Further study is required to determine a more exact relationship.

B.2 Guidelines concerning the practical application of jitter accumulation relationships in a digital network

These aspects require further study.

Annex C

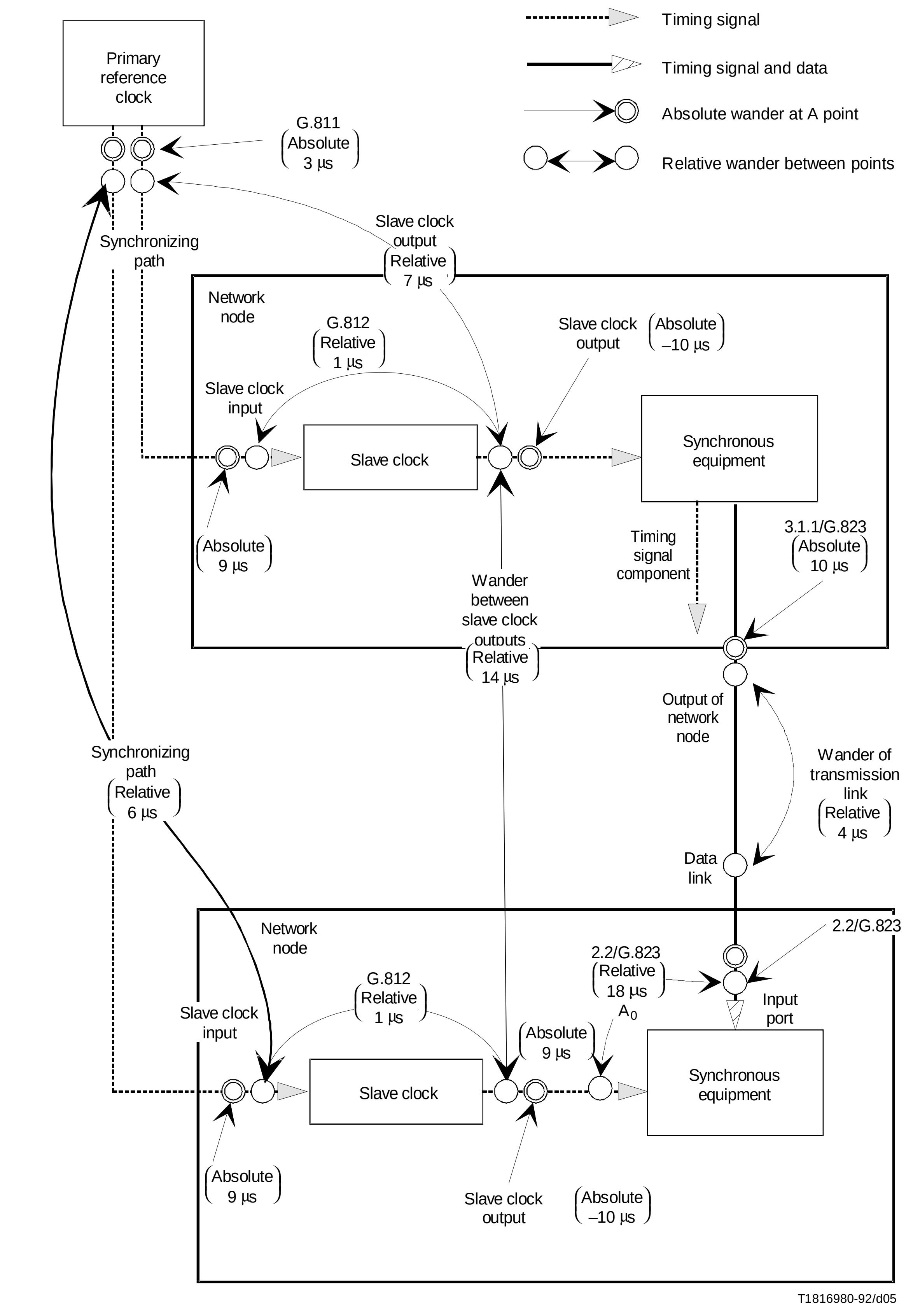
Wander reference model for network nodes

(This annex forms an integral part of this Recommendation)

A Wander reference model for network nodes explaining the A_0 value is given in Figure C.1.

Assumptions made in this model are as follows:

- maximum relative wander at the network nodes 18 µs;
- MTIE of a primary reference clock 3 µs as in Recommendation G.811;
- MTIE at the output of a network node 10 µs as in this Recommendation and Recommendation G.824;
- maximum relative wander in slave clocks 1 µs as in Recommendation G.812.



NOTE – This figure uses the worst case assumption of linear addition of wander. However, more accurate analysis of wander accumulation indicates that this may be pessimistic. This if for further study.

FIGURE C.1/G.823

Wander reference model

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