INTERNATIONAL TELECOMMUNICATION UNION

ITU-T G.192

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

(03/96)

GENERAL CHARACTERISTICS OF INTERNATIONAL TELEPHONE CONNECTIONS AND INTERNATIONAL TELEPHONE CIRCUITS

A COMMON DIGITAL PARALLEL INTERFACE FOR SPEECH STANDARDISATION ACTIVITIES

ITU-T Recommendation G.192

(Previously "CCITT Recommendation")

FOREWORD

The ITU-T (Telecommunication Standardization Sector) is a permanent organ of the International Telecommunication Union (ITU). The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1 (Helsinki, March 1-12, 1993).

ITU-T Recommendation G.192 was prepared by ITU-T Study Group 15 (1993-1996) and was approved under the WTSC Resolution No. 1 procedure on the 19th of March 1996.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

CONTENTS

ABSTRACT

This Recommendation defines the physical, electrical and logical specification of a digital parallel interface which is to be used to interconnect the different devices needed in standardisation activities of speech codecs sponsored by the ITU-T.

Included in this Recommendation are the data formats at the input and output of the encoder, decoder and bit manipulation devices.

Finally, rules for the implementation of codecs to guarantee proper interoperation of devices interconnected using that digital parallel interface are presented.

Recommendation G.192

A COMMON DIGITAL PARALLEL INTERFACE FOR SPEECH STANDARDISATION ACTIVITIES

(Geneva, 1996)

1 Scope

This Recommendation describes a 16-bit parallel input and output interface for the interconnection of test and reference devices in ITU-T standardisation activities.

2 Introduction

The history of the Digital Parallel Interface (DPI) specification goes back to the CCITT wideband speech 64 kbit/s codec tests that led to the present Recommendation G.722, where a similar parallel interface was used. That interface was simplified to fit into a 25-pin connector for the host laboratory sessions of the subjective tests of the GSM full rate codec. This simplified interface has also been used in the standardisation of the second generation GSM system and in the standardisation of the ITU-T 8 kbit/s speech coder. The interface is simple to build and easy to use and, compared to a serial interface, allows for a simpler access to the data flow for monitoring and measuring codec parameters, e.g. delay and timing.

This Recommendation is structured as follows: initially an overview of the principles of the interface is given, with a functional description of the signals and data lines. Then hardware aspects are considered. Specialisations of the interface are given in the annexes. These specialisations involve:

- the DPI implementation using TTL family integrated circuits;
- description of data formats based on the type of device where the DPI is employed;
- device implementation rules when the device is a speech coder; and
- configuration examples for the DPI.

For information, a description of the specialisation used for the host laboratory work of the ITU-T 8 kbit/s coder is given as an appendix.

3 Definitions

For the purposes of this Recommendation, the following definitions and abbreviations apply.

3.1 **codec**: An encoder/decoder pair.

3.2 **coded bitstream signal**: One of the possible signal representations on the DPI, in general representing the signal at the output of an encoder, or the input of a decoder. May also be the representation of a communication channel.

3.3 **CuT**: Codec under Test.

3.4 **DPD**: Digital Processing Device.

3.5 **DPI:** The Digital Parallel Interface defined in this Recommendation.

3.6 **interface timeslot (INTI)**: A rising-edge to rising-edge time interval of the clock signal. A marked INTI refers to a INTI that occurs together with the Mark signal active (high) and an unmarked INTI when Mark is low.

3.7 **LSb**: Least Significant bit.

3.8 **mark signal (mark)**: A one-bit signal that indicates whether the data on the data bus is valid or not.

3.9 **MSb**: Most Significant bit.

3.10 **normal operation**: Mode of operation of the interface used for regular processing by the devices. Alternative to the reset operation.

3.11 **reset operation**: A procedure started when the Reset signal is active for 16 INTIs, and that lasts 1616 INTIs in total. Used to synchronise all the devices in the chain to their initial reset state. After the end of the Reset Operation, the DPI and the interconnected devices resumeNormal Operation.

NOTE – 1616 INTIs represent 1 ms (16 INTIs) plus 100 ms (1600 INTIs) for a 16 kHz clock.

3.12 **reset**: Active-low, one bit signal used to start the Reset Operation.

3.13 **Rx_Clk**: Backwards clock signal. Used to clock devices when the clock master lies in one of the intermediate devices of the chain.

3.14 **softbit**: An element of the coded bitstream signal where logical bits '1' and '0' are represented by 16-bit right adjusted words.

3.15 **synchronisation word**: An element of the coded bitstream signal provided for synchronisation and frame erasure purposes.

3.16 **time signal**: Another of the possible signal representations on the DPI, in general representing time samples. Used necessarily between data source, data sink, and codecs.

3.17 **Tx_Clk**: Forward clock signal. A continuous-time running signal providing the basic rate of the interconnected devices.

4 General Description of the Digital Parallel Interface

Normally, a set of digital test data is processed over different Codecs under Test (CuT) during a standardisation procedure of a speech codec by the ITU-T. Figure 1 shows an example of test configuration where three Digital Processing Devices (DPD) are interconnected by means of the DPI. Each of the DPD have an input and an output DPI.

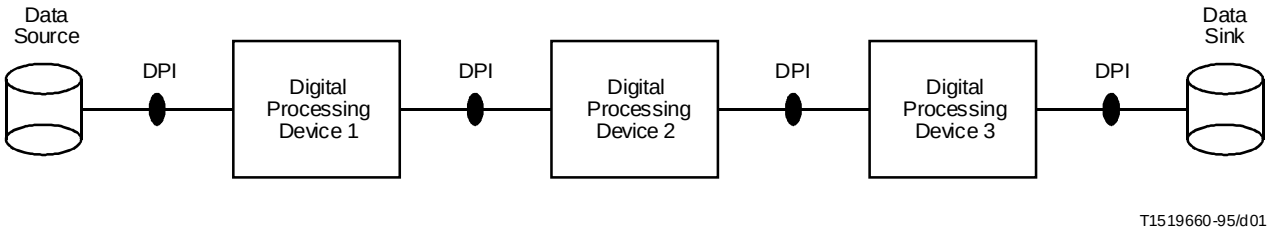


FIGURE 1/G.192

A generic test configuration where the DPI is used

A set of digital test data (usually digitised speech) is sent out synchronously from the data source to the first DPD, what could be the encoding portion of a CuT. Processed data is then sent in an appropriate format to the second DPD in the chain, for example a channel model. After processing by the second DPD, data is sent to the final DPD in the example chain, what could be the decoding portion of a CuT. Data out of this last DPD is finally collected by the data sink. It should be noted that the data type in the different usages of the DPI in Figure 1 does not need to have the same format.

Any number of DPD could be connected in principle, allowing to build complex structures (e.g. to simulate a tandem of codecs in two different digital cellular mobile systems). Other application examples are given in Annex D.

The interface is able to transport in parallel up to 16 bits of Data (D15..D0) from one device (transmitter) to another (receiver). Valid data words are identified by mark bits.

A clock signal is transmitted in parallel with the data lines of the interface in the forward direction (Tx_Clk). A clock signal is also available in the backward direction (Rx_Clk), what can be used for special purposes. An active-low /Reset signal is applied for synchronisation of the devices in a chain.

4.1 Logical Description

Test hardware configurations may differ in each standardisation process. However, the basic format for the data passing through the DPI is the same. It is composed of 16-bit data words, clocked in and out at a certain rate (e.g. 16 kHz) and marked as valid or invalid by a special mark bit, as indicated in Figure 2. The transmission throughout the test configuration is processed synchronously and the mark bit identifies whether the preceding device was ready to send out data or not.

Figure 3 describes a generic hardware structure for the DPI. All data, mark and clock lines are buffered in both transmitter and receiver ends. The data and mark bits are stored in a parallel register during one interface timeslot. The hardware structure is independent of the logic family used, but the same family is needed for a given pair transmitter and receiver interconnected ends. If a termination is needed to reduce signal reflections, it needs to be adequate (and possibly specific) to the logic family chosen.

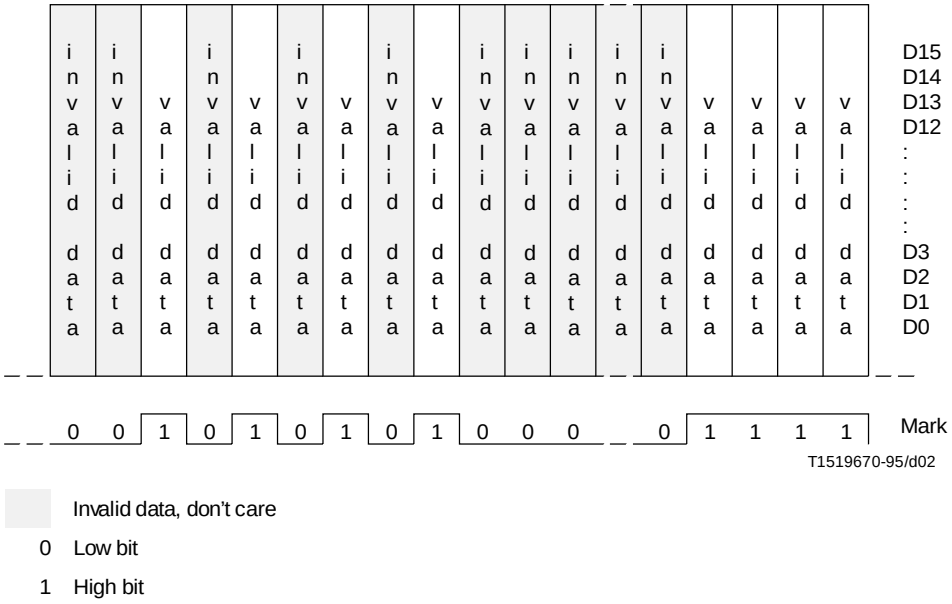


FIGURE 2/G.192

Example for a possible data flow in the DPI

While Figure 3 displays the interface from the point of view of two interconnected devices, Figure 4 displays the interface from a given device's point of view. There it can be seen where the algorithm resides, the data lines it is supposed to use, and how the other control signals are routed inside and through the given DPD. Examples are given in Figure 4 for 3 device setups. This figure is further described in 4.2.

Currently only a TTL (Transistor-Transistor Logic) implementation of the basic hardware has been tested and used. Its description is given in Annex A.

4.2 Master Clock and Reset

The clock signal for devices interconnected by the DPI must be generated by only one device in the chain. This master clock in the simplest case is provided by the data source. In this case, only a clock line in the forward direction is necessary, i.e. from the data source towards the data sink through the interconnected devices.

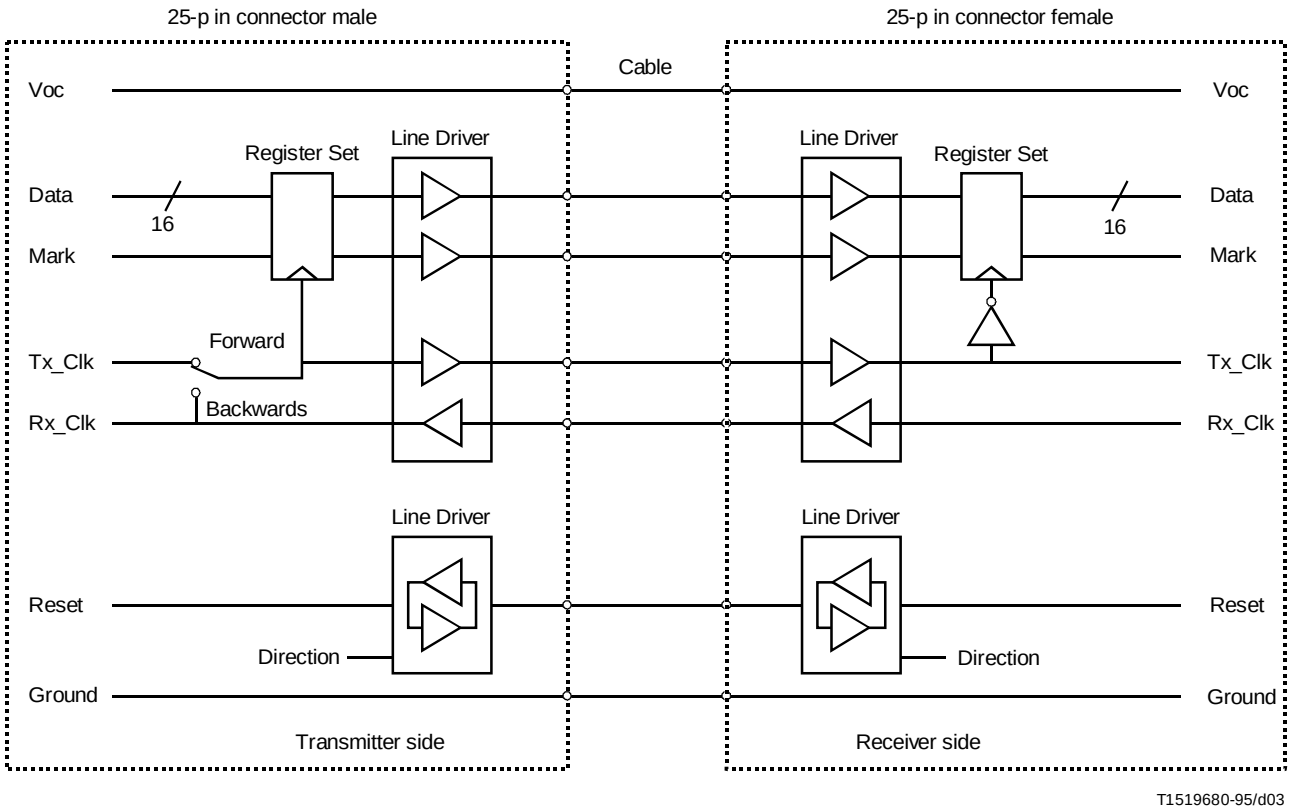


FIGURE 3/G.192

Basic diagram for the hardware implementation of the DPI

In other cases, as illustrated in Figure 4, the master clock may be a device somewhere in the chain. This could occur, for example, in connecting a codec to a real channel. In this situation the channel must provide the master clock and reset, and all other devices must synchronise to the channel. The channel has to generate clocks in the forward direction (Tx_Clk) and in the backward direction (Rx_Clk) through the chain. All devices in the chain must be configured to use either Rx_Clk or Tx_Clk, depending on where the master clock is located. See Figure 4 for an example configuration.

The same holds for the reset signal, which a given device must derive either from its output interface (for devices before the master reset) or from its input interface (devices in forward direction).

4.3 Timing, Timeslots and Capacity

The data and mark bits are clocked out from the transmitter side on the rising edge of Tx_Clk and clocked in at the receiver side on the falling edge of Tx_Clk (see Figure 5).

An "INterface TImeslot" (INTI) is defined as one clock period from rising edge to rising edge of the clock signal. Sixteen data bits, numbered D0 to D15, and one mark bit are transmitted by each INTI. INTIs with mark high (active high) are called "marked", otherwise they are said to be "unmarked".

The functions of the interface are in principle independent from the clock rate, which can be as high as several MHz, constrained by cable lengths and the logic family of the integrated circuits used. For telephony codecs, a 16 kHz clock (Tx_Clk) having a 50% duty cycle will be used in most cases. This gives in principle a total capacity of 256 kbit/s (16 bits × 16 kHz).

If the master device is located within a chain of interconnected devices, as in Figure 4, then its input interface sends the Rx_Clk backwards in the chain. The neighbouring backwards device has to regenerate this clock signal and use it as Tx_Clk. Due to possible phase shifts between Rx_Clk and Tx_Clk, the data and mark bits shall always be triggered with the clock line in the forward direction, Tx_Clk.

4.4 Reset procedure

The reset signal /Reset is an active-low signal whose purpose is to synchronise all the devices in the chain. In normal operation, /Reset shall be inactive (high). The reset signal will be applied by the master reset (e.g. the data source or the channel) to the adjacent device(s) in the chain. For the reset procedure, the steps described below must be followed to guarantee the desired synchronisation. Figure 6 illustrates the signals during the reset procedure.

The reset procedure is initiated by switching the reset signal /Reset to low (active) with the rising edge of Tx_Clk (same as Data and Mark bits).

Every device in the chain has to receive the reset signal at its /Reset input and must regenerate and output the reset signal at its /Reset output (input and output may depend on the location of the master reset).

All devices shall test the reset signal with the falling edge of Tx_Clk (same as data and mark bits) and start or continue their specific reset procedure when /Reset is active (low) at that time.

The reset signal shall remain active for at least 16 clock cycles (1 ms for a 16 kHz clock) and be switched to inactive (high) with the rising edge of Tx_Clk. This is indicated in Figure 6.

The source of data shall wait exactly for another 1600 clock cycles (100 ms for a 16 kHz clock) before the first INTI is marked to transmit the first valid data value (e.g. first sample to a speech encoder). This will be the available time for all devices in the chain to initialise properly and to be ready for processing.

5 Hardware implementation

5.1 Connector type, pin assignment and cabling

At the transmitter side there is a 25 pin Sub-D male connector and at the receiver side there is a 25 pin Sub-D female connector. Table 1 shows the pin assignment for the digital parallel interface.

It is advisable to use a cabling strategy that maximises noise rejection. For reducing the influence of noise, it is recommended to use twisted-pair parallel conductors with the pin assignment of Table 1. In this case, signals Mark, /Reset, Tx_Clk, and Rx_Clk should be twisted with ground especially in the case of regular to long cable lengths.

5.2 Line drivers and receiver termination

Because all data, mark, reset, and clock lines should be driven by equivalent line-drivers for the applied signalling voltage, there should be an adequate line termination to avoid reflections. The kind of termination will depend on the logic family. Annex A gives a specification for the TTL family.

5.3 Distributed multiplexer

The termination networks shall not be placed inside the receiving devices, but externally at the far end(s) of the cable. This makes possible the connection of more than one receiver to the same line, provided that only one is enabled at a given time, while the others are tri-stated.

Both features together (external termination networks and tri-stated buffers) can be used to implement distributed multiplexers and demultiplexers. This function can be used, for example, for the randomisation of the speech material in subjective tests.

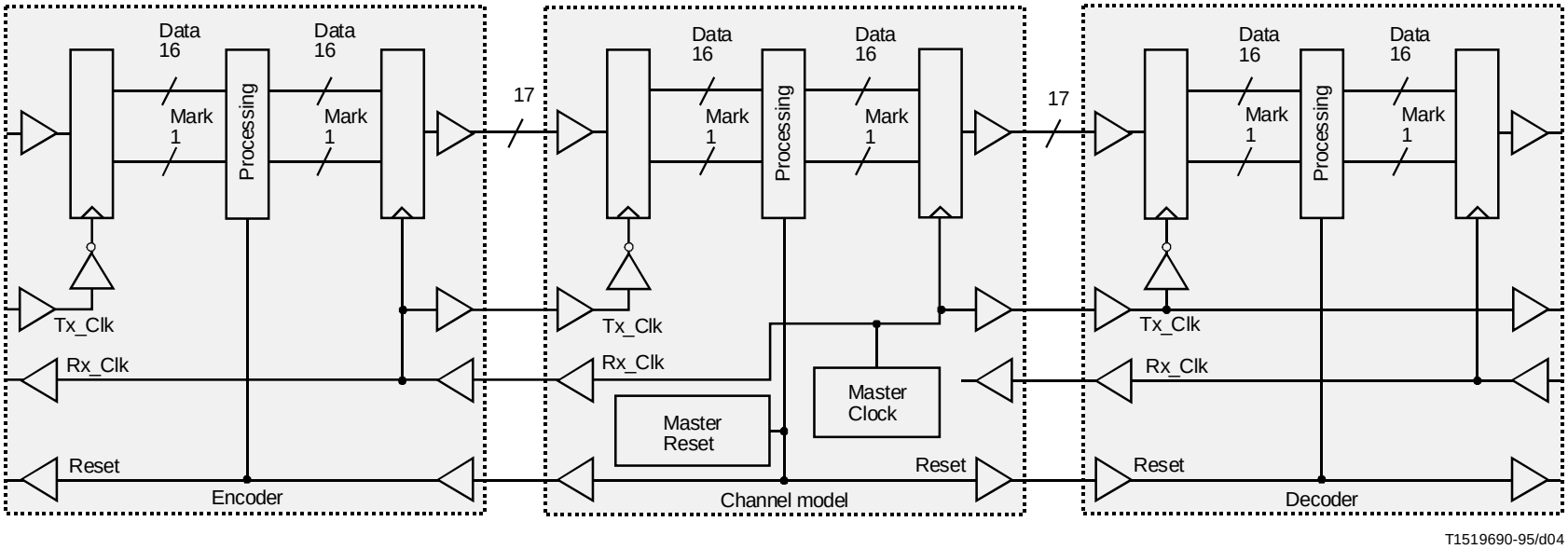
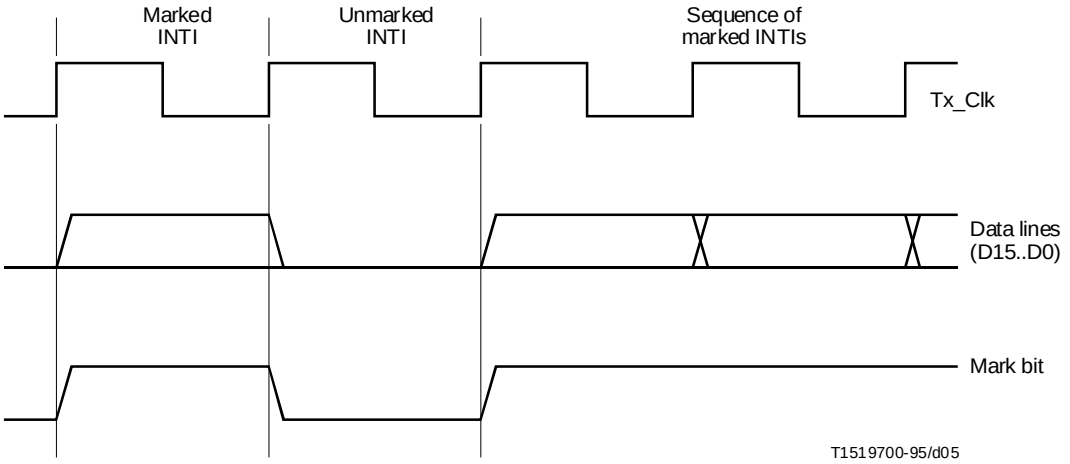


FIGURE 4/G.192

Example for usage of the Rx_Clk when the master clock lies inside the device chain – in this case, in the channel model



INTI INterface TImeslot

FIGURE 5/G.192

Example of interface Timing

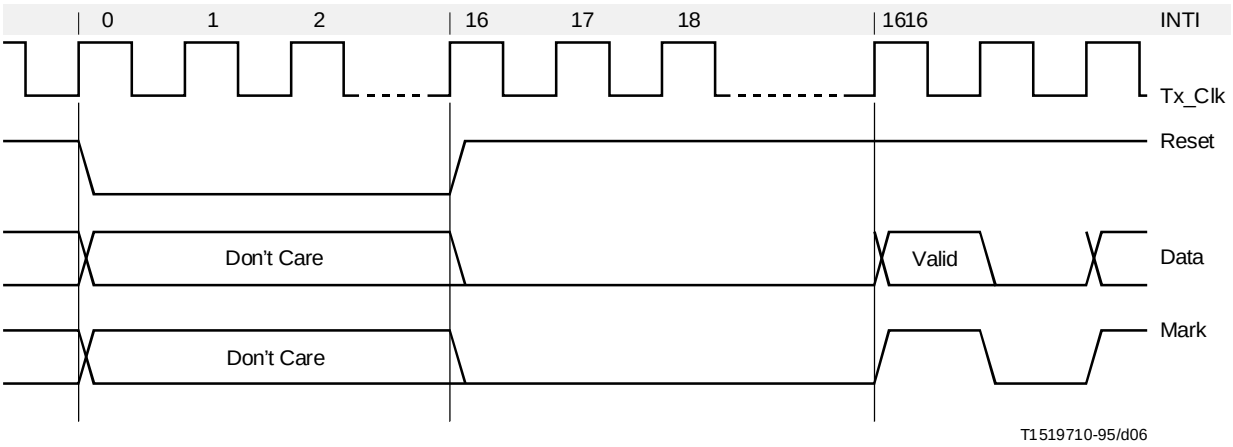


FIGURE 6/G.192

Timing during the reset procedure (output of the source of data)

Additional functionality can be added to the DPI by using pins 22, 23, and 24 as device address lines, instead of being grounded. This extended configuration allows the interface to be used as a simple data bus. Because these lines would usually represent ground twisted with the clock lines, this may introduce a loss in noise rejection[1)]. The advantages of the use of address lines are the automatic selection by the data source of one out of several devices in a distributed multiplex configuration.

To allow downward compatibility with existing devices, the address 0 shall be defined as "all devices selected" because this is electrically equivalent as having pins 22, 23, and 24 as ground. There is therefore address space for up to seven different devices in a multiplex configuration. Address line A0 is assigned to pin 24, A1 to pin 23, and A2 to pin 22.

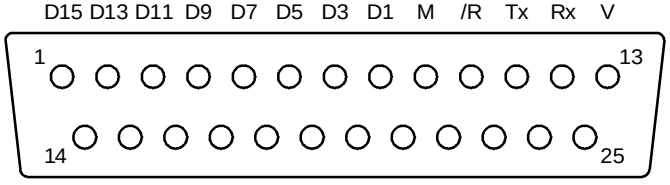
1) Further study is necessary in this topic to determine environmental and cabling conditions to assure reliable operation.

TABLE 1/G.192

Pin assignment for the Digital Parallel Interface

Pin	Signal name	Pin	Direction	Pin	Signal name	Pin
	D15	1	→	1	D15	
14	D14		→		D14	14
	D13	2	→	2	D13	
15	D12		→		D12	15
	D11	3	→	3	D11	
16	D10		→		D10	16
	D9	4	→	4	D9	
17	D8		→		D8	17
	D7	5	→	5	D7	
18	D6		→		D6	18
	D5	6	→	6	D5	
19	D4		→		D4	19
	D3	7	→	7	D3	
20	D2		→		D2	20
	D1	8	→	8	D1	
21	D0		→		D0	21
	Mark	9	→	9	Mark	
22	Ground/A2		Gnd/→		A2/Ground	22
	/Reset	10	(←) →	10	/Reset	
23	Ground/A1		Gnd/→		A1/Ground	23
	Tx_Clk	11	→	11	Tx_Clk	
24	Ground/A0		Gnd/→		A0/Ground	24
	Rx_Clk	12	←	12	Rx_Clk	
25	Ground				Ground	25
	+5 V/2 Ω	13		13	Not connected	
Digital Output Interface Male connector view onto the pins				Digital Input Interface Female connector view onto the holes		

D15-D0	16 data bit in parallel (D15 = MSb; D0 = LSb)
A2-A0	Optional 3-bit address running in the forward direction
Mark	Additional bit for special purposes
Tx_Clk	Forward direction clock signal
Rx_Clk	Backwards direction clock signal
/Reset	Low-active reset signal to/from that device
+5 V/2 Ω	Power supply for the termination network with a 2 Ω series resistance
Gnd/→	Either ground connection or the address line in the forward direction



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M Mark /R /Reset Tx Transmit clock Rx Receive clock
V Power G ground
(Male connector)

The address lines are active all the time, and the devices shall check the selection every falling edge of the Tx_Clk, and the data source shall change it on the rising edge of the Tx_Clk of an unmarked INTI. Unselected devices can either continue running as if the input is zero-valued, or just freeze. This is for further study.

In the case these lines are used as address bits, they shall be buffered and have terminations as done for the data, mark, clock, and reset lines, always in the forward direction, as indicated in Table 1. If this feature is not used, these lines should be directly connected from the input to the output of the device.

5.4 Signal delays within devices

Devices which receive data at their input, process them and deliver data at their output, must handle the clocks and the reset signal in the way described, to ensure proper operation in the complete chain of devices.

The clock signals Tx_Clk and Rx_Clk and the reset signal /Reset must be regenerated inside the devices and forwarded at the other end. The delay for these signals within the device shall be as low as possible (e.g. as low as the delay of two SN74LS245, i.e. up to 20 ns). This will guarantee proper phase relationship between all signals in practical applications and will simplify the timing for interconnecting master and slave devices.

Annex A

DPI implementation using TTL logic integrated circuits

(This annex forms an integral part of this Recommendation)

Figure A.1 shows the hardware implementation of the DPI from the point of view of interconnected devices using standard TTL (Transistor-Transistor Logic) integrated circuits.

All data, mark and clock lines are driven by simple TTL-drivers of type SN74LS245. For the parallel data register a SN74LS273 is used. Equivalent integrated circuit types may be used, but care has to be taken in this case.

The 5 V/2 Ω power supply is provided by the transmitter for the sole purpose of feeding the line termination network at the receiver side. Since termination networks are external to the interface, this line shall not be connected electrically on the receiver side.

A special kind of cable termination is needed to avoid signal reflections. For cable lengths between 2 and 10 meters, all lines shall terminate at the destination (receiving) end of the signal with a passive network of 330/470 Ω to +5 V/Ground respectively. This is the reason why, in Figure A.1, all the signals in the forward direction are terminated at the receiver's side, while the only backward-direction signal, Rx_Clk, is terminated at the transmitter's side.

For short cable lengths (less than 2 meters) the termination may be omitted. For very long cables (more than 10 meters), termination networks may be necessary at both ends of the lines.

SW1 in Figure A.1 connects Tx_Clk to the position labelled forward when the transmitter side of a DPD is in the forward direction, and to the position labelled backward when the transmitter side is in the backwards direction respective to the master clock. See Figure 4 for connection examples.

Signals Dir and $\overline{G}_R$ are generated internally by each DPD in the chain. Signal Dir indicate whether the DPD is in the forward direction ('0') or in the backwards direction ('1'). Signal $\overline{G}_R$ is an active-low signal that defines whether the DPD is enabled or disabled. $\overline{G}_R$ is generated from the address lines if the bus mode of the DPI is used. If the bus mode feature is not to be used, $\overline{G}_R$ shall be connected to ground.

To help understand the description of the interface, the DPI is described in Figures A.2A and A.2B for a given DPD. Figure A.2A describes the DPI implementation for a device which is not a master clock/reset. This device will be operating in the forward direction if switch SW1 is in position F and in the backward direction if it is in position B. Figure A.2B describes the DPI implementation for a master-clock-and-reset device.

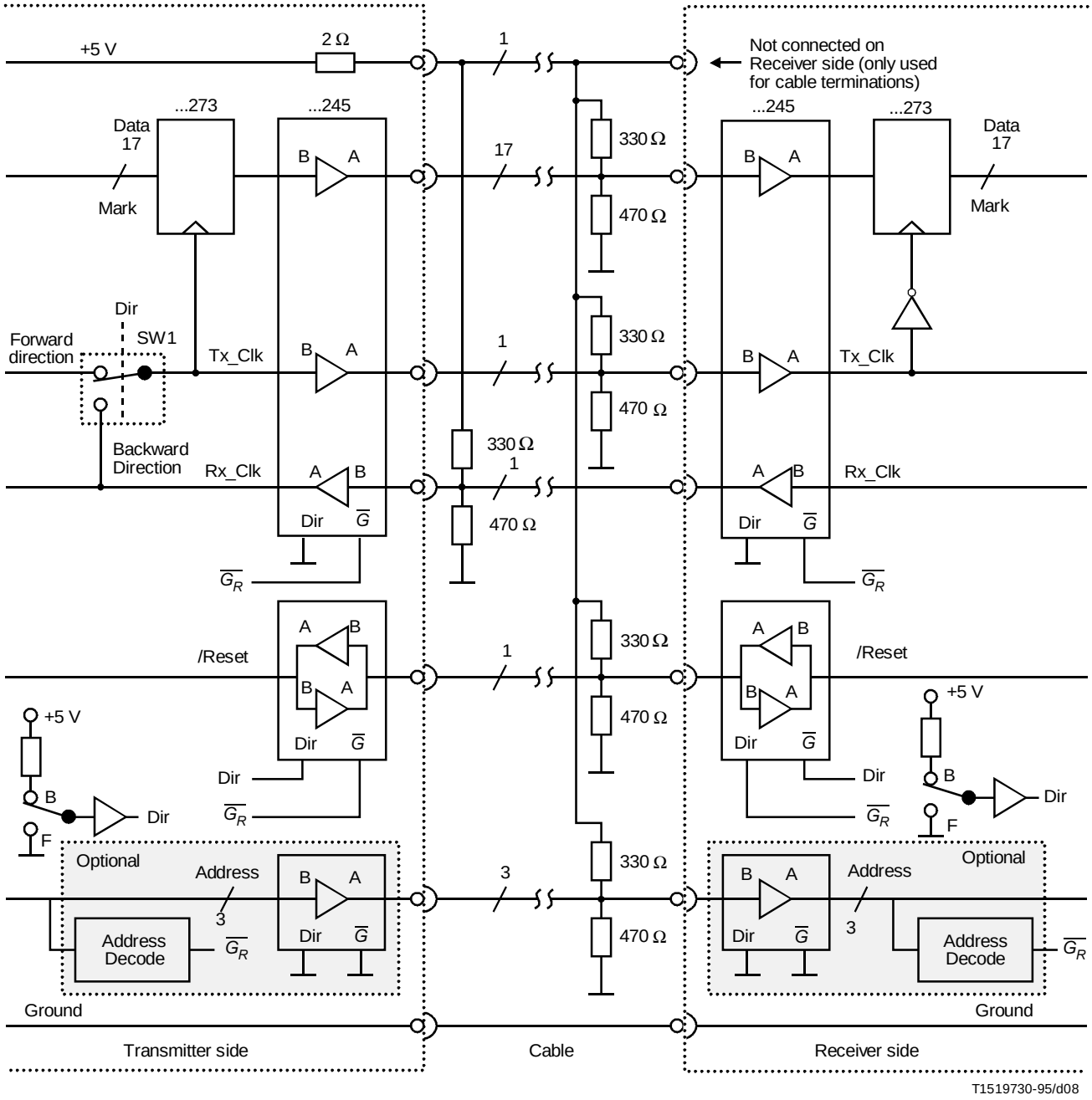


FIGURE A.1/G.192

Basic configuration hardware interface diagram for two interconnected DPT – The address lines of the extended configuration are optional (see main body of this Recommendation for details) – Signals Dir and $\overline{G_R}$ are generated by each DPD in the chain

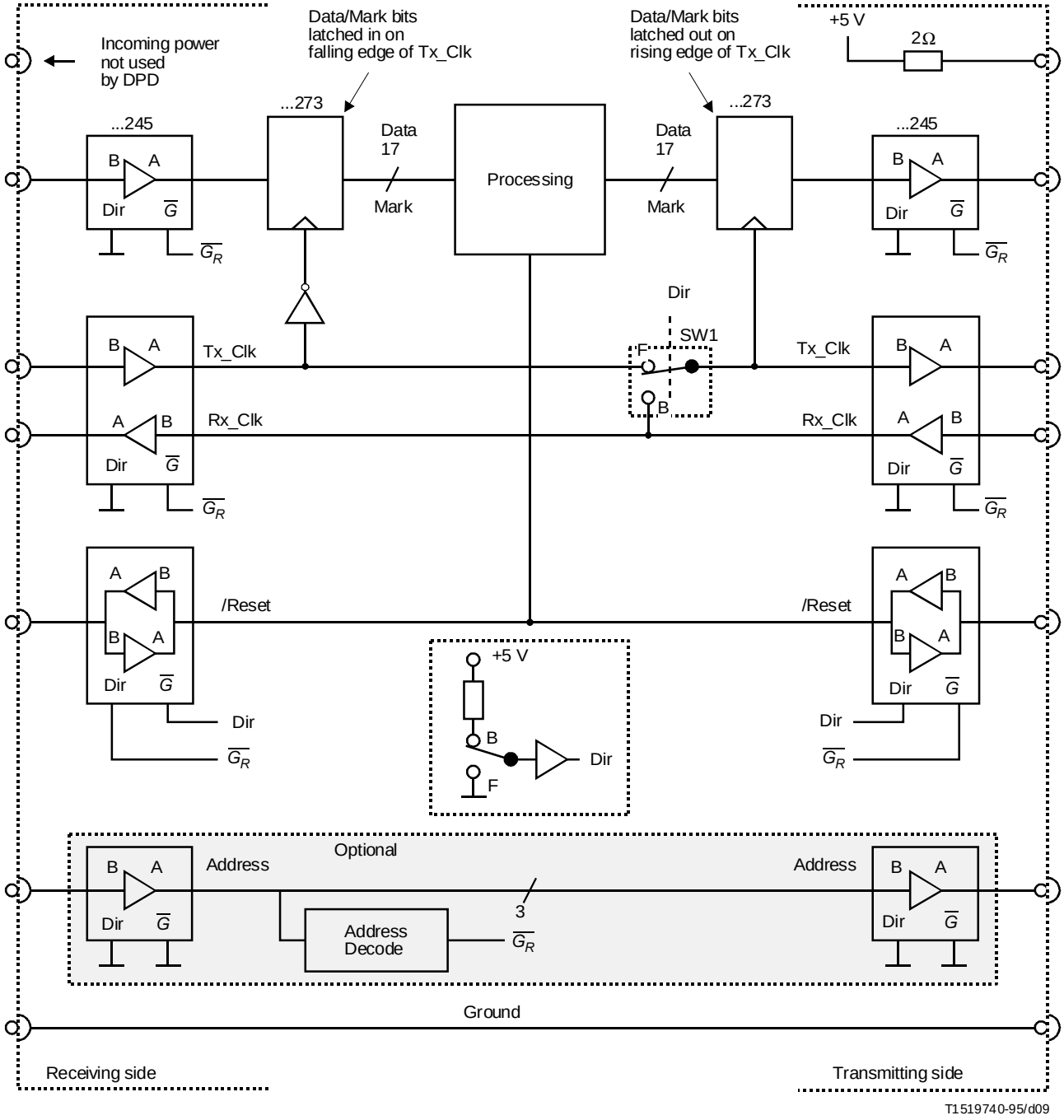


FIGURE A.2A/G.192

Basic configuration hardware interface diagram for a given DPD when the device is not the master clock/reset – If switch SW1 is in position B, the device will be operating in the backward direction, and SW1 is in position F, the DPD will be operating in the forward direction

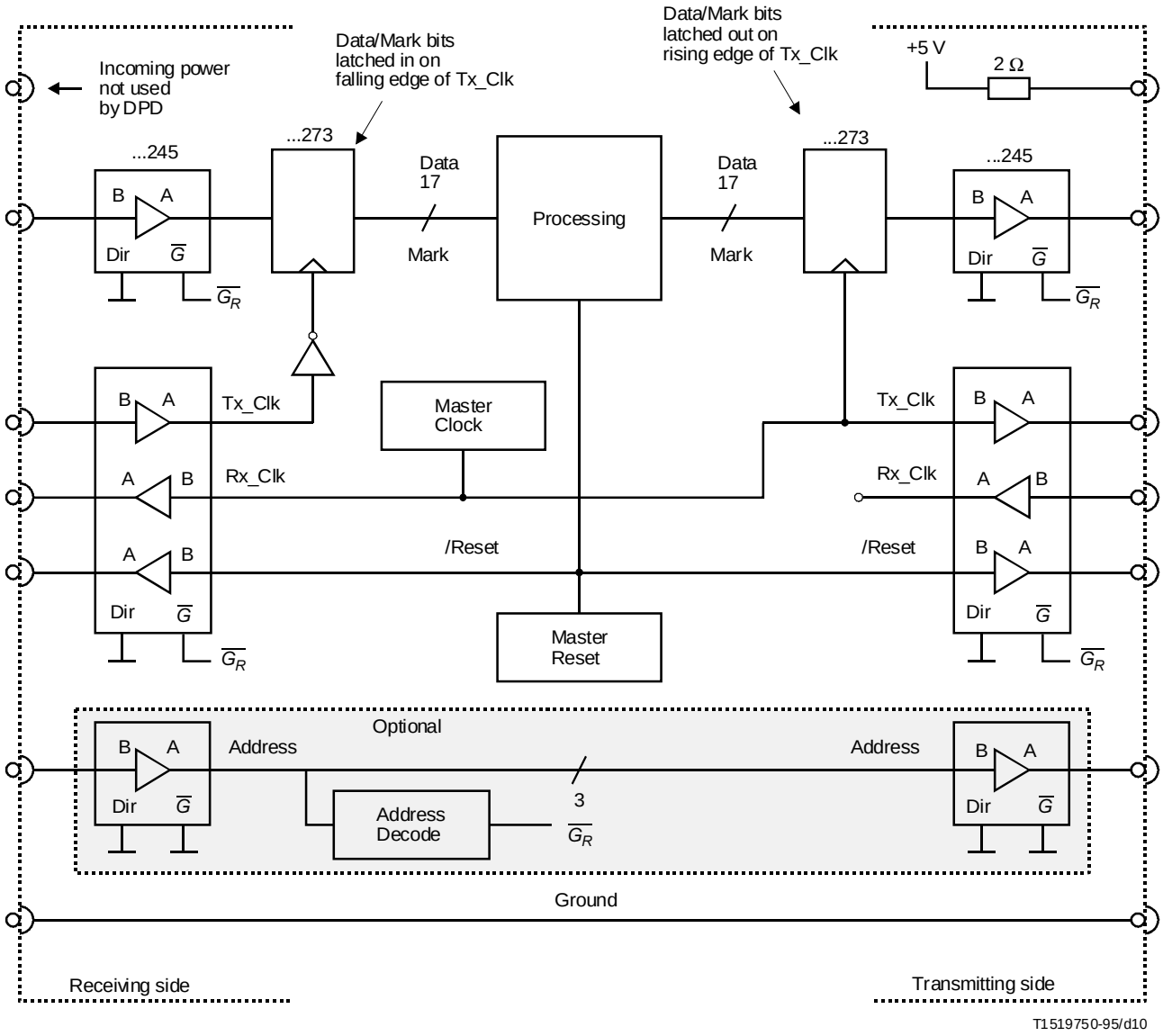


FIGURE A.2B/G.192

Basic configuration hardware interface diagram for a master clock/reset DPD – This device will generate the forward clock (Tx_Clk) – and backward clock (Rx_Clk), as well as the /Reset signal, for the interconnected DPD – The Tx_Clk used by the Master DPD comes from the preceding DPD, which has regenerated Rx_Clk as its Tx_Clk

Annex B

Data formats

(This annex forms an integral part of this Recommendation)

The DPI is capable of transporting different data structures between different devices without any changes in the physical and electrical specifications. However, different data formats and protocols have to be defined for higher layer operation.

Currently, only two types of data are defined: time signals (representing, e.g. speech samples) and coded bitstreams (representing, e.g. codec parameters). The following is the description of the structure of these data types.

B.1 Time signals

Time signals shall be transported in the format described below at the input of an encoder and the output of a decoder. This guarantees that different interconnection configurations can be used.

The data representation is a left-justified, 16-bit 2's complement format, i.e. the most significant bit is always bit D15. If a bit resolution b other than 16-bit is required, the (16-b) least-significant bits shall be set to zero. This is also the convention adopted for the integer number representation by the ITU-T Software Tool Library defined in Recommendation G.191.

The sampling frequency should be set to 8 kHz for the general case of telephony codecs. It should be noted that the sampling frequency is independent of the clock-rate signal (Tx_Clk or Rx_Clk) and can be higher than the sampling rate (e.g. 16 kHz for a telephony codec).

Whenever a sample is transported by means of the digital interface, the mark bit is set (high).

The data structure of a sampled data is defined by a marked INTI always followed by an unmarked INTI. This is done to allow real-time processing by the devices in the chain during speech sentences. Multiple unmarked INTIs in a row are only allowed between completely processed materials (e.g. between the end of a speech file and the start of the next one), because at that time there will be no time signals to be transported by the DPI. This simplifies the data handling inside the data source and the data sink. Further data structuring for the DPI time signal representation is not required at this level. See Figures B.1 and B.2.

As described above, after applying the reset procedure, the encoder receives the first sample from the data source. All other samples will follow in the defined data structure, until the processing of the whole data is terminated. Figure B.1 illustrates a possible data flow where each sample has a 13-bit resolution.

NOTE – For objective measurements (such as for voiceband data) the data source and sink can be an A/D and D/A converter device. This will use exactly the same data format. Also, the data format makes it possible to connect the data source directly to the data sink, e.g. for hardware verification purposes.

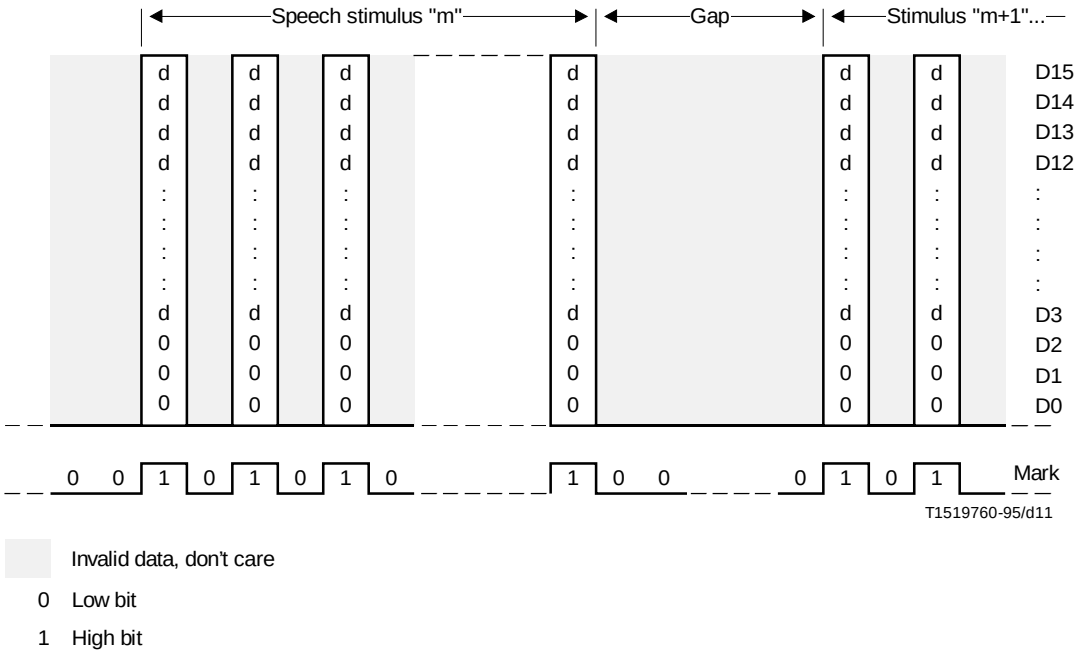


FIGURE B.1/G.192

Example of a time signal representing a sampled data with 13-bit resolution (left-justified)

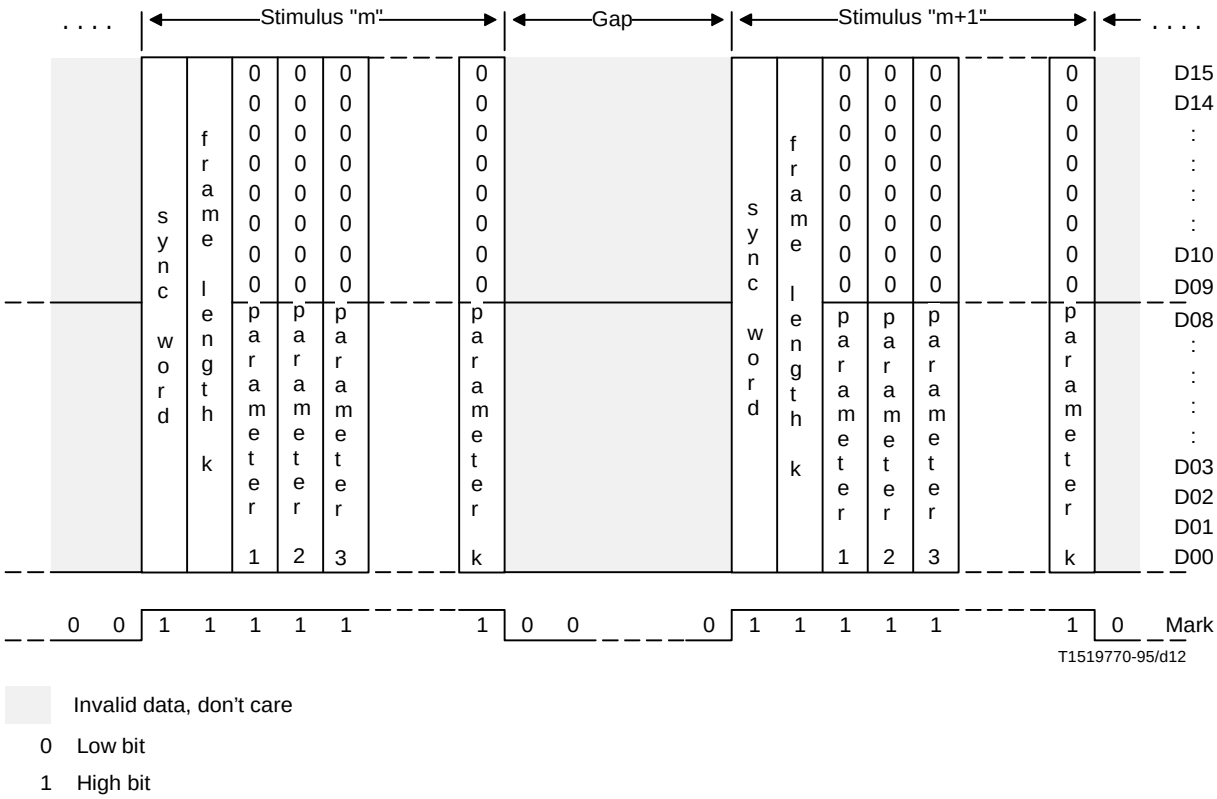


FIGURE B.2/G.192

Example of a coded bitstream signal representing a data frame of k softbits, preceded by a synchronization word and its length k (all right-justified)

B.2 Coded bitstream

When DPDs are implementations of the encoder portion of a codec, their output DPI will represent a coded bitstream. The same happens with the input DPI of a DPD implementing a decoder.

In order to enable the DPI to transport different bitstream formats without electrical or physical changes, it is necessary to define a flexible format.

Each bit of the bitstream data is represented as a 16-bit word, preceded by a synchronization word and a frame length word. This enables the implementation of the concept of "softbits", what permits easy introduction of synchronisation words in the bitstream, and allows for the use of probabilistic models to hit samples or frames by errors of several types (e.g. random, burst, as well as frame erasure errors).

The recommended definition for the softbits is given in the ITU-T Software Tool Library Manual. The bits out of an encoder are coded as 256-level softbit words. A bit '0' is coded as the softbit 0x007F and a bit '1' as the softbit 0x0081. Data at the decoder with these values are taken as correct, while other values in the range of 0..255 are taken as samples with an associated chance of being in error. The (hard) information of the softbit can be seen in the MSb of the 8-bit softbit data. Softbits in the range 0x6B21..0x6B2F are used as synchronisation words. The four LSbs of the synchronisation words are used to distinguish between the different kinds of synchronisation words that may appear in a system. A synchronisation word of 0x6B20 is the bad-frame indicator. The length word is always right-adjusted and its value will depend on the frame size and on the codec data rate. For example, the length word will be 80 (0x0050) for an 8 kbit/s codec with a frame size of 10 ms.

Figure B.2 illustrates a coded bitstream layout, where the bitstream has k (soft) bits and every frame is preceded by a synchronisation word and its length k (all right-justified).

Annex C

Rules for codec implementation

(This annex forms an integral part of this Recommendation)

As described in Annex B, an undefined number of unmarked INTIs may occur at the digital output interface of the digital data source at any time, in order to simplify the file handling inside the data source and sink. Therefore, an encoder in the chain must not synchronise to the Tx_Clk (which will be a continuously running clock, providing the transport medium), but rather to the Mark bit at its input (see Figure 4). For every received Mark bit another sample has to be shifted into the input buffer of the encoder and processed according to the encoding algorithm.

The encoder output must transmit only valid and complete encoded frames. The Mark bit must be set accordingly as illustrated in Figure B.2.

To guarantee proper start up after reset and to keep the delay to a minimum, all variables within the encoder should be reinitialised during the reset procedure. Reinitialising means setting all variables to values as if there would have been a 0-sample input sequence for an infinitely long time before the first sample from the control system or conditioning device is received. Possible exceptions to this rule are variables defined by the implementor as having a special initial reset value at the encoder.

Devices that manipulate the encoded frame bitstream (e.g. error insertion devices) may introduce short delays of a few INTIs in the processing chain in order to synchronise their operation with a synchronisation word in the bitstream.

Similarly to the encoder, the decoder must synchronise to the Mark bit at its input interface, process the received encoded word or frame and output its first valid sample when it is available. Before this event, only unmarked INTIs must be generated. The decoder should assume again an infinitely long sequence on "encoded silence" (0-sample sequence) before the first valid bitstream is received after reset. Again, possible exceptions to this rule are variables defined by the implementor as having a special initial reset value at the decoder. The decoder has to ensure that within a given speech stimulus (e.g. a speech file provided by a computer acting as data source), data will be output every other INTI without gaps (see Figure B.1).

NOTES

1 This synchronisation protocol allows for real-time measurements using A/D and D/A converters, such as for voiceband data performance evaluation. The data sink will take the first sample emerging from the output of the decoder as the response to the first sample at the input of the encoder.

2 By measuring the time interval between these two instants, one can derive an estimate of the signal delay for the chain "encoder, bit-manipulation devices and decoder".

Annex D

Example host laboratory test configurations

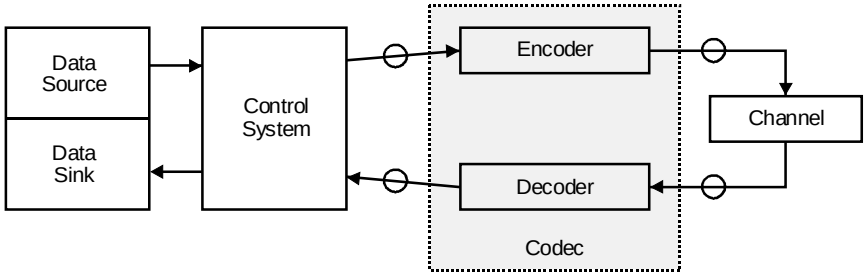
(This annex forms an integral part of this Recommendation)

In general, in a test configuration there will be a control system that issues control signals to the interconnected devices, what also operates as the source and sink of data. The interconnected devices may be, for example, an encoder and its decoder connected by a hardware model of the transmission channel. This is represented in Figure D.1 a).

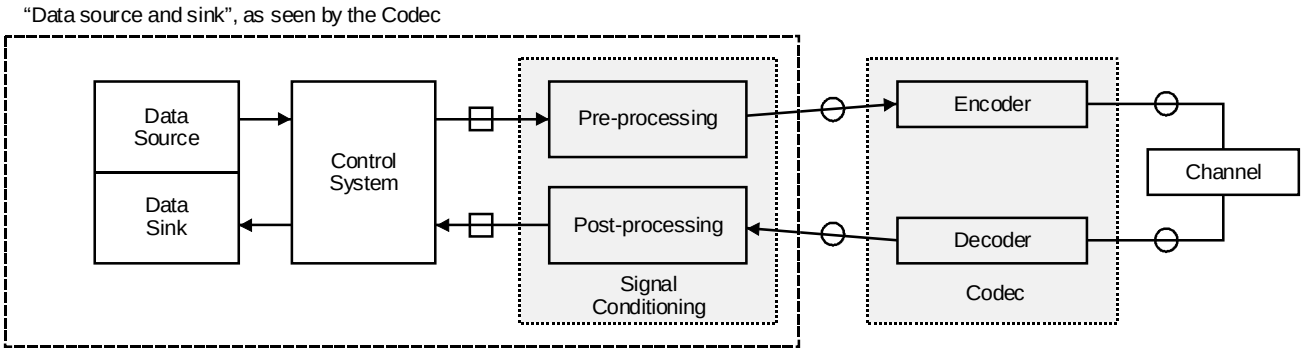
Another configuration could be to have a signal conditioning device in between the control system and the codec, in order to perform pre- and post-processing of the source and sink data, respectively. This configuration is shown in Figure D.1 b).

When measuring the performance of a system for analogue signals, it may be necessary that the source of data be an A/D converter, and the sink of data a D/A converter. This is the case for carrying out voiceband data measurements. This is shown in Figure D.1 c).

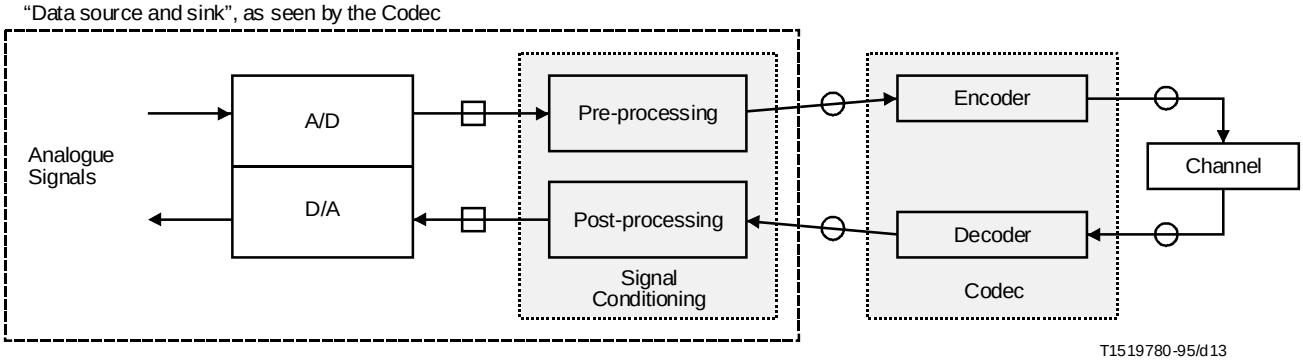
The interface of this Recommendation has been defined to be flexible enough to accommodate a wide range of configurations that usually appear in the evaluation processes of ITU-T standardisation activities.



a) Configuration without a signal conditioning device



b) Configuration with a signal conditioning device



c) Configuration with signal source from an A/D converter

FIGURE D.1/G.192

Example reference configurations for interconnecting devices using the digital parallel interface – The circles represent the digital parallel interface data paths and the squares a potentially specialised, high-performance interface (as used in the ITU-T 8 kbit/s codec Host Laboratory)

Appendix I

The ITU-T 8 kbit/s speech codec test parallel interface

(This appendix does not form an integral part of this Recommendation)

It was decided to use a full digital approach in the host laboratory session for the evaluation of the subjective speech quality of codec candidates for the ITU-T 8 kbit/s coder selection test.

In the hardware setup used by the host laboratory, the "Host Laboratory Control System" (HLCS) was used as data source and data sink. The HLCS sends out stimulus data (test sentences) by means of a "Signal Conditioning Device" (SCD) to the (speech and channel) encoder under test and collect the output of the (speech and channel) decoder (resynthesised speech). Selection of stimulus data, control of the SCD and the "Error Insertion Device" (EID), and randomisation of processed sentences are done by software inside the HLCS. The error insertion device was used to implement the radio channel model.

Figure I.1 gives an overview and shows the devices in the chain of the data flow.

All interfaces at the inputs and outputs of the codec candidate under test, illustrated in Figure I.1, are completely digital and of the same type.

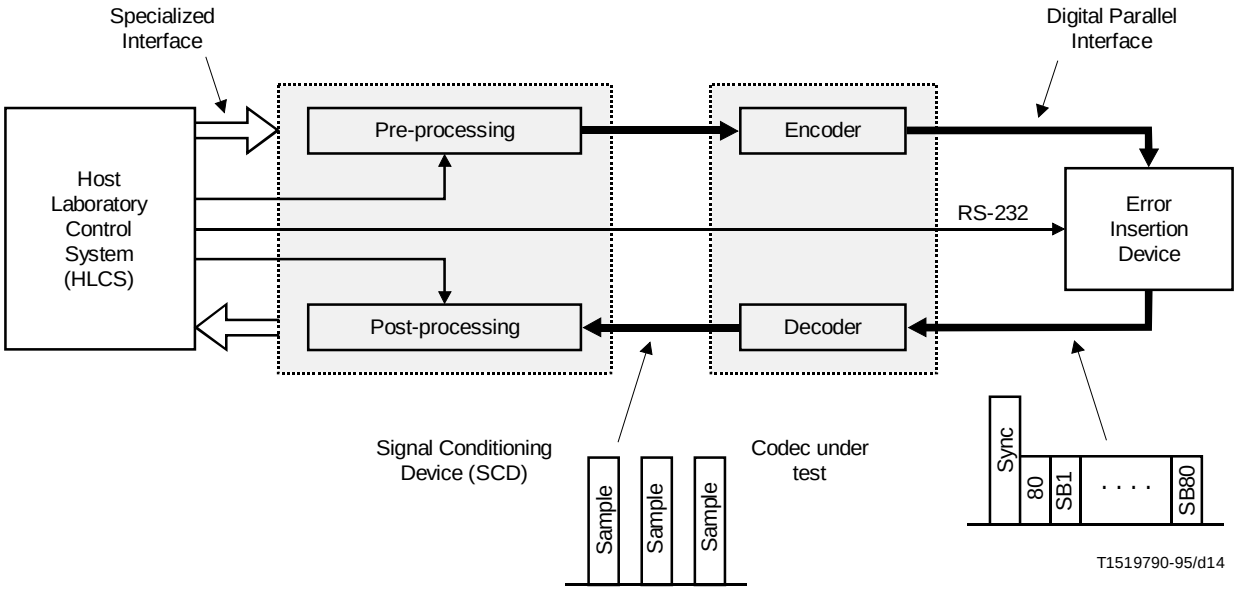


FIGURE I.1/G.192

Data flow for host laboratory session

I.1 Specialisation of the interface

The host laboratory for the selection tests of the ITU-T G.729 8 kbit/s speech coder used the DPI defined in this Recommendation. Not all functions of this interface were necessary in the host laboratory sessions of the codec selection and of the codec characterisation tests.

To simplify the interface as much as possible, the following specialisations were defined:

i) Only one transmitter was connected to only one receiver. No distributed multiplexing was used. All line drivers at the transmitter and receiver side were always enabled.

ii) Only Tx_Clk was used throughout the tests; Rx_Clk was not used (the HLCS device was the master clock source).

iii) /Reset was used only in the forward direction (the HLCS was the master reset source).

iv) Only marked INTIs held valid data. The data bits in unmarked INTIs were set to '0' at the transmitter side and were not considered at the receiver side.

v) The source and sink of data was the HLCS/SCD (for processing of the speech material) or equivalent A/D and D/A converters (for objective measurements with voiceband data).

I.2 Data formats

Time signals. The 8 kbit/s coder selection host laboratory configuration used the time signal format between the SCD and the codecs under test.

Bitstream signals. For the signals between the EID and the codecs under test, a bitstream format with length word equal to 80 (01010000 in binary) was used. This bitstream format is illustrated in Figure I.2. In the event of frame erasures, the EID did not change the synchronisation word 0x6B21 to 0x6B20, but changed all the softbits in the frame to 0x0000 to indicate loss of information.

Both definitions allowed the bypassing of the EID or of the codecs, for verification of the adequate operation of the system.

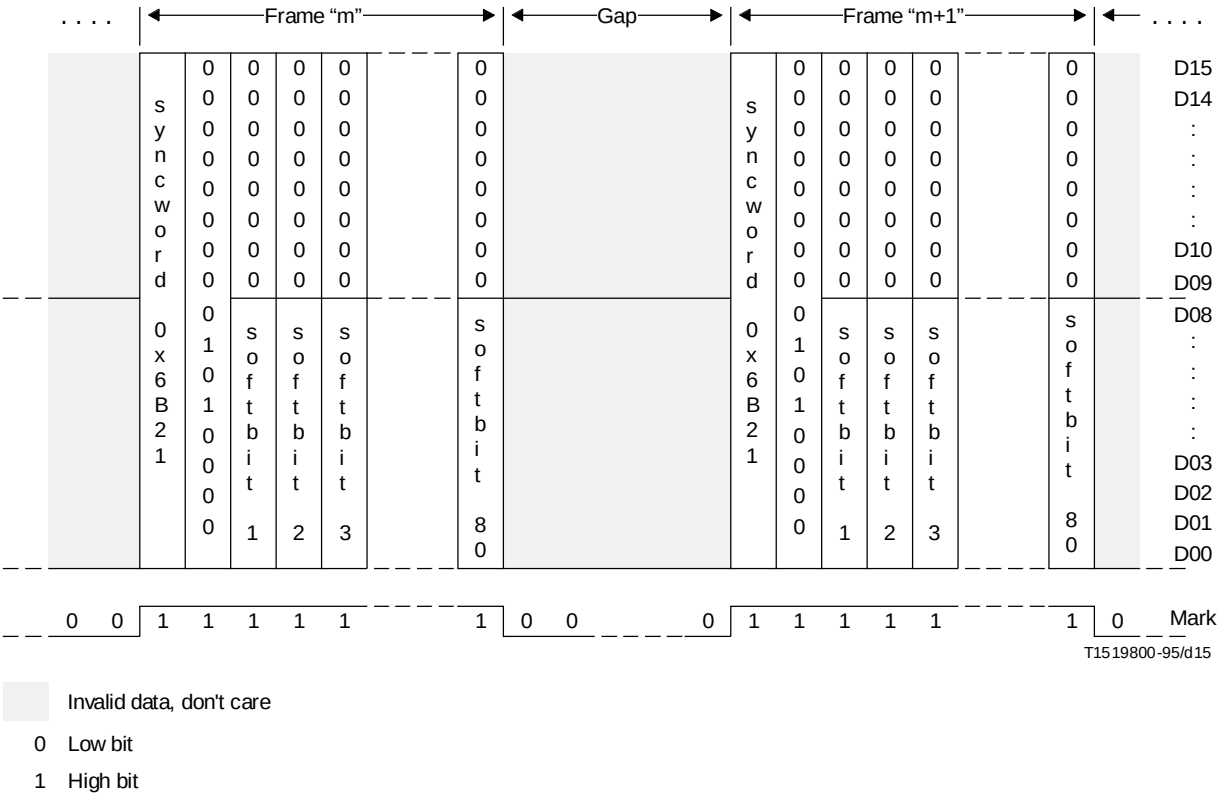


FIGURE I.2/G.192

Channel signal representing the 8 kbit/s codec encoded bitstream for a 10 ms speech frame length

References

– ITU-T Recommendation G.191 (1993), *Software tools for speech and audio coding standards.*

– ITU-T Recommendation G.729 (1996), *Coding of speech at 8 kbit/s using conjugate-structure algebraic-code-excited linear-prediction (CS-ACELP).*