IEEE Std 802.3af™-2003
(Amendment to IEEE Std 802.3™-2002,
including IEEE Std 802.3ae™-2002)

IEEE Standards

802.3af™

IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment: Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

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Approved 12 June 2003
IEEE-SA Standards Board

Abstract: Support for optionally powering a 10BASE-T, 100BASE-TX or 1000BASE-T DTE device via the Power Interface (PI) using physical layers defined in Clauses 14, 25, and 40. The Power Sourcing Equipment (PSE) is located at an endpoint or midspan, separate from and between the MDIs, and provides power to the Powered Device (PD) over the Link Section. The PSE detection protocol distinguishes a compatible PD from non-compatible devices and precludes the application of power and possible damage to non-compatible devices. The PSE monitors the Maintain Power Signature (MPS) and removes power when it is no longer requested or required. Optional management function requirements are specified.

Keywords: 802.3af, Link Section, midspan, MPS, PD, PI, POE, power, Power over Ethernet, PSE

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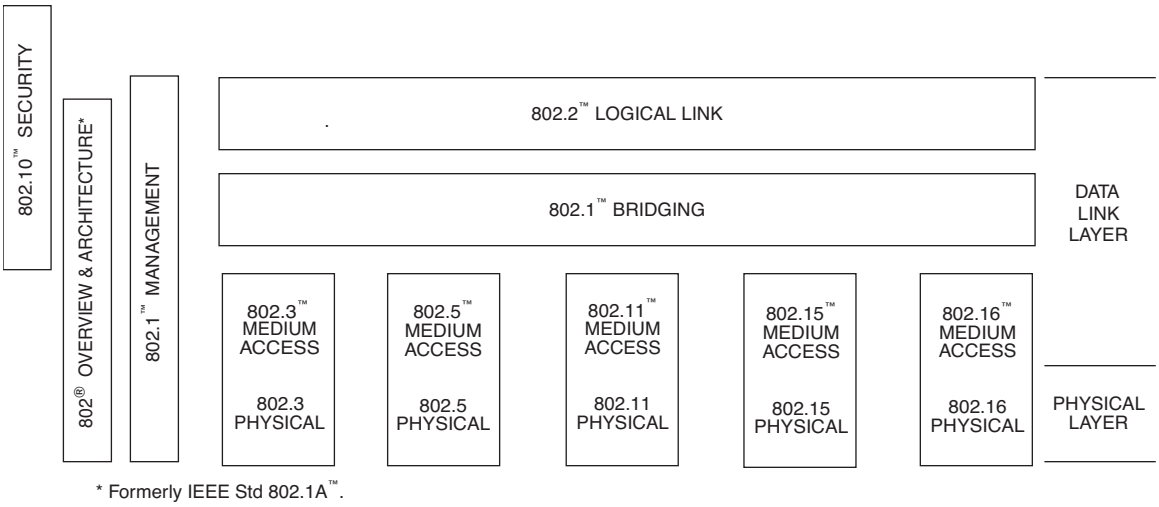
Introduction to IEEE Std 802.3af-2003

[This introuduction is not part of IEEE Std 802.3af-2003, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks— Specific requirements CSMA/CD Access Method and Physical Layer Specifications Amendment: Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)]

This amendment is part of a family of standards for local and metropolitan area networks. The relationship between the standard and other members of the family is shown below. (The numbers in the figure refer to IEEE standard numbers.[1])



This family of standards deals with the Physical and Data Link layers as defined by the International Organization for Standardization (ISO) Open Systems Interconnection (OSI) Basic Reference Model (ISO/IEC 7498-1: 1994). The access standards define five types of medium access technologies and associated physical media, each appropriate for particular applications or system objectives. Some access standards have been withdrawn and other types are under investigation.

The standards defining the technologies noted above are as follows:

- IEEE Std 802[2] — *Overview and Architecture*. This standard provides an overview to the family of IEEE 802 Standards.
- IEEE Std 802.1B™ and 802.1k™ [ISO/IEC 15802-2] — *LAN/MAN Management*. Defines an OSI management-compatible architecture, and services and protocol elements for use in a LAN/MAN environment for performing remote management.
- IEEE Std 802.1D™ — *Media Access Control (MAC) Bridges*. Specifies an architecture and protocol for the interconnection of IEEE 802 LANs below the MAC service boundary.
- IEEE Std 802.1E™ [ISO/IEC 15802-4] — *System Load Protocol*. Specifies a set of services and protocol for those aspects of management concerned with the loading of systems on IEEE 802 LANs.

[1]The IEEE standards referred to in the above figure and list are trademarks owned by the Institute of Electrical and Electronics Engineers, Incorporated.

[2]The IEEE 802 Overview and Architecture Specification, originally known as IEEE Std 802.1A, has been renumbered as IEEE Std 802. This has been done to accomodate recognition of the base standard in a family of standards. References to IEEE Std 802.1A should be considered as references to IEEE Std 802.

- IEEE Std 802.1F™ — *Common Definitions and Procedures for IEEE 802 Management Information*.
- IEEE Std 802.1G™ [ISO/IEC 15802-5] — *Remote Media Access Control (MAC) Bridging*. Specifies extensions for the interconnection, using non-LAN communication technologies, of geographically separated IEEE 802 LANs below the level of the logical link control protocol.
- IEEE Std 802.1H™ [ISO/IEC TR 11802-5] — *Media Access Control (MAC) Bridging of Ethernet V2.0 in Local Area Networks*.
- IEEE Std 802.2 [ISO/IEC 8802-2] — *Logical Link Control*.
- IEEE Std 802.3 — *CSMA/CD Access Method and Physical Layer Specifications*.
- IEEE Std 802.5 [ISO/IEC 8802-5] — *Token Ring Access Method and Physical Layer Specifications*.
- IEEE Std 802.10 — *Interoperable LAN/MAN Security*.
- IEEE Std 802.11 [ISO/IEC DIS 8802-11] — *Wireless LAN Medium Access Control (MAC) and Physical Layer Specifications*.
- IEEE Std 802.15 — *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for: Wireless Personal Area Networks*.
- IEEE Std 802.16 — *Standard Air Interface for Fixed Broadband Wireless Access Systems*.

In addition to the family of standards, the following is a recommended practice for a common Physical Layer technology:

- IEEE Std 802.7™ — *IEEE Recommended Practice for Broadband Local Area Networks*.

Conformance test methodology

An additional standard, IEEE Std 1802.3™ provides conformance test information for 10BASE-T.

IEEE Std 802.3af-2003

This standard contains state-of-the-art material. The area covered by this standard is undergoing evolution. Revisions are anticipated to this standard within the next few years to clarify existing material, to correct possible errors, and to incorporate new related material.

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Special symbols and operators

Printed Character	Meaning	Frame V character code	Font
*	Boolean AND	ALT-042	Symbol
+	Boolean OR, Arithmetic addition	ALT-043	Symbol
^	Boolean XOR	^	Times
!	Boolean NOT	ALT-033	Symbol
<	Less than	ALT-060	Symbol
≤	Less than or equal to	ALT-0163	Symbol
=	Equal to	ALT-061	Symbol
≠	Not equal to	ALT-0185	Symbol
≥	Greater than or equal to	ALT-0179	Symbol
>	Greater than	ALT-062	Symbol
⇐	Assignment operator	ALT-0220	Symbol
∈	Indicates membership	ALT-0206	Symbol
∉	Indicates nonmembership	ALT-0207	Symbol
±	Plus or minus (a tolerance)	ALT-0177	Symbol
°	Degrees (as in degrees Celsius)	ALT-0176	Symbol
∑	Summation	ALT-0229	Symbol
—	Big dash (Em dash)	Ctrl-q Shft-q	Times
–	Little dash (En dash)	Ctrl-q Shft-p	Times
†	Dagger	ALT-0134	Times
‡	Double dagger	ALT-0135	Times

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Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment: Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

[These changes are part of IEEE Std 802.3-2002.]

EDITORIAL NOTE—This amendment is based on the current edition of IEEE Std 802.3-2002 plus changes incorporated by IEEE Std 802.3ae-2002. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of IEEE Std 802.3ae-2002.

Editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions. ***Replace*** is used to make large changes in existing text, subclauses, tables, or figures by removing existing material and replacing it with new material. Editorial notes will not be carried over into future editions because the changes will be incorporated into the base standard.

1. Introduction

1.4 Definitions

Replace 1.4.170 with the following:

1.4.170 Medium Dependent Interface (MDI): The mechanical and electrical or optical interface between the transmission medium and the MAU (e.g., 10BASE-T) or the PHY (e.g., 1000BASE-T) and also between the transmission medium and any associated (optional per IEEE 802.3 Clause 33) Powered Device (PD) or Endpoint Power Sourcing Equipment (PSE).

Insert the following definitions alphabetically into 1.4. Renumber the definitions as required.

1.4.x Endpoint PSE: Power Sourcing Equipment (PSE) that is located at an endpoint.

1.4.x Link Section: The portion of the link from the PSE to the PD.

1.4.x Midspan: An entity located within a link segment that is distinctly separate from and between the Medium Dependent Interfaces (MDIs).

1.4.x Midspan PSE: Power Sourcing Equipment (PSE) that is located in the Midspan.

1.4.x PSE Group: A PSE or a collection of PSEs that can be related to the logical arrangement for management within an encompassing system.

1.4.x Power Interface (PI): The mechanical and electrical interface between the Power Sourcing Equipment (PSE) or Powered Device (PD) and the transmission medium. In an Endpoint PSE and in a PD the Power Interface is the MDI.

1.4.x Twisted Pair Medium Dependent Interface (TP MDI): The mechanical and electrical interface between the transmission medium and the Medium Attachment Unit (MAU) or PHY, e.g., (10BASE-T, 100BASE-TX, or 1000BASE-T).

1.4.x Power Sourcing Equipment (PSE): A DTE or midspan device that provides the power to a single link section. DTE powering is intended to provide a single 10BASE-T, 100BASE-TX, or 1000BASE-T device with a unified interface for both the data it requires and the power to process these data.

1.4.x Powered Device (PD): A device that is either drawing power or requesting power from a PSE.

1.5 Abbreviations

Insert the following items alphabetically in 1.5.

MPS	Maintain Power Signature
PD	Powered Device
PI	Power Interface
PSE	Power Sourcing Equipment
SELV	Safety Extra Low Voltage

14. Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T

14.3.1.1 Isolation requirement

Change the first paragraph of this subclause as follows:

A MAU that encompasses the PI of a PD within its MDI (see 33.1.3) shall provide isolation between all external conductors, including frame ground, and all MDI leads including those not used by 10BASE-T. A MAU that does not encompass the PI of a PD within its MDI~~the MAU~~ shall provide isolation between the DTE Physical Layer circuits including frame ground and all MDI leads including those not used by 10BASE-T. This electrical separation shall withstand at least one of the following electrical strength tests.

14.10.4.5.11 Isolation requirements

Replace item 1 of the table in this subclause with the following:

1a	Isolation, MDI leads to DTE Physical Layer circuits	14.3.1.1	C		Any of the three tests listed in 14.3.1.1. Function provided by MAUs that do not encompass the PI of a PD within their MDI.
1b	Isolation, MDI leads to all external conductors	14.3.1.1	C		Any of the three tests listed in 14.3.1.1. Function provided by MAUs that encompass the PI of a PD within their MDI.

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.2.4 Management functions

Change the third paragraph of this subclause as follows:

The MII basic register set consists of two registers referred to as the Control register (Register 0) and the Status register (Register 1). All PHYs that provide an MII shall incorporate the basic register set. All PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15). The status and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through ~~10~~12 are part of the extended register set. The format of Registers 4 through 10 are defined for the specific Auto-Negotiation protocol used (Clause 28 or Clause 37). The format of these registers is selected by the bit settings of Registers 1 and 15.

Change Table 22–6 as follows:

Table 22–6—MII management register set

Register address	Register name	Basic/Extended	
		MII	GMII
0	Control	B	B
1	Status	B	B
2,3	PHY Identifier	E	E
4	Auto-Negotiation Advertisement	E	E
5	Auto-Negotiation Link Partner Base Page Ability	E	E
6	Auto-Negotiation Expansion	E	E
7	Auto-Negotiation Next Page Transmit	E	E
8	Auto-Negotiation Link Partner Received Next Page	E	E
9	MASTER-SLAVE Control Register	E	E
10	MASTER-SLAVE Status Register	E	E
11	PSE Control register	E	E
12	PSE Status register	E	E
~~11~~13~~, through~~ 14	Reserved	E	E
15	Extended Status	Reserved	B
16 through 31	Vendor Specific	E	E

22.2.4.3 Extended capability registers

Change the first paragraph of this subclause as follows:

In addition to the basic register set defined in 22.2.4.1 and 22.2.4.2, PHYs may provide an extended set of capabilities that may be accessed and controlled via the MII management interface. Eleven~~Nine~~ registers have been defined within the extended address space for the purpose of providing a PHY-specific identifier to layer management, ~~and~~ to provide control and monitoring for the Auto-Negotiation process, and to provide control and monitoring of power sourcing equipment.

Add the following two new subclauses after subclause 22.2.4.3.8 and renumber current subclause 22.2.4.3.9 as 22.2.4.3.11.

22.2.4.3.9 PSE Control register (Register 11)

Register 11 provides control bits that are used by a PSE. See 33.6.1.1.

22.2.4.3.10 PSE Status register (Register 12)

Register 12 provides status bits that are supplied by a PSE. See 33.6.1.2.

30. 10 Mb/s, 100 Mb/s, 1000 Mb/s and 10 Gb/s Management

30.1 Overview

Change the first paragraph of this subclause as follows:

This clause provides the Layer Management specification for DTEs, repeaters, ~~and~~ MAUs, and Midspans based on the CSMA/CD access method. The clause is produced from the ISO framework additions to Clause 5, Layer Management; Clause 19, Repeater Management; and Clause 20, MAU Management. It incorporates additions to the objects, attributes, and behaviors to support 100 Mb/s, 1000 Mb/s and 10 Gb/s, full duplex operation, MAC Control, ~~and~~ Link Aggregation and DTE Power via MDI.

30.1.1 Scope

Change the first paragraph of this subclause as follows:

This clause includes selections from Clauses 5, 19, and 20. It is intended to be an entirely equivalent specification for the management of 10 Mb/s DTEs, 10 Mb/s baseband repeater units, and 10 Mb/s integrated MAUs. It also includes the additions for management of MAC Control, DTEs and repeaters at speeds greater than 10 Mb/s, embedded MAUs, ~~and~~ PHYs and DTE Power via MDI. Implementations of management for DTEs, repeater units, and embedded MAUs should follow the requirements of this clause (e.g., a 10 Mb/s implementation should incorporate the attributes to indicate that it is not capable of 100 or 1000 Mb/s operation~~,~~; half duplex DTE should incorporate the attributes to indicate that it is not capable of full duplex operation, etc.).

30.1.2 Relationship to objects in IEEE 802.1F

Change the second paragraph of this subclause as follows:

oResourceTypeID

This object class is mandatory and shall be implemented as defined in IEEE 802.1F. This object is bound to oMAC-Entity, oRepeater, oMidSpan and oMAU as defined by the NAME BINDINGs in ~~30A.8.1~~30A.10.1. Note that the binding to oMAU is mandatory only when MII is present. The Entity Relationship Diagrams, Figures 30–3 and 30–4, shows these bindings pictorially.

30.1.4 Management model

Change the second last paragraph of this subclause as follows:

The above items are defined in 30.3~~, 30.4, 30.5, 30.6, 30.7 and 30.8~~ through 30.10 of this clause in terms of the template requirements of ISO/IEC 10165-4: 1991.

30.2.2.1 Text description of managed objects

Insert the following text immediately after the description of oWIS:

oMidSpan

The top-most managed object class of the Midspan containment tree shown in Figure 30–4. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oPSEGroup

The PSE Group managed object class is a view of a collection of PSEs.

oPSE

The managed object of that portion of the containment trees shown in Figure 30–3 and Figure 30–4. The attributes and actions defined in this subclause are contained within the oPSE managed object.

30.2.3 Containment

Change the first paragraph of this subclause as follows:

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in the entity relationship diagrams, Figure 30–3 and Figure 30–4. ~~This~~ These figures ~~shows~~ the names of the object classes and whether a particular containment relationship is one-to-one or one-to-many. For further requirements on this topic, see IEEE Std 802.1F-1993. PSE management is only valid in a system that provides management at the next higher containment level, that is, either a DTE, repeater or Midspan with management.

Replace the existing Figure 30–3 with the following new figure:

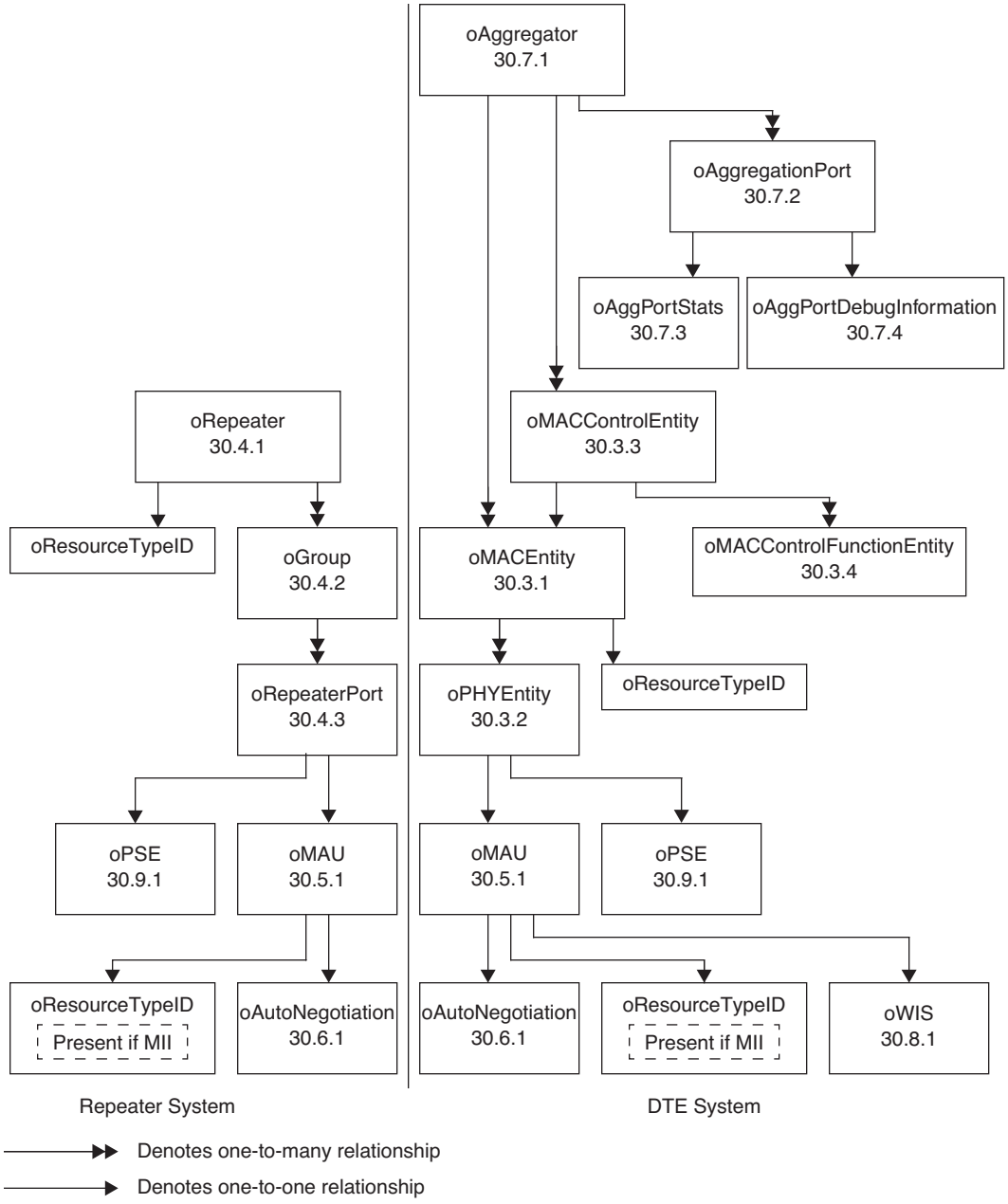


Figure 30–3—Repeater and DTE System Eentity relationship diagram

Insert new Figure 30–4 as follows:

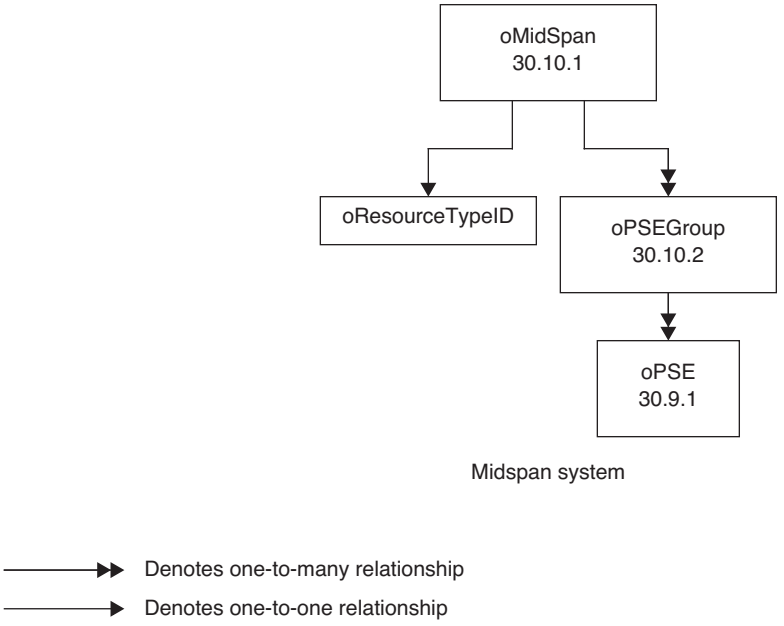


Figure 30–4—Midspan entity relationship diagram

30.2.5 Capabilities

Change the first paragraph of this subclause as follows:

This standard makes use of the concept of *packages* as defined in ISO/IEC 10165-4: 1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory, or be conditional, that is to say, present if a given condition is true. Within this standard *capabilities* are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. Implementation of the appropriate basic and mandatory packages is the minimum requirement for claiming conformance to IEEE 802.3 Management. Implementation of an entire optional capability is required in order to claim conformance to that capability. The capabilities and packages for IEEE 802.3 Management are specified in Tables 30–1~~, 30–2 and 30–3~~ through 30–4.

Insert the following paragraphs at the end of this subclause:

For managed PSEs, the PSE Basic Package is mandatory and the PSE Recommended Package is optional. For a managed PSE to be conformant to this standard, it shall fully implement the PSE Basic Package. For a managed PSE to be conformant to the optional Recommended Package it shall implement that entire package. PSE management is optional with respect to all other CSMA/CD management.

For managed Midspans, the Midspan managed object class shall be implemented in its entirety. All attributes and notifications are mandatory. Midspan management is optional with respect to all other CSMA/CD management.

Insert the following new table after Table 30–3:

Table 30–4—PSE Capabilities

			PSE Basic Package (Mandatory)	PSE Recommended Package (Optional)	Midspan Basic Capability (Mandatory)
oResourceTypeID managed object					
aResourceTypeIDName	ATTRIBUTE	GET			X
aResourceInfo	ATTRIBUTE	GET			X
oMidSpan managed object class (30.10.1)					
aMidSpanID	ATTRIBUTE	GET			X
aMidSpanPSEGroupCapacity	ATTRIBUTE	GET			X
aMidSpanPSEGroupMap	ATTRIBUTE	GET			X
nMidSpanPSEGroupMapChange	NOTIFICATION				X
oPSEGroup managed object class (30.10.2)					
aPSEGroupID	ATTRIBUTE	GET			X
aPSECapacity	ATTRIBUTE	GET			X
aPSEMap	ATTRIBUTE	GET			X
nPSEMapChange	NOTIFICATION				X
oPSE managed object class (30.9.1)					
aPSEID	ATTRIBUTE	GET	X		
aPSEAdminState	ATTRIBUTE	GET	X		
aPSEPowerPairsControlAbility	ATTRIBUTE	GET	X		
aPSEPowerPairs	ATTRIBUTE	GET-SET	X		
aPSEPowerDetectionStatus	ATTRIBUTE	GET	X		
aPSEPowerClassification	ATTRIBUTE	GET		X	
aPSEInvalidSignatureCounter	ATTRIBUTE	GET		X	
aPSEPowerDeniedCounter	ATTRIBUTE	GET		X	
aPSEOverLoadCounter	ATTRIBUTE	GET		X	
aPSEShortCounter	ATTRIBUTE	GET		X	
aPSEMPSAbsentCounter	ATTRIBUTE	GET		X	
acPSEAdminControl	ACTION		X		
Common Attributes Template					
aCMCounter	ATTRIBUTE	GET		X	

Insert the following subclause after subclause 30.8

30.9 Management for Power Sourcing Equipment (PSE)

30.9.1 PSE managed object class

This subclause formally defines the behaviours for the oPSE managed object class attributes and actions.

30.9.1.1 PSE attributes

30.9.1.1.1 aPSEID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPSEID is assigned so as to uniquely identify a PSE among the subordinate managed objects of the containing object.;

30.9.1.1.2 aPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

enabled	PSE functions enabled
disabled	PSE functions disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the PSE functions. An interface which can provide the PSE functions specified in Clause 33 will be enabled to do so when this attribute has the enumeration “enabled.” When this attribute has the enumeration “disabled” the interface will act as it would if it had no PSE function. The operational state of the PSE function can be changed using the acPSEAdminControl action. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Enable bit specified in 33.6.1.1.3.;

30.9.1.1.3 aPSEPowerPairsControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
Indicates the ability to control which PSE Pinout Alternative (see 33.2.2) is used for PD detection and power. When “true” the PSE Pinout Alternative used can be controlled through the aPSEPowerPairs attribute. When “false” the PSE Pinout Alternative used cannot be controlled through the aPSEPowerPairs attribute. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control Ability bit specified in 33.6.1.2.10;

30.9.1.1.4 aPSEPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

signal	PSE Pinout Alternative A
spare	PSE Pinout Alternative B

BEHAVIOUR DEFINED AS:

A read-write value that identifies the supported PSE Pinout Alternative specified in 33.2.2. A GET operation returns the PSE Pinout Alternative in use. A SET operation changes the PSE Pinout Alternative used to the indicated value only if the attribute aPSEPowerPairsControlAbility is "true." If the attribute aPSEPowerPairsControlAbility is "false" a SET operation has no effect.

The enumeration "signal" indicates that PSE Pinout Alternative A is used for PD detection and power. The enumeration "spare" indicates that PSE Pinout Alternative B is used for PD detection and power. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control bits specified in 33.6.1.1.2.;

30.9.1.1.5 aPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	PSE disabled
searching	PSE searching
deliveringPower	PSE delivering power
test	PSE test mode
fault	PSE fault detected
otherFault	PSE implementation specific fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 33.2.6.

The enumeration "disabled" indicates that the PSE State diagram (Figure 33–6) is in the state DISABLED. The enumeration "deliveringPower" indicates that the PSE State diagram is in the state POWER_ON. The enumeration "test" indicates that the PSE State diagram is in the state TEST_MODE. The enumeration "fault" indicates that the PSE State diagram is in the state TEST_ERROR. The enumeration "otherFault" indicates that the PSE State diagram is in the state IDLE due to the variable error_condition = true. The enumeration "searching" indicates the PSE State diagram is in a state other than those listed above. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Status bits specified in 33.6.1.2.9.

NOTE—A derivative attribute may wish to apply a delay to the use of the "deliveringPower" enumeration as the PSE state diagram will enter then quickly exit the POWER_ON state if a short-circuit or overcurrent condition is present when power is first applied.;

30.9.1.1.6 aPSEPowerClassification

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

class0	Class 0 PD
class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected PD as specified in 33.2.7.2.

This value is only valid while a PD is being powered, that is the attribute aPSEPowerDetectionStatus reporting the enumeration “deliveringPower.” If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PD Class bits specified in 33.6.1.2.8.;

30.9.1.1.7 aPSEInvalidSignatureCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–6) enters the state SIGNATURE_INVALID. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Invalid Signature bit specified in 33.6.1.2.4.;

30.9.1.1.8 aPSEPowerDeniedCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–6) enters the state POWER_DENIED. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Denied bit specified in 33.6.1.2.2.;

30.9.1.1.9 aPSEOverLoadCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–6) enters the state ERROR_DELAY_OVER. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Overload bit specified in 33.6.1.2.6.;

30.9.1.1.10 aPSEShortCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–6) enters the state ERROR_DELAY_SHORT. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Short Circuit bit specified in 33.6.1.2.5.;

30.9.1.1.11 aPSEMPSAbsentCounter

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 33–6) transitions directly from the state POWER_ON to the state IDLE due to tmpdo_timer_done being asserted. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the MPS Absent bit specified in 33.6.1.2.7.;

30.9.1.2 PSE actions

30.9.1.2.1 acPSEAdminControl

ACTION

APPROPRIATE SYNTAX:
Same as aPSEAdminState

BEHAVIOUR DEFINED AS:
This action provides a means to alter aPSEAdminState.;

30.10 Layer management for Midspan

30.10.1 Midspan managed object class

This subclause formally defines the behaviours for the oMidSpan managed object class, attributes, and notifications.

30.10.1.1 Midspan attributes

30.10.1.1.1 aMidSpanID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMidSpanID is assigned so as to uniquely identify a Midspan device among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2: 1992 [SMI]).;

30.10.1.1.2 aMidSpanPSEGroupCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aMidSpanPSEGroupCapacity is the number of PSE groups that can be contained within the Midspan device. Within each managed Midspan device, the PSE groups are uniquely numbered in the range from 1 to aMidSpanPSEGroupCapacity.

Some PSE groups may not be present in a given Midspan instance, in which case the actual number

of PSE groups present is less than aMidSpanPSEGroupCapacity. The number of PSE groups present is never greater than aMidSpanPSEGroupCapacity.;

30.10.1.1.3 aMidSpanPSEGroupMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of PSE groups that are viewed by PSE group managed objects. The length of the bitstring is “aMidSpanPSEGroupCapacity” bits. The first bit relates to PSE group 1. A “1” in the bitstring indicates presence of the PSE group, “0” represents absence of the PSE group.;

30.10.1.2 Midspan notifications

30.10.1.2.1 nMidSpanPSEGroupMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the PSE group structure of a Midspan device. This occurs only when a PSE group is logically removed from or added to a Midspan device. The nMidSpanPSEGroupMapChange notification is not sent when powering up a Midspan device. The value of the notification is the updated value of the aMidSpanPSEGroupMap attribute.;

30.10.2 PSE Group managed object class

This subclause formally defines the behaviours for the oPSEGroup managed object class, attributes, actions, and notifications.

30.10.2.1 PSE Group attributes

30.10.2.1.1 aPSEGroupID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A value unique within the Midspan device. The value of aPSEGroupID is assigned so as to uniquely identify a PSE group among the subordinate managed objects of the containing object (oMidSpan). This value is never greater than aMidSpanPSEGroupCapacity.;

30.10.2.1.2 aPSECapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aPSECapacity is the number of PSEs contained within the PSE group. Valid range is 1–1024.

Within each PSE group, the PSEs are uniquely numbered in the range from 1 to aPSECapacity. Some PSEs may not be present in a given PSE group instance, in which case the actual number of PSEs present is less than aPSECapacity. The number of PSEs present is never greater than aPSECapacity.;

30.10.2.1.3 aPSEMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
A string of bits that reflects the current configuration of PSE managed objects within this PSE group. The length of the bitstring is “aPSECapacity” bits. The first bit relates to PSE 1. A “1” in the bitstring indicates presence of the PSE, “0” represents absence of the PSE.;

30.10.2.2 PSE Group notifications

30.10.2.2.1 nPSEMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the PSE structure of a PSE group. This occurs only when a PSE is logically removed from or added to a PSE group. The nPSEMapChange notification is not sent when powering up a Midspan device. The value of the notification is the updated value of the aPSEMap attribute.;

40. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 1000BASE-T

40.6.1.1 Isolation requirement

Change the first paragraph of this subclause as follows:

A PHY that encompasses the PI of a PD within its MDI (see 33.1.3) shall provide isolation between all external conductors, including frame ground (if any), and all MDI leads. A PHY that does not encompass the PI of a PD within its MDI~~The PHY~~ shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

40.12.2 Major capabilities/options

Insert the following row at the bottom (following item AXO) of the table:

*PD	Powered Device	40.6.1.1	O	Yes [ ] No [ ]	PHY encompasses the PI of a PD within its MDI.

40.12.7 PMA Electrical Specifications

Change the second row (item PME15) of the table in this subclause as follows:

PME15a	The PHY shall provide electrical isolation between	40.6.1.1	!PD:M	Yes [ ] N/A [ ]	The port device circuits including frame ground, and all MDI leads.

Insert a row between the second and third rows (between items PME15 and PME16) of the table in this subclause as follows:

PME15b	The PHY shall provide electrical isolation between	40.6.1.1	PD:M	Yes [ ] N/A [ ]	All external conductors, including frame ground, and all MDI leads.

Annex 30A

(normative)

GDMO specification for IEEE 802.3 managed object classes

Change the first paragraph of this annex as follows:

This annex formally defines the protocol encodings for CMIP and ISO/IEC 15802-2: 1995 [ANSI/IEEE Std 802.1B and 802.1k, 1995 Edition] for the IEEE 802.3 Managed Objects using the templates specified in ISO/IEC 10165-4: 1992. The application of a GDMO template compiler against 30A.1 to ~~30A.15~~30A.18 will produce the proper protocol encodings.

30A.10.1 ResourceTypeID, formal definition

Insert the following paragraph at the end of this subclauses:

nbResourceTypeID-midSpan **NAME BINDING**

SUBORDINATE OBJECT CLASS "IEEE802.1F":oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS oMidSpan AND SUBCLASSES;
WITH ATTRIBUTE aMidSpanID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) resourceTypeID-midSpan(25)};

Insert the following subclauses after subclause 30A.15.2:

30A.16 PSE managed object class

30A.16.1 PSE, formal definition

oPSE **MANAGED OBJECT CLASS**

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;

CHARACTERIZED BY
pPSEBasic PACKAGE
ATTRIBUTES aPSEID GET,
aPSEAdminState GET,
aPSEPowerPairsControlAbility GET,
aPSEPowerPairs GET-REPLACE,
aPSEPowerDetectionStatus GET;
ACTIONS acPSEAdminControl;
;
;
CONDITIONAL PACKAGES
pPSERecommended PACKAGE
ATTRIBUTES aPSEPowerClassification GET,
aPSEInvalidSignatureCounter GET,
aPSEPowerDeniedCounter GET,

aPSEOverLoadCounter GET,
aPSEShortCounter GET,
aPSEMPSAbsentCounter GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pseRecommendedPkg(27)};
PRESENT IF The recommended package is implemented;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) pseObjectClass(15)};

nbPSE-repeaterPortName NAME BINDING

SUBORDINATE OBJECT CLASS oPSE;
NAMED BY SUPERIOR OBJECT CLASS oRepeaterPorts AND SUBCLASSES;
WITH ATTRIBUTE aPSEID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) pse-repeaterPortName(26)};

nbPSE-dteName NAME BINDING

SUBORDINATE OBJECT CLASS oPSE;
NAMED BY SUPERIOR OBJECT CLASS oPHYEntity AND SUBCLASSES;
WITH ATTRIBUTE aPSEID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) pse-dteName(27)};

nbPSE-pseGroupName NAME BINDING

SUBORDINATE OBJECT CLASS oPSE;
NAMED BY SUPERIOR OBJECT CLASS oPSEGroup AND SUBCLASSES;
WITH ATTRIBUTE aPSEID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) pse-pseGroupName(28)};

30A.16.2 PSE attributes

aPSEID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseID(209)};

bPSEID BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.1;

aPSEAdminState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
MATCHES FOR EQUALITY;

BEHAVIOUR bPSEAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseAdminState(210)};

bPSEAdminState BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.2;

aPSEPowerPairsControlAbility ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PairCtrlAbility;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerPairsControlAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerPairsControlAbility(211)};

bPSEPowerPairsControlAbility BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.3;

aPSEPowerPairs ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PSEPowerPairs;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerPairs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerPairs(212)};

bPSEPowerPairs BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.4;

aPSEPowerDetectionStatus ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DetectStatus;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerDetectionStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerDetectionStatus(214)};

bPSEPowerDetectionStatus BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.5;

aPSEPowerClassification ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PowerClass;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerClassification;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerClassification(215)};

bPSEPowerClassification **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.6;

aPSEInvalidSignatureCounter **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEInvalidSignatureCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7)pseInvalidSignatureCounter(227)};

bPSEInvalidSignatureCounter **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.7;

aPSEPowerDeniedCounter **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerDeniedCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7)psePowerDeniedCounter(228)};

bPSEPowerDeniedCounter **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.8;

aPSEOverLoadCounter **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEOverLoadCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7)pseOverLoadCounter(229)};

bPSEOverLoadCounter **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.9;

aPSEShortCounter **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEShortCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7)pseShortCounter(230)};

bPSEShortCounter **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.10;

aPSEMPSAbsentCounter **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEMPSAbsentCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseMPSAbsentCounter(217)};

bPSEMPSAbsentCounter **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.11;

30A.16.3 PSE actions

acPSEAdminControl **ACTION**

BEHAVIOUR bPSEAdminControl;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) pseAdminControl(13)};

bPSEAdminControl **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.2.1;

30A.17 Midspan managed object class

oMidSpan **MANAGED OBJECT CLASS**

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
pMidSpanBasic PACKAGE
ATTRIBUTES aMidSpanID GET,
aMidSpanPSEGroupCapacity GET,
aMidSpanPSEGroupMap GET;
NOTIFICATIONS nMidSpanPSEGroupMapChange;
;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) midSpanObjectClass(17)};

nbMidSpanName **NAME BINDING**

SUBORDINATE OBJECT CLASS oMidSpan;
NAMED BY SUPERIOR OBJECT CLASS “ISO/IEC 10165-2 ”:system AND SUBCLASSES;
WITH ATTRIBUTE aMidSpanID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) midSpanName(31)};

nbMidSpanMonitor **NAME BINDING**

SUBORDINATE OBJECT CLASS "IEEE802.1F ":oEWMAMetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2 ":system AND SUBCLASSES;
WITH ATTRIBUTE "IEEE802.1F":aScannerId;
CREATE WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) midSpanMonitor(32)};

30A.17.1 Midspan attributes

aMidSpanID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bMidSpanID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) midSpanID(221)};

bMidSpanID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.10.1.1.1;

aMidSpanPSEGroupCapacity **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY,ORDERING;
BEHAVIOUR bMidSpanPSEGroupCapacity;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) midSpanPSEGroupCapacity(222)};

bMidSpanPSEGroupCapacity **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.10.1.1.2;

aMidSpanPSEGroupMap **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
MATCHES FOR EQUALITY;
BEHAVIOUR bMidSpanPSEGroupMap;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) midSpanPSEGroupMap(223)};

bMidSpanPSEGroupMap **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.10.1.1.3;

30A.17.2 Midspan notifications

nMidSpanPSEGroupMapChange **NOTIFICATION**

BEHAVIOUR bMidSpanPSEGroupMapChange;

WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10)midSpanPSEGroupMapChange(8)};

bMidSpanPSEGroupMapChange **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.1.2.1;

30A.18 PSE Group managed object class

oPSEGroup **MANAGED OBJECT CLASS**

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
pPSEGroupBasic PACKAGE
ATTRIBUTES aPSEGroupID GET,
aPSECapacity GET,
aPSEMap GET;
NOTIFICATIONS nPSEMapChange;
;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) midSpanGroupObjectClass(18)};

nbPSEGroupName **NAME BINDING**

SUBORDINATE OBJECT CLASS oPSEGroup;
NAMED BY SUPERIOR OBJECT CLASS oMidSpan AND SUBCLASSES;
WITH ATTRIBUTE aPSEGroupID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) pseGroupName(33)};

30A.18.1 PSE Group attributes

aPSEGroupID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEGroupID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseGroupID(224)};

bPSEGroupID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.2.1.1;

aPSECapacity **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY,ORDERING;
BEHAVIOUR bPSECapacity;

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseCapacity(225)};

bPSECapacity **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.2.1.2;

aPSEMap **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEMap;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseMap(226)};

bPSEMap **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.2.1.3;

30A.18.2 PSE Group notifications

nPSEMapChange **NOTIFICATION**

BEHAVIOUR bPSEMapChange;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10)pseMapChange(9)};

bPSEMapChange **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.2.2.1;

Annex 30B

(normative)

GDMO and ASN.1 definitions for management

30B.2 ASN.1 module for CSMA/CD managed objects

Insert the following ASN.1 definitions into the ASN.1 module, in appropriate alphabetic sequence:

```
CurrentStatus ::= ENUMERATED {
      MPSAbsent               (0),     -- MPS absent
      ok                      (1)      -- MPS present and over current not detected
      }

DetectStatus ::= ENUMERATED {
      disabled                (0),     -- PSE disabled
      searching               (1),     -- PSE searching
      deliveringPower         (2),     -- PSE delivering power
      test                    (3),     -- PSE test mode
      fault                   (4),     -- PSE fault detected
      otherFault              (5)      -- PSE implementation specific fault detected
      }

PairCtrlAbility ::=BOOLEAN

PowerClass ::= ENUMERATED {
      class0                  (0),     -- Class 0 PD
      class1                  (1),     -- Class 1 PD
      class2                  (2),     -- Class 2 PD
      class3                  (3),     -- Class 3 PD
      class4                  (4)      -- Class 4 PD
      }

PSEPowerPairs ::= ENUMERATED {
      signal                  (0),     -- PSE Pinout Alternative A
      spare                   (1)      -- PSE Pinout Alternative B
      }
```

33. Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

NOTE—Although this clause existed in previous publications of IEEE Std 802.3, it was reserved for future use and therefore contained no information. All information in this clause is new material.

33.1 Overview

This clause defines the functional and electrical characteristics of two optional power (non-data) entities, a Powered Device (PD) and Power Sourcing Equipment (PSE), for use with the physical layers defined in Clauses 14, 25, and 40. These entities allow devices to supply/draw power using the same generic cabling as is used for data transmission.

DTE powering is intended to provide a 10BASE-T, 100BASE-TX, or 1000BASE-T device with a single interface to both the data it requires and the power to process these data. This clause specifies the following:

a) A power source to add power to the 100Ω balanced cabling system,
b) The characteristics of a powered device's load on the power source and the structured cabling,
c) A protocol allowing the detection of a device that requires power,
d) Optionally, a method to classify devices based on their power needs, and
e) A method for scaling supplied power back to the detect level when power is no longer requested or required.

The importance of item c) above should not be overlooked. Given the large number of legacy devices (both IEEE 802.3 and other types of devices) that could be connected to a 100Ω balanced cabling system, and the possible consequences of powering such devices, the protocol to distinguish compatible devices and non-compatible devices is important to prevent damage to non-compatible devices.

The detection and powering algorithms are likely to be compromised by cabling that is multi-point as opposed to point-to-point, resulting in unpredictable performance and possibly damaged equipment.

This clause differentiates between the two ends of the powered portion of the link, defining the PSE and the PD as separate but related devices.

33.1.1 Objectives

The following are the objectives of Power via MDI:

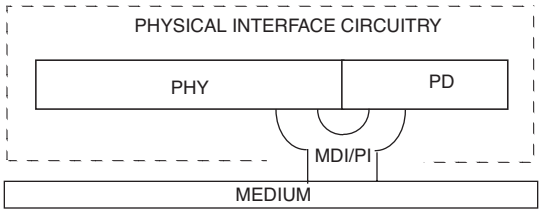
a) *Power*—A PD designed to the standard, and within its range of available power, can obtain both power and data for operation through the MDI and therefore need no additional connections.
b) *Safety*—A PSE designed to the standard will not introduce non-SELV (Safety Extra Low Voltage) power into the wiring plant.
c) *Compatibility*—Clause 33 utilizes the existing MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T without modification and adds no significant requirements to the cabling. The use of other IEEE 802.3 MDIs is beyond the scope of this clause.
d) *Simplicity*—The powering system described here is no more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, or 1000BASE-T.

33.1.2 Compatibility considerations

All implementations of PD and PSE systems shall be compatible at their respective Power Interfaces (PIs) when used in accordance with the restrictions of Clause 33 where appropriate. Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied.

33.1.3 Relationship of Power via MDI to the IEEE 802.3 Architecture

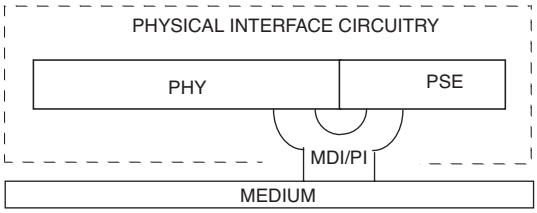
Power via MDI comprises an optional non-data entity. As a non-data entity it does not appear in a depiction of the OSI Reference Model. Figure 33–1 depicts the positioning of Power via MDI in the case of the PD.



MDI = MEDIUM DEPENDENT INTERFACE
PD = POWERED DEVICE
PHY = PHYSICAL LAYER DEVICE
PI = POWER INTERFACE

Figure 33–1—DTE Power via MDI powered device relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

Figure 33–2 and Figure 33–3 depict the positioning of Power via MDI in the cases of the Endpoint PSE and the Midspan PSE, respectively.



MDI = MEDIUM DEPENDENT INTERFACE
PHY = PHYSICAL LAYER DEVICE
PI = POWER INTERFACE
PSE = POWER SOURCING EQUIPMENT

Figure 33–2—DTE Power via MDI endpoint power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

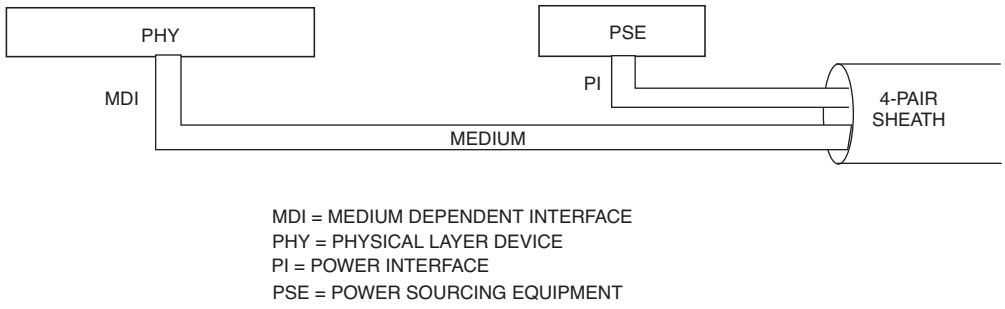


Figure 33–3—DTE Power via MDI midspan power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

Any device that contains an MDI compliant with Clause 14, Clause 25, and/or Clause 40, and sinks and/or sources power in accordance with the specifications of this clause is permitted.

The Power Interface (PI) is the generic term that refers to the mechanical and electrical interface between the PSE or PD and the transmission medium.

In an Endpoint PSE and in a PD the PI is encompassed within the MDI.

PSE power interface specifications that are defined at the MDI apply to an Endpoint PSE. They may or may not apply to a Midspan PI.

33.2 Power sourcing equipment

PSE, as the name implies, is the equipment that provides the power to a single link section. The PSE's main functions are to search the link section for a PD, optionally classify the PD, supply power to the link section (only if a PD is detected), monitor the power on the link section, and scale power back to the detect level when power is no longer requested or required. An unplugged link section is one instance when power is no longer required.

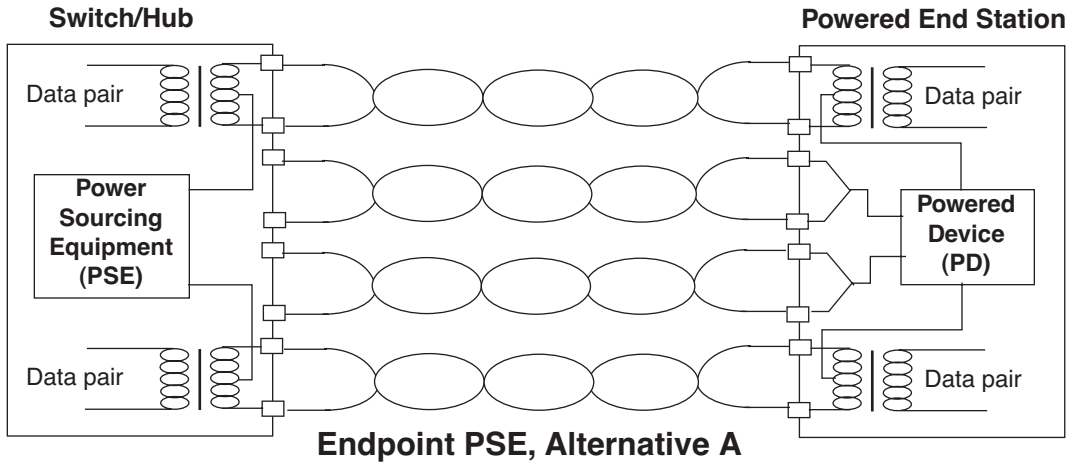
A PSE is electrically specified at the point of the physical connection to the cabling. Characteristics, such as the losses due to overvoltage protection circuits, or power supply inefficiencies, after the PI connector are not accounted for in this specification.

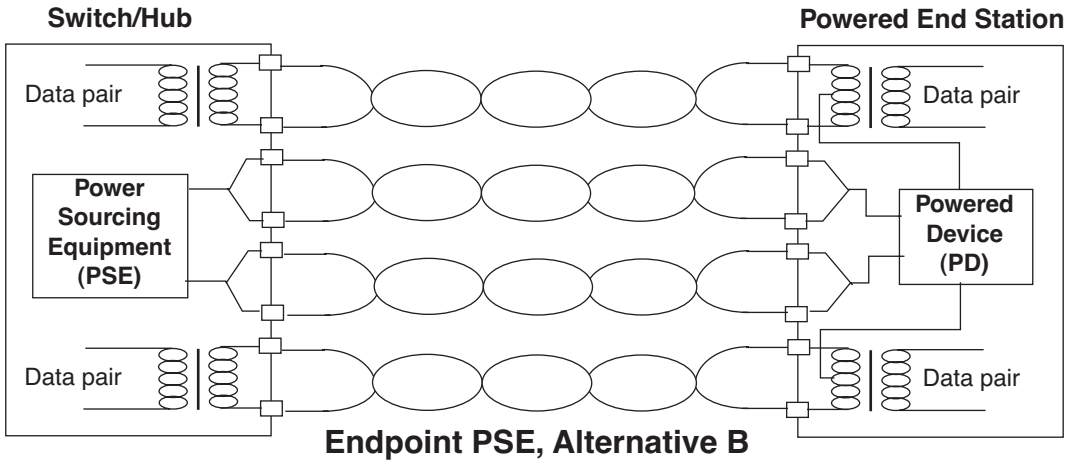
33.2.1 PSE location

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater or midspan. A PSE that is coincident with the DTE/Repeater is an "Endpoint PSE." A PSE that is located within a link segment that is distinctly separate from and between the MDIs is a "Midspan PSE." The requirements of this document shall apply equally to Endpoint and Midspan PSEs unless the requirement contains an explicit statement that it applies to only one implementation. See Figure 33–4.

Endpoint PSEs may support either Alternative A or B, or both. Endpoint PSEs can be compatible with 10BASE-T, 100BASE-TX and/or 1000BASE-T.

Midspan PSEs shall use Alternative B. Midspan PSEs are limited to operation with 10BASE-T and 100BASE-TX systems. Operation of Midspan PSEs on 1000BASE-T systems is beyond the scope of this standard.





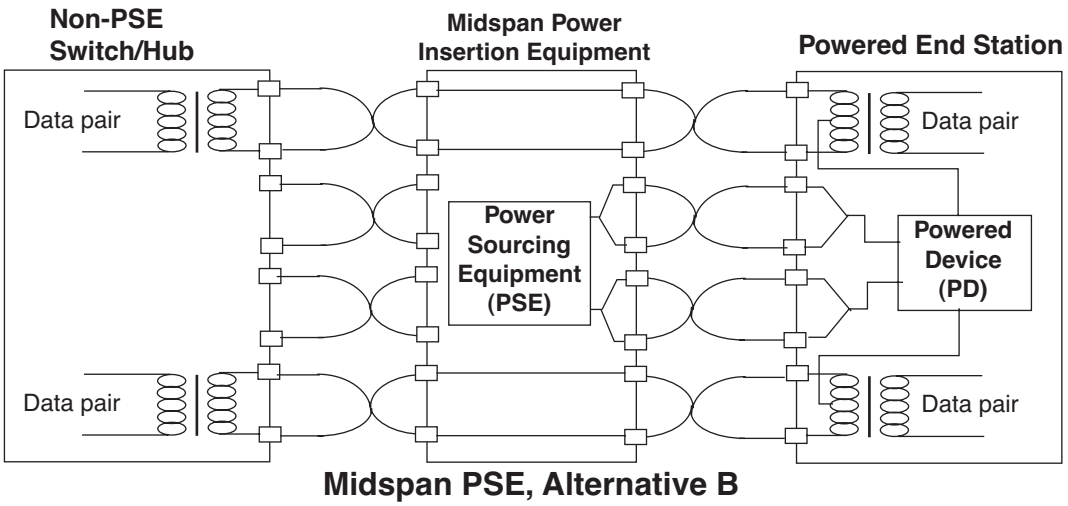


Figure 33–4—PSE location overview

33.2.2 PI pin assignments

A PSE device may provide power via one of two valid four-wire connections. In each four-wire connection, the two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 33–5, in conjunction with Table 33–1, illustrates the valid alternatives.

Table 33–1—PSE pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{Port}	Positive V_{Port}	
2	Negative V_{Port}	Positive V_{Port}	
3	Positive V_{Port}	Negative V_{Port}	
4			Positive V_{Port}
5			Positive V_{Port}
6	Positive V_{Port}	Negative V_{Port}	
7			Negative V_{Port}
8			Negative V_{Port}

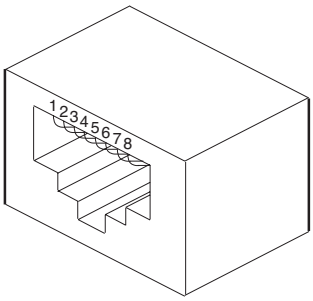


Figure 33–5—PD and PSE eight-pin modular jack

For the purposes of data transfer, the type of PSE data port is relevant to the far-end PD and in some cases to the cabling system between them. Therefore, Alternative A matches the positive voltage to the transmit pair of the PSE. PSEs that use automatically-configuring MDI/MDI-X ("Auto MDI-X") ports may choose either polarity choice associated with Alternative A configurations. For further information on the placement of MDI vs. MDI-X, see 14.5.2.

A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously.

33.2.3 PSE state diagrams

The PSE state diagrams specify the externally observable behavior of a PSE. Equivalent implementations that present the same external behavior are allowed.

The PSE shall provide the behavior of the state diagrams shown in Figure 33–6 and Figure 33–7.

33.2.3.1 Overview

Detection, classification, and power turn-on timing shall meet the specifications in Table 33–5.

The PSE shall turn on power after a valid detection in less than T_{pon} as specified in Table 33–5, if power is to be applied. If the PSE cannot supply power within T_{pon}, it shall initiate and successfully complete a new detection cycle before applying power.

It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 33.2.1), may be attached to the same link segment. In such a configuration, and without the required backoff algorithm, the PSEs could prevent each other from ever detecting a PD by interfering with the detection process of the other.

After a PSE that is performing detection using Alternative B fails to detect a valid PD detection signature, the PSE shall back off no less than T_{dbo} as specified in Table 33–5 before attempting another detection. During this backoff, the PSE shall not apply a voltage greater than 2.8Vdc to the PI. A PSE that is performing Alternative B detection shall not resume detection mode until at least one backoff cycle has elapsed.

If a PSE that is performing detection using Alternative B detects an open circuit (see 33.2.6.3) on the link section, then that PSE may optionally omit the detection backoff.

If a PSE performing detection using Alternative A detects an invalid signature, it should initiate a second detection attempt within 1 second after the beginning of the first detection attempt. This ensures that a PSE performing detection using Alternative A will complete a second detection cycle prior to a PSE using Alternative B that might also be present on the same Link Section, and therefore causing the invalid signature, completing its second detection cycle due to the Alternative B detection backoff described above.

33.2.3.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.2.3.3 Constants

The PSE state diagrams use the following constants:

I_{CUT}
: Overload current detection range (see Table 33–5)

I_{LIM}
: Output current at short circuit condition (see Table 33–5)

I_{Inrush}
: Current during inrush period of startup (see Table 33–5)

33.2.3.4 Variables

The PSE state diagrams use the following variables:

error_condition

A variable indicating the status of implementation-specific fault conditions that require the PSE not to source power. These error conditions are not the same conditions monitored by the state diagrams in Figure 33–7.

Values: FALSE: No fault indication.
TRUE: A fault indication exists.

mr_mps_valid

The PSE monitors either the DC or AC Maintain Power Signature (MPS, see 33.2.10.1). This variable indicates the presence or absence of a valid MPS.

Values: FALSE: If monitoring both components of the MPS, when the DC component of MPS is absent or the AC component of MPS is absent. If monitoring only one component of MPS, that component of MPS is absent.
TRUE: If monitoring both components of the MPS, the DC component of MPS and the AC component of MPS are both present. If monitoring only one component of MPS, that component of MPS is present.

mr_pse_alternative

This variable indicates which pinout alternative the PSE will use to apply power to the link (see Table 33–1). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.

Values: A: The PSE uses PSE pinout Alternative A.
B: The PSE uses PSE pinout Alternative B.

mr_pse_enable

A control variable that selects PSE operation and test functions. This variables is provided by a management interface that may be mapped to the PSE Control register PSE Enable bits (11.1:0), as described below, or other equivalent function.

Values: disable: All PSE functions disabled (behavior is as if there was no PSE functionality). This value corresponds to MDIO register bits 11.1:0 = '00'.
enable: Normal PSE operation. This value corresponds to MDIO register bits 11.1:0 = '01'.
force_power:Test mode selected that causes the PSE to apply power to the PI when there are no detected error conditions. This value corresponds to MDIO register bits 11.1:0 = '10'.

performs_classification

The performance of optional classification by the PSE is indicated by performs_classification.

Values: FALSE: The PSE does not perform classification.
TRUE: The PSE does perform classification.

pi_powered

A variable that controls the circuitry that the PSE uses to power the PD.

Values: FALSE: The PSE is not to apply power to the link (default).
TRUE: The PSE has detected a PD, optionally classified it, and determined the PD will be powered.

power_applied

A variable indicating that the PSE has begun steady state operation by having asserted pi_powered, completed the ramp of power per T_{Rise} of Table 33–5 and is operating beyond the startup requirements of 33.2.8.5.

Values: FALSE: The PSE is either not applying power or has begun applying power but is still in startup.
TRUE: The PSE has begun steady state operation.

pse_available_power

This variable indicates the highest power PD Class that could be supported. The value is determined in an implementation-specific manner.

Values: 0: Class 1
1: Class 2
2: Class 0, Class 3 and Class 4

power_not_available
: Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the PD Class of the attached PD.
  Values: FALSE: PSE is capable to continue to source power to a PD.
  TRUE: PSE is no longer capable of sourcing power to a PD.

pse_ready
: Variable that is asserted in an implementation-dependent manner to probe the link segment.
  Values: FALSE: PSE is not ready to probe the link segment.
  TRUE: PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid signature is detected due to the delay it will introduce between detection attempts (see 33.2.3.1).

pse_reset
: Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation specific reasons require reset of PSE functionality.
  Values: FALSE: Do not reset the PSE state diagram.
  TRUE: Reset the PSE state diagram.

33.2.3.5 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

tdbo_timer
: A timer used to regulate backoff upon detection of an invalid signature, see T_{dbo} in Table 33–5.

tdet_timer
: A timer used to limit an attempt to detect a PD, see T_{det} in Table 33–5.

ted_timer
: A timer used to regulate a subsequent attempt to detect a PD after an error condition causes power removal, see T_{ed} in Table 33–5.

tlim_timer
: A timer used to monitor the duration of a short-circuit condition, see T_{LIM} in Table 33–5.

tovld_timer
: A timer used to monitor the duration of an overcurrent condition, see T_{ovld} in Table 33–5.

tmpdo_timer
: A timer used to monitor the dropout of the MPS, see T_{MPDO} in Table 33–5.

tpon_timer
: A timer used to limit the time for power turn-on, see T_{pon} in Table 33–5.

tpdc_timer
: A timer used to limit the classification time, see T_{pdc} in Table 33–5.

33.2.3.6 Functions

do_detection
: This function returns multiple variables:
  The variable signature as defined in 33.2.6 and the variable mr_valid_siganture.
  signature: This variable indicates the presence or absence of a PD.
  Values: open_circuit: The PSE has detected an open circuit. This value is optionally returned by a PSE performing detection using Alternative B.
  valid: The PSE has detected a PD requesting power.
  invalid: Neither open_circuit, nor valid PD detection signature has been found.

mr_valid_signature: This variable indicates that the PSE has detected a valid signature.

Values: FALSE: No valid signature detected.
TRUE: Valid signature detected.

do_classification

This function returns multiple variables:

pd_requested_power: This variable indicates the power class requested by the PD.

Values: 0: Class 1
1: Class 2
2: Class 0, Class 3 or Class 4

mr_pd_class_detected: The class of the PD associated with the PD detection signature, see Table 33–3, 33.2.7. Class 0 is returned if an invalid classification signature is detected.

Values: Class_0
Class_1
Class_2
Class_3
Class_4

33.2.3.7 State diagrams

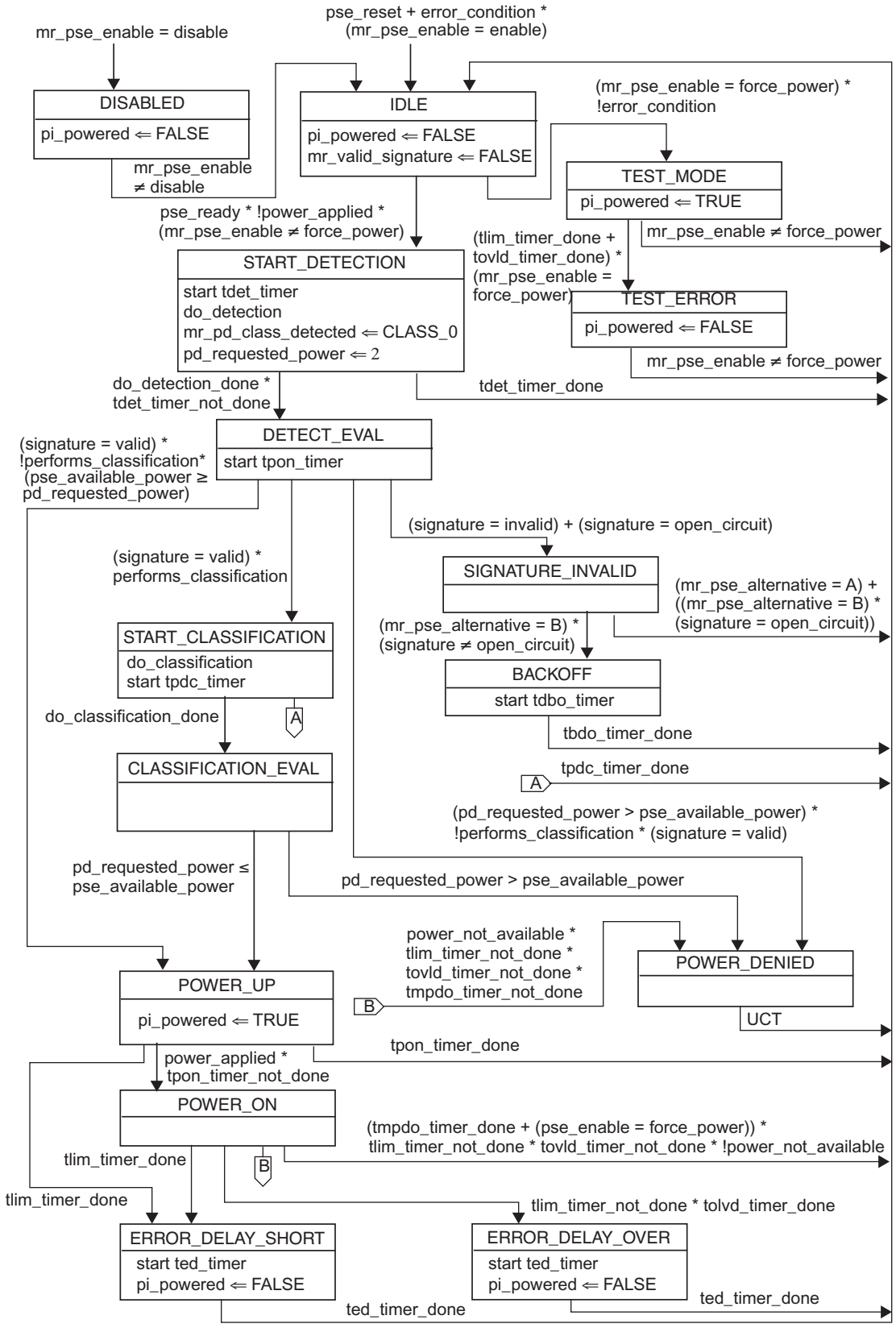


Figure 33–6—PSE state diagram

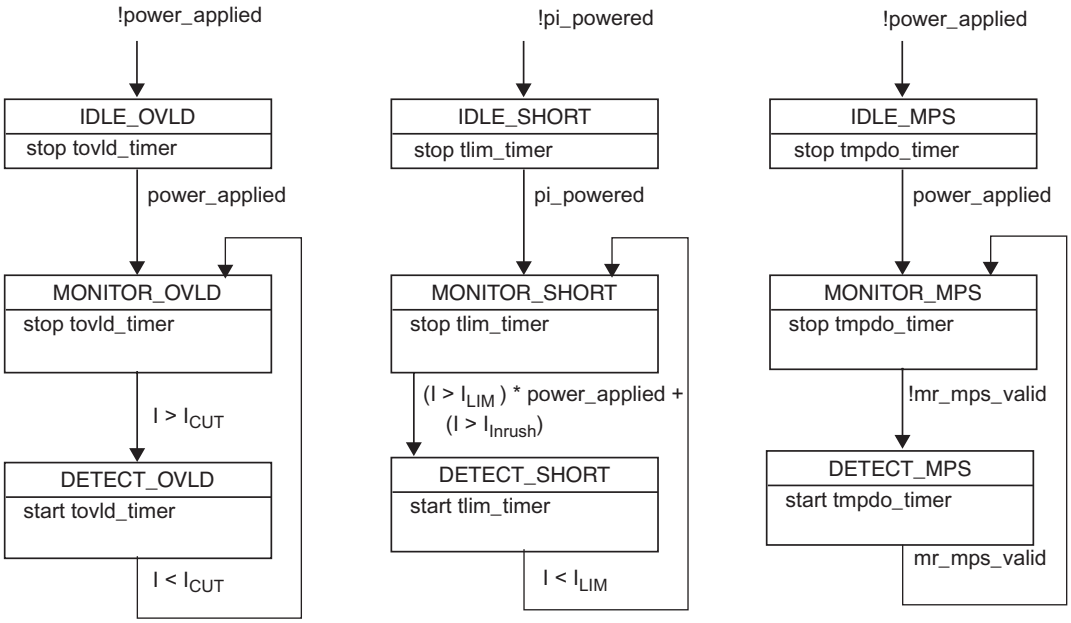


Figure 33–7—PSE monitor overload, monitor short, and monitor MPS state diagrams

33.2.4 PD detection

In an operational mode, the PSE shall not apply operating power to the PI until the PSE has successfully detected a PD requesting power.

The PSE is not required to continuously probe to detect a PD signature. The period of time when a PSE is not attempting to detect a PD signature is implementation dependent. Also, a PSE may successfully detect a PD, but may then opt not to power the detected PD.

PSE operation is independent of data link status.

The PSE shall turn on power only on the same pairs as those used for detection.

33.2.5 PSE validation circuit

The PSE shall detect the PD by probing via the PSE PI. The Thevenin equivalent of the detection circuit is shown in Figure 33–8. PSE requirements are stated for a Thevenin circuit only; they may be transformed via circuit theory into other circuit parameters in specific implementations.

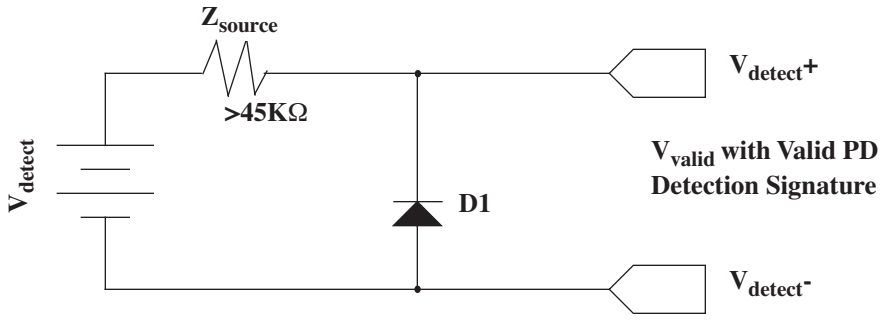


Figure 33–8—PSE detection source

A functional equivalent of the detection circuit that has no source impedance limitation, but restricts the PSE detection circuit to the first quadrant, is shown in Figure 33–9.

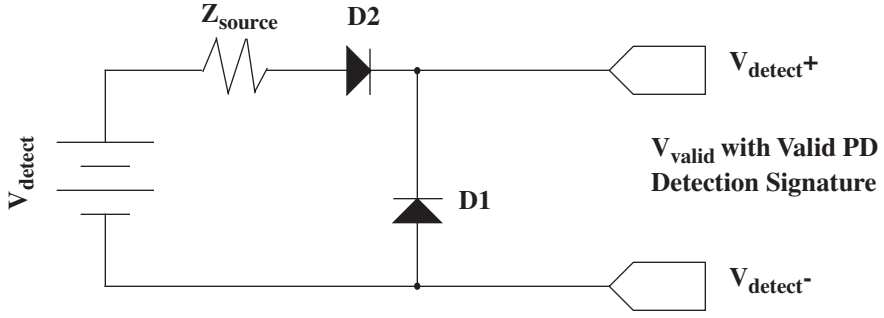


Figure 33–9—Alternative PSE detection source

In Figure 33–8 and Figure 33–9, the behavior of diode D1 ensures a non-valid PD detection signature for a reversed voltage PSE to PSE connection.

The open circuit voltage and short circuit current shall meet the specifications in Table 33–2. The PSE shall not be damaged by up to 5mA backdriven current over the range of V_{Port} as specified in Table 33–5. Output capacitance shall be as specified in Table 33–5. The PSE shall exhibit Thevenin equivalence to one of the detection circuits shown in Figure 33–8 or Figure 33–9 in all detection states.

Table 33–2—PSE PI detection mode electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	V_{oc}	V		30	In detection mode only
2	Short circuit current	I_{sc}	mA		5	In detection mode only
3	Valid test voltage	V_{valid}	V	2.8	10	

Table 33–2—PSE PI detection mode electrical requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Additional information
4	Voltage difference between test points	ΔV_{test}	V	1		
5	Time between any two test points	T_{BP}	ms	2		This timing implies a 500Hz maximum probing frequency.
6	Slew rate	V_{slew}	V/μs		0.1	
7	Accept signature resistance	R_{good}	KΩ	19	26.5	
8	Reject signature resistance	R_{bad}	KΩ	15	33	
9	Open circuit resistance	R_{open}	KΩ	500		
10	Accept signature capacitance	C_{good}	nF		150	
11	Reject signature capacitance	C_{bad}	μF	10		
12	Signature offset voltage tolerance	V_{os}	V	0	2.0	See Annex 33A for examples of valid signatures.
13	Signature offset current tolerance	I_{os}	μA	0	12	

33.2.5.1 Detection probe requirements

The detection voltage V_{detect} shall be within the V_{valid} voltage range at the PSE PI as specified in Table 33–2 with a valid PD detection signature connected. The PSE shall make at least two measurements with V_{detect} values that create at least a ΔV_{test} difference as specified in Table 33–2 between the two measurements with a valid PD detection signature connected.

NOTE—Settling time before voltage or current measurement: the voltage or current measurement should be taken after V_{detect} has settled to within 1% of its steady state condition.

The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be less than V_{slew} as specified in Table 33–2.

The polarity of V_{detect} shall match the polarity of V_{Port} as defined in 33.2.1.

33.2.6 PSE detection of PDs

The PSE probes the link section in order to detect a valid PD detection signature.

33.2.6.1 Detection criteria

A PSE shall accept as a valid signature a link section with both of the following characteristics between the powering pairs with an offset voltage up to V_{os} max and an offset current up to I_{os} max, as specified in Table 33–2:

a) Signature resistance R_{good}, and
b) Parallel signature capacitance C_{good}.

NOTE—Caution, in a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents.

33.2.6.2 Rejection criteria

The PSE shall reject link sections as having an invalid signature, when those link sections exhibit any of the following characteristics between the powering pairs, as specified in Table 33–2:

a) Resistance less than or equal to R_{bad} min, or
b) Resistance greater than or equal to R_{bad} max, or
c) Capacitance greater than or equal to C_{bad} min.

A PSE may accept or reject a signature resistance in the band between R_{good} min and R_{bad} min, and in the band between R_{good} max and R_{bad} max.

In instances where the resistance and capacitance meet the detection criteria, but one or both of the offset tolerances are exceeded, the detection behavior of the PSE is undefined.

33.2.6.3 Open circuit criteria

If a PSE that is performing detection using Alternative B (see 33.2.2) determines that the impedance at the PI is greater than R_{open} as defined in Table 33-2 item 9, then it may optionally consider the link to be open circuit and omit the tdbo_timer interval.

33.2.7 PSE classification of PDs

The PSE may optionally classify a PD to allow features such as load management to be implemented. If a PSE successfully completes detection of a PD, and the PSE does not classify the PD in Class 1, 2, 3, or 4, then the PSE shall assign the PD to Class 0.

A successful classification of a PD requires:

a) Successful PD detection, and subsequently,
b) Successful Class 0–4 classification.

A PSE may remove power to a PD that violates the maximum power required for its advertised class.

A PSE performs optional classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2. The PSE classification circuit should have adequate stability to prevent oscillation when connected to a PD.

33.2.7.1 Classification power levels

PDs provide information that allow a PSE to classify their power requirements. The classifications are listed in Table 33–3.

Class 4 is reserved for future use. PDs classified as Class 4 shall be treated as Class 0 for powering purposes.

33.2.7.2 PSE classification

The PSE shall provide V_{Class} between 15.5 and 20.5 volts, limited to 100 mA or less to the PI. Polarity shall be the same as defined for V_{Port} in 33.2.2 and timing specifications shall be as defined by T_{pdc} in Table 33–5. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–4. If the measured I_{Class} is equal to or greater than 51mA, the PSE shall classify the PD as Class 0.

Table 33–3—Power classifications

Class	Usage	Minimum power levels at output of PSE
0	Default	15.4 Watts
1	Optional	4.0 Watts
2	Optional	7.0 Watts
3	Optional	15.4 Watts
4	Reserved for future use	Treat as Class 0

NOTE— This is the minimum power at the PSE PI. For maximum power available to PDs, see Table 33–10.

Table 33–4—PD classification

Measured I_{Class}	Classification
0mA to 5mA	Class 0
> 5mA and < 8mA	May be Class 0 or 1
8mA to 13mA	Class 1
> 13mA and < 16mA	May be Class 0, 1, or 2
16mA to 21mA	Class 2
> 21mA and < 25mA	May be Class 0, 2, or 3
25mA to 31mA	Class 3
> 31mA and < 35mA	May be Class 0, 3, or 4
35mA to 45mA	Class 4
> 45mA and < 51mA	May be Class 0 or 4

33.2.8 Power supply output

When the PSE provides power to the PI, it shall conform with Table 33–5, Figure 33–6, and Figure 33–7.

Table 33–5—PSE output PI electrical requirements for all PD classes, unless otherwise specified

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Output voltage	V_{Port}	Vdc	44	57	See 33.2.8.1
2	Load regulation		V	44	57	See 33.2.8.2
3	Power feeding ripple and noise:					
	f < 500Hz		V_{pp}		0.5	See 33.2.8.3
	500Hz to 150kHz		V_{pp}		0.2	
	150KHz to 500KHz		V_{pp}		0.15	
	500KHz to 1MHz		V_{pp}		0.1	
4	Maximum output current in normal powering mode at PSE min output voltage	I_{Port_max}	mAdc	350		See 33.2.8.4
5	Output current in startup mode	I_{Inrush}	mA	400	450	See 33.2.8.5
6	a) IDLE state current 1	I_{Min1}	mA	0	5	Relevant for 33.2.10.1.2. PSE removes power for $t > T_{MPDO}$
	b) IDLE state current 2	I_{Min2}	mA	5	10	Relevant for 33.2.10.1.2. PSE may or may not remove power for $t > T_{MPDO}$
7a	PD Maintain Power Signature dropout time limit	T_{MPDO}	ms	300	400	See 33.2.10
7b	PD Maintain Power Signature time for validity	T_{MPS}	ms	60		See 33.2.10
8	Overload current detection range	I_{CUT}	mA	15400/ V_{Port}	400	See 33.2.8.6
9	Overload time limit	T_{ovld}	ms	50	75	See 33.2.8.7
10	Output current – at short circuit condition	I_{LIM}	mA	400	450	See 33.2.8.8
11	Short circuit time limit	T_{LIM}	ms	50	75	See 33.2.8.9
12	Turn on rise time	T_{Rise}	μs	15		From 10% to 90% of V_{Port}
13a	Turn off time	T_{Off}	ms		500	See 33.2.8.10
13b	Turn off voltage	V_{Off}	Vdc		2.8	See 33.2.8.11
14	Continuous Output Power	P_{Port}	W	15.4		Over the range of output voltage. Averaged over 1 second.

Table 33–5—PSE output PI electrical requirements for all PD classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Additional information
15	Current unbalance	I_{unb}	mA		10.5	See 33.2.8.12
16	Power turn on time	T_{pon}	ms		400	See 33.2.8.13
17	Detection backoff time	T_{dbo}	sec	2		PSE detection backoff time limit.
18	Output capacitance during detection mode	C_{out}	nF		520	
19	Detection timing	T_{det}	ms		500	Time to complete detection of a PD.
20	Classification timing	T_{pdc}	ms	10	75	Time to classify the PD.
21	Error delay timing	T_{ed}	ms	750		Delay before PSE may attempt subsequent detection after power removal because of error condition.

33.2.8.1 Output voltage

The specification for V_{Port} in Table 33–5 shall include line and temperature variations. The voltage potential shall be measured between any conductor of one power pair and any conductor of the other power pair.

33.2.8.2 Load regulation

The specification for load regulation in Table 33–5 shall be met from 0.44W to 15.4W load step at a rate of change of 35mA/μs max. The voltage transients as a result of the load changes shall be limited to 3.5V/μs max.

33.2.8.3 Power feeding ripple and noise

The specification for power feeding ripple and noise in Table 33–5 shall be met for common-mode and/or pair-to-pair noise values for power outputs from 0.44W to 15.4W at operating $V_{Port.}$ The limits are meant to ensure data integrity. To meet EMI standards, lower values may be needed. For higher frequencies, see 33.4.4 and 33.4.5.

33.2.8.4 Maximum output current in normal powering mode at PSE min output voltage

For $V_{Port} > 44V$, the minimum value for I_{Port_max} in Table 33–5 shall be $15.4W/V_{Port}$.
The current I_{Port_max} ensures 15.4W min output power.

The PSE shall support the following AC current waveform parameters:

a) $I_{peak} = 0.4A$ minimum for 50ms minimum and 5% duty cycle minimum.
b) For $V_{Port} > 44V$, $I_{peak} = 17.6W/V_{Port}$.

33.2.8.5 Output current in startup mode

The specification for I_{Inrush} in Table 33–5 shall be met under the following conditions:

a) For duration of 50ms min, duty cycle = 5% min.
b) Measurement to be taken after 1ms to ignore startup transients.

c) During startup, the minimum I_{Inrush} requirement applies for duration T_{LIM}.
d) During startup, for PI voltages above 30V, the minimum I_{Inrush} requirement is as specified in Table 33–5, item 5.
e) During startup, for PI voltages between 10V and 30V, the minimum I_{Inrush} requirement is 60mA. See Figure 33C.4 and Figure 33C.6.

33.2.8.6 Overload current detection range

If I_{Port} in Table 33–5 exceeds I_{CUT} for longer than T_{ovld}, the PSE shall remove power from the PI. See Figure 33C.6.

In a PSE that supports the optional classification function (33.2.7), the minimum value of I_{CUT} may optionally be

$(P\_class \times 1000)/Vportmin$,

where P_class is the minimum power level at the output of the PSE (as specified by Table 33–3) and Vportmin is V_{Port} min in Table 33–5.

33.2.8.7 Overload time limit

After time duration of T_{ovld} as specified in Table 33–5, the PSE shall remove power from the PI. See Figure 33C.6.

33.2.8.8 Output current—at short circuit condition

The power shall be removed from the PI within T_{LIM}, as specified in Table 33–5, under the following conditions:

a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC input voltage up to the maximum voltage as specified in item 1 of Table 33–5.
c) Measurement to be taken after 1ms to ignore initial transients.

See Figure 33C.4 and Figure 33C.6.

33.2.8.9 Short circuit time limit

If a short circuit condition is detected, power removal from the PI shall begin within T_{LIM} and be complete by T_{Off}, as specified in Table 33–5. See Figure 33C.4 and Figure 33C.6.

33.2.8.10 Turn off time

The specification for T_{Off} in Table 33–5 shall apply to the discharge time from V_{Port} to 2.8Vdc with a test resistor of 320KΩ attached to the PI. In addition, it is recommended that the PI be discharged when turned off. The PSE enters the IDLE state when V_{Port} drops 1V below the steady-state value after the pi_powered variable is cleared (see Figure 33–6). The PSE remains in the IDLE state as long as the average voltage across the PI is V_{Off}. The IDLE State is the mode when the PSE is not in Detection, Classification, or normal powering mode.

33.2.8.11 Turn off voltage

The specification for V_{Off} in Table 33–5 shall apply to the PI voltage in the IDLE State.

33.2.8.12 Current unbalance

The specification for I_{unb} in Table 33–5 shall apply to the current unbalance between the two conductors of a power pair over the current load range. The 10.5mA value is based on a simulated output current unbalance of 3%.

33.2.8.13 Power turn on time

The specification for T_{pon} in Table 33–5 shall apply to the PSE power up time for a PD after completion of detection. If power is not applied as specified, a new detection cycle is initiated (See 33.2.3.1).

33.2.8.14 PSE stability

NOTE — Caution, when connected together as a system, the PSE and PD might exhibit instability at the PSE side or the PD side or both due to the presence of negative impedance at the PD input. See Annex 33D for PSE design guidelines to ensure stable operation.

33.2.9 Power supply allocation

A PSE shall not initiate power provision to a link if the PSE is unable to provide the maximum power level requested by the PD based on the PD's class. Where a PSE does not provide the optional classification function specified in 33.2.7, all PDs are treated as Class 0.

The PSE may manage the allocation of power based on additional information beyond the classification of the attached PD. Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically, the interaction between one PSE PI and another PSE PI in the same system is beyond the scope of this standard.

33.2.10 PSE power removal

Figure 33–7 shows the PSE monitor state diagrams. These state diagrams monitor for overload current, short circuit, inrush current, and the absence of the Maintain Power Signature (MPS).

If any of these conditions exists for longer than its related time limit, the power will be removed from the PI.

33.2.10.1 PSE Maintain Power Signature (MPS) requirements

The MPS consists of two components, an AC MPS component and a DC MPS component.

The PSE may optionally monitor the AC MPS component only, the DC MPS component only or both the AC and the DC MPS components.

33.2.10.1.1 PSE AC MPS component requirements

A PSE that monitors the AC MPS component shall meet the "AC Signal parameters" and "PSE PI voltage during AC disconnect detection" parameters in Table 33–6.

A PSE shall consider the AC MPS component to be present when it detects an AC impedance at the PI equal to or lower than |Zac1| as defined in Table 33–6.

A PSE shall consider the AC MPS component to be absent when it detects an AC impedance at the PI equal to or greater than |Zac2| as defined in Table 33–6. Power shall be removed from the PI when AC MPS has been absent for a time duration greater than T_{PMDO}.

A PSE may consider the AC MPS component to be either present or absent when it detects a AC impedance between the values |Zac1| and |Zac2| as defined in Table 33–6.

See Figure 33C.15 for timing relationships.

33.2.10.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if the DC current is greater than or equal to I_{Min2} max for a minimum of T_{MPS}. A PSE may consider the DC MPS component to be present or absent if the DC current is in the range I_{Min2}.

A PSE shall consider the DC MPS component to be absent when it detects a DC current in the range I_{Min1}. Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

The specification for T_{MPS} in Table 33–5 applies only to the DC MPS component. The PSE shall not remove power from the port when the DC current is greater than or equal to I_{Min2} max for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–5. This allows a PD to minimize its power consumption. See Figure 33C.9 for timing relationships.

Table 33–6—PSE PI parameters for AC disconnect-detection function

Item	Parameter	Symbol	Unit	Min	Max	Additional information
	AC signal parameters					
1a	PI probing AC voltage	V_open	V_{pp}	1.9	10% of the average value of V_{Port}, $44V<V_{Port}<60V$.	Includes noise, ripple, etc. V_open is the AC voltage across the PI when the PD is not connected to the PI and before the detection of this condition by the PSE.
		V_open1	V_p		30V, $V_{Port} \leq 44V$.	V_open1 is the AC voltage across the PI when the PD is not connected to the PI and after the detection of this condition by the PSE and the removal of power from the PI.
1b	AC probing signal frequency	F_p	Hz		500	
1c	AC probing signal slew rate	SR	V/µs		0.1	Positive or negative.

Table 33–6—PSE PI parameters for AC disconnect-detection function *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Additional information
	AC source output impedance					
2a	Source output current during the operation of the AC disconnect detection function	I_sac	mA		5	During operation of the AC disconnect detection function.
2b	PSE PI impedance during PD detection when measured at the PI of the PSE PI	R_rev	KΩ	45		Specified in 33.2.5 and Figure 33–8. Shown here to clarify the difference in PI impedance during the signature detection function.
	PSE PI voltage during AC disconnect detection					
3a	PI AC voltage when PD is connected	V_{CLOSE}	V_{pp}			See Table 33–5, item 3.
3b	PI voltage when PD is disconnected	V_{Port}	V_p		60	
3c	Disconnect detection time	T_{MPDO}	ms			See Table 33–5, item 7a.
	AC Maintain Power Signature					
4a	Shall not remove power from the PI	$\lvert Z_{ac1} \rvert$	KΩ		27	F_p = 5Hz, Testing voltage >2.5V. See Figure 33–10. Impedance shall have non-negative resistive component and a net capacitive reactive component.
4b	Shall remove power from the PI	$\lvert Z_{ac2} \rvert$	KΩ	1980		See Figure 33–11.

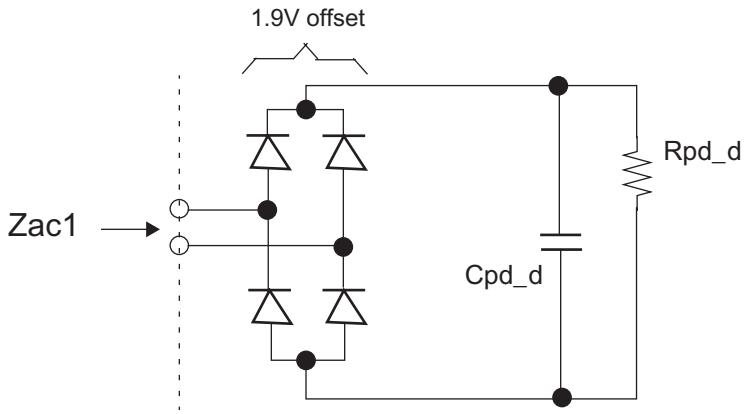


Figure 33–10—Z_{ac1} definition as indicated in Table 33–6
(Rpd_d, Cpd_d specified in Table 33–13. Cpd_d may be located either before or after the diode bridge.)

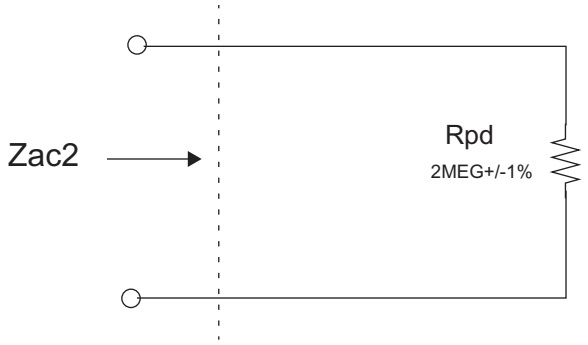


Figure 33–11—Z_{ac2} definition as indicated in Table 33–6

33.3 Powered devices

A PD is a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a powered device may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PI. PD capable devices that are neither drawing nor requesting power are also covered in this clause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

33.3.1 PD PI

The PD shall be capable of accepting power on either of two sets of PI conductors. The two conductor sets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal average voltage. Figure 33–5 in conjunction with Table 33–7 illustrates the two power modes.

Table 33–7—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{Port} , Negative V_{Port}	
2	Positive V_{Port} , Negative V_{Port}	
3	Negative V_{Port} , Positive V_{Port}	
4		Positive V_{Port} , Negative V_{Port}
5		Positive V_{Port} , Negative V_{Port}
6	Negative V_{Port} , Positive V_{Port}	
7		Negative V_{Port} , Positive V_{Port}
8		Negative V_{Port} , Positive V_{Port}

The PD shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the PD Mode-A column and the PD Mode-B column in Table 33–7.

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard.

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0V to 57V at the PI indefinitely without permanent damage.

33.3.2 PD state diagram

The PD shall provide the behavior of the state diagram shown in Figure 33–12.

33.3.2.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

33.3.2.2 Variables

The PD state diagram uses the following variables:

pd_reset
: An implementation specific control variable that unconditionally resets the PD state diagram to the NOT_MDI_POWERED state.
  Values: FALSE: The device has not been reset (default).
  TRUE: The device has been reset.

present_pd_signature
: Controls presenting the detection (see 33.3.3) and classification (see 33.3.4) signatures by the PD.
  Values: FALSE: The PD detection and classification signatures are not to be applied to the link.
  TRUE: The PD detection and classification signatures are to be applied to the link.

present_mps
: Controls applying MPS (see 33.3.6) to the link by the PD.
  Values: FALSE: The Maintain Power Signature (MPS) is not to be applied to the link.
  TRUE: The MPS is to be applied to the link.

mdi_power_required
: A control variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power.
  Values: FALSE: PD functionality is disabled.
  TRUE: PD functionality is enabled.

power_received
: An indication from the circuitry that power is present on the link.
  Values: FALSE: Power not being received.
  TRUE: Power being received.

33.3.2.3 State diagram

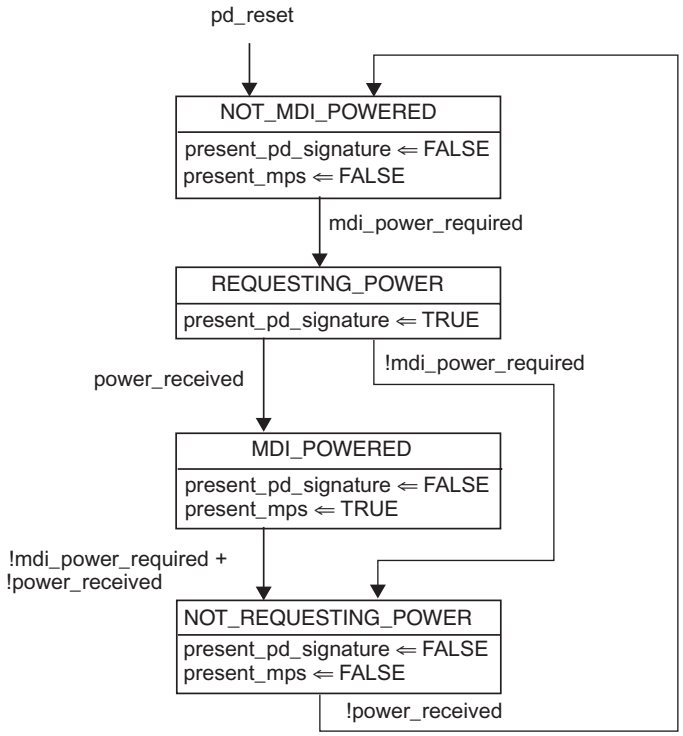


Figure 33–12—PD state diagram

33.3.3 PD valid and non-valid detection signatures

A PD shall present a valid detection signature at the PI between Positive V_{Port} and Negative V_{Port} of PD Mode A and between Positive V_{Port} and Negative V_{Port} of PD Mode B as defined in 33.3.1 while it is in a state where it will accept power via the PI, but is not powered via the PI.

A PD shall present a non-valid detection signature at the PI between Positive V_{Port} and Negative V_{Port} of PD Mode A and between Positive V_{Port} and Negative V_{Port} of PD Mode B as defined in 33.3.1 while it is in a state where it will not accept power via the PI.

When a PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which is it not drawing power.

The valid and non-valid detection signature regions are separated by guardbands. The guardbands for the V-I slope are the ranges 12KΩ to 23.75KΩ and 26.25KΩ to 45KΩ. A PD that presents a signature in a guardband is non-compliant.

V-I slope is the effective resistance calculated from the two voltage/current measurements made during the detection process.

$$\text{V-I slope} = (V_2 - V_1)/(I_2 - I_1) \quad (33\text{–}1)$$

where (V_1, I_1) and (V_2, I_2) are measurements made at the PD PI.

The valid PD detection signature shall have the characteristics of Table 33–8.

Table 33–8—Valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
V-I Slope (at any 1V or greater chord within the voltage range conditions)	2.7V to 10.1V	23.75	26.25	KΩ
V offset			1.9	V
I offset			10	μA
Input capacitance	2.7V to 10.1 V	0.05	0.12	μF
Input inductance	2.7V to 10.1 V		100	μH

A non-valid detection signature shall have one or both of the characteristics in Table 33–9

Table 33–9—Non-valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Range of values	Unit
V-I Slope	V < 10.1V	Either greater than 45 or less than 12	KΩ
Input Capacitance	V < 10.1V	Greater than 10	μF

33.3.4 PD classifications

A PD may be classified by the PSE based on the classification information provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Class 0 is the default for PDs. However, to improve power management at the PSE, the PD may opt to provide a signature for Class 1 to 3.

The PD is classified based on power. The classification of the PD is the maximum power that the PD will draw across all input voltages and operational modes.

A PD shall return Class 0 to 3 in accordance with the maximum power draw as specified by Table 33–10.

Table 33–10—PD power classification

Class	Usage	Range of maximum power used by the PD
0	Default	0.44 to 12.95 Watts
1	Optional	0.44 to 3.84 Watts
2	Optional	3.84 to 6.49 Watts
3	Optional	6.49 to 12.95 Watts
4	Not Allowed	Reserved for Future Use

NOTE—Class 4 is defined but is reserved for future use. A Class 4 signature cannot be provided by a compliant PD.

In addition to a valid detection signature, PDs shall provide the characteristics of a classification signature as specified in Table 33–11. A PD shall present one, and only one, classification signature during classification.

Table 33–11—Classification signature, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	14.5V to 20.5V	0	4	mA
Current for Class 1	14.5V to 20.5V	9	12	mA
Current for Class 2	14.5V to 20.5V	17	20	mA
Current for Class 3	14.5V to 20.5V	26	30	mA
Current for Class 4	14.5V to 20.5V	36	44	mA

33.3.5 PD power

The power supply of the PD shall operate within the characteristics in Table 33–12.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Table 33–12—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input voltage	V_{Port}	Vdc	36	57	See 33.3.5.1
2	Input average power	P_{Port}	W		12.95	See 33.3.5.2
3	Input inrush current	I_{Inrush}	mA		400	Peak Value—See 33.3.5.3
4	Peak operating current, Class 0, 3	I_{Port}	mA		400	See 33.3.5.4
	Peak operating current, Class 1	I_{Port}	mA		120	
	Peak operating current, Class 2	I_{Port}	mA		210	
5	Input current (DC or RMS), V_{Port}=37Vdc	I_{Port}	mA		350	See 33.3.5.3
	Input current (DC or RMS), V_{Port}=57Vdc	I_{Port}	mA		230	
6	PI capacitance during normal powering mode	C_{Port}	μF	5		See 33.3.5.5
7	Ripple and noise, < 500Hz		V_{PP}		0.5	See 33.3.5.6
	Ripple and noise, 500Hz to 150KHz		V_{PP}		0.2	
	Ripple and noise, 150KHz to 500KHz		V_{PP}		0.15	
	Ripple and noise, 500KHz to 1MHz		V_{PP}		0.1	
8	a) PD Power supply turn on voltage	V_{On}	V		42	See 33.3.5.7
	b) PD power supply turn off voltage	V_{Off}	V	30		
9	PD classification stability time	T_{class}	ms		5	See 33.3.5.8
10	Backfeed voltage	V_{bfd}	V		2.8	See 33.3.5.10

33.3.5.1 Input voltage

The specification for V_{Port} in Table 33–12 is for the input voltage range after startup, and it includes loss in the cabling plant. The PD shall turn on at a voltage less than V_{On}. After the PD turns on, the PD shall stay on over the entire V_{Port} range. The PD shall turn off at a voltage less than V_{Port} minimum and greater than V_{Off}.

33.3.5.2 Input average power

The specification for P_{Port} in Table 33–12 shall apply for the input power averaged over 1 second.

$P_{Port} = V_{Port} \times I_{Port}$, measured when the PD is fed by 44V to 57V with 20Ω in series.

33.3.5.3 Input inrush current

Input inrush current at startup will be limited by the PSE if $C_{Port} < 180\mu F$, as specified in Table 33–5.

If $C_{Port} \geq 180\mu F$, input inrush current shall be limited by the PD so that I_{Inrush} max is satisfied.

33.3.5.4 Peak operating current

At any operating condition the peak current shall not exceed P_{Port} max/V_{Port} for more than 50ms max and 5% duty cycle max. Peak current shall not exceed I_{Port} max.

Ripple current content (I_{ac}) superimposed on the DC current level (I_{dc}) is allowed if the total input power is less than or equal to P_{Port} max.

The RMS, DC and ripple current shall be bounded by the following equation: $Irms = \sqrt{(Idc)^2 + (Iac)^2}$.

The maximum I_{Port_dc} and I_{Port_rms} values for all operating V_{Port} range shall be defined by the following equation: I_{Port_max} [mA] =12950/V_{Port}.

33.3.5.5 PI capacitance during normal powering mode

While there is no max capacitance, the PD max input capacitance (C_{Port} in Table 33–12) and the PD input circuitry shall be designed in such a way that when a PD is connected to a PSE through a series resistance of up to 20Ω and the PSE voltage is changed from 44V to 57V, the peak current I_{Port} will be as specified in Table 33–12, item 4, for a maximum duration of 50ms. Input capacitance of 180μF or less requires no special input considerations.

33.3.5.6 Ripple and noise

The specification for ripple and noise in Table 33–12 shall be for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry. The ripple and noise specification shall be for all operating voltages in the range defined by Table 33–12, item 1, and over the range of input power of the device.

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 33–5, item 3.

Limits are provided to ensure data integrity. To meet EMI standards, lower values may be needed.

The system designer is advised to assume the worst case condition in which both PSE and PD generate the maximum noise allowed by Table 33–5 and Table 33–12, which may cause a higher noise level to appear at

the PI than the standalone case as specified by this clause.

33.3.5.7 PD power supply turn on / turn off voltages

The PD shall turn on at V_{On} and turn off at V_{Off} (as specified in Table 33–12) when connected to a PSE through a 20Ω series resistor. The PD shall turn on or off without startup oscillation and within the first trial at any load value.

33.3.5.8 PD classification stability time

The PD classification signature shall be valid within T_{class} as specified in Table 33–12 and remain valid for the duration of the classification period.

33.3.5.9 PD stability

NOTE—Caution, when connected together as a system, the PSE and PD might exhibit instability at the PSE side or the PD side or both due to the presence of negative impedance at the PD input. See Annex 33D for PD design guidelines to ensure stable operation.

33.3.5.10 Backfeed Voltage

When V_{Port} max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–7, the voltage measured across the PI for Mode B with a 100KΩ load resistor connected shall not exceed V_{bfd} max as specified in Table 33–12. When V_{Port} max is applied across the PI at either polarity specified on the conductors for Mode B according to Table 33–7, the voltage measured across the PI for Mode A with a 100KΩ load resistor connected shall not exceed V_{bfd} max.

33.3.6 PD Maintain Power Signature

In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI. The MPS shall be both:

a) Current draw equal or above the minimum Input current (I_{Port} min) as specified in Table 33–13 for a minimum duration of 75ms followed by an optional MPS dropout for no longer than 250ms, and
b) Input impedance with resistive and capacitive components as defined in Table 33–13.

A PD that does not maintain any one of:

c) The minimum input current as defined in Table 33–13 for at least 75ms, and
d) Input impedance with resistive and capacitive components as defined by Table 33–13 (also, see Figure 33–10 and Figure 33–11),

may have its power removed within the limits of T_{MPDO} as specified in Table 33–5.

Powered PDs that no longer require power shall remove both components a) and b) of the MPS. To ensure power removal, the impedance of the PI must rise above Z_{ac2} as specified in Table 33–6.

Table 33–13—PD Maintain Power Signature

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input current	I_{port}	mA	10		See 33.3.6.1
2	Input resistance	R_{pd_d}	KΩ		26.25	
3	Input capacitance	C_{pd_d}	μF	0.05		With 0V to 57V DC bias applied

33.3.6.1 Input current

The specification for I_{Port} in Table 33–13 includes the following additional information:

a) I_{Port} =10mA min for $C_{port} \leq 180\mu F$.
b) I_{Port} = 10mA × C_{port} [μF] /180 for $C_{port} > 180\mu F$, or the PD will need to make special accommodation to ensure that the 10 mA minimum current be maintained within the limits of T_{MPDO} when the PD input voltage is dropped from 57V to 44V at the maximum allowable slew rate.
c) Minimum current requirement applies when the PD is fed by 44V to 57V with 20Ω in series.

33.4 Additional Electrical specifications

This clause defines additional electrical specifications for both the PSE and PD. The specifications apply for all PSE and PD operating conditions at the cabling side of the mated connection of the PI. The requirements apply during data transmission only when specified as an operating condition.

The requirements of 33.4 are consistent with the requirements of the PHYs of 10BASE-T, 100BASE-TX, and 1000BASE-T.

33.4.1 Isolation

The PSE shall provide electrical isolation between the PI device circuits, including frame ground (if any), and all PI leads.

The PD shall provide electrical isolation between all external conductors, including frame ground (if any), and all PI leads.

This electrical isolation shall be in accordance with the isolation requirements between SELV circuits and telecommunication network connections in subclause 6.2 of IEC 60950-1:2001.

This electrical isolation shall withstand at least one of the following electrical strength tests:

a) 1500 Vrms steady-state at 50-60 Hz for 60 seconds, applied as specified in subclause 6.2 of IEC 60950-1:2001.
b) An impulse test consisting of a 1500 V, 10/700μs waveform, applied 10 times, with a 60 second interval between pulses, applied as specified in subclause 6.2 of IEC 60950-1:2001.

There shall be no insulation breakdown, as defined in subclause 6.2.2.3 of IEC 60950-1:2001.

Conductive link segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

33.4.1.1 Electrical isolation environments

There are two electrical power distribution environments to be considered that require different electrical isolation properties. They are as follows:

— **Environment A:** When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
— **Environment B:** When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

33.4.1.1.1 Environment A requirements

Attachment of network segments via NIDs that have multiple instances of a twisted pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the basic MAU/PHY/medium standard. (See 14.3.1.1, TP-PMD, and 40.6.1.1.) Equipment with multiple instances of PSE and/or PD shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

A multi-port NID complying with Environment A requirements does not require electrical power isolation between link segments.

An Environment A PSE shall switch the more negative conductor. It is allowable to switch both conductors.

33.4.1.1.2 Environment B requirements

The attachment of network segments that cross environment A boundaries requires electrical isolation between each segment and all other attached segments as well as to the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the basic MAU/PHY/medium standard (See 14.3.1.1, TP-PMD, and 40.6.1.1.). Equipment with multiple instances of PSE and/or PD shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated.

The requirements for interconnected electrically conducting link segments that are partially or fully external to a single building environment may require additional protection against lightning strikes or other hazards. Protection requirements for such hazards are beyond the scope of this standard. Guidance on these requirements may be found in Section 6 of IEC 60950-1:2001, as well as any local and national codes related to safety.

33.4.2 Fault tolerance

Each wire pair of the PSE or PD when it is encompassed within the MDI shall meet the fault tolerance requirements of the appropriate specifying clause, (See 14.3.1.2.7, Clause 25, and 40.8.3.4). When a PSE is not encompassed within an MDI, the PSE PI shall meet the fault tolerance requirements of this subclause.

The PSE PI shall withstand without damage the application of short circuits of any wire to any other wire within the cable for an indefinite period of time. The magnitude of the current through such a short circuit shall not exceed I_{LIM} max as defined in Table 33–5, item 10.

Each wire pair shall withstand, without damage, a 1000V common-mode impulse applied at Ecm of either polarity (as indicated in Figure 33–13). The shape of the impulse shall be (0.3/50)μs (300ns virtual front

time, 50μs virtual time or half value), as defined in IEC 60060, where Ecm is an externally applied AC voltage as shown in Figure 33–13.

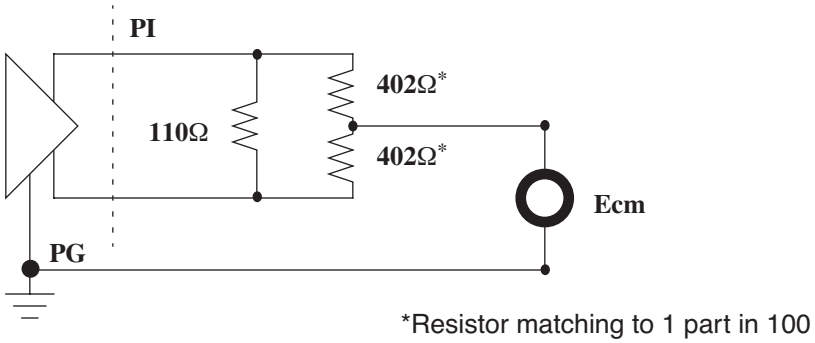


Figure 33–13—PI fault tolerance test circuit

33.4.3 Impedance balance

Impedance balance is a measurement of the common-mode-to-differential-mode offset of the PI. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed:

$$29 - 17\log_{10}(f/10)\text{dB} \quad (33\text{–}2)$$

from 1.0-20 MHz for a 10 Mb/s PHY, and

$$34 - 19.2\log_{10}(f/50)\text{dB} \quad (33\text{–}3)$$

from 1.0–100 MHz for a 100 Mb/s or greater PHY, where f is the frequency in MHz.

The impedance balance is defined as

$$20\log_{10}(\text{Ecm}/\text{Edif}) \quad (33\text{–}4)$$

where Ecm is an externally applied AC voltage as shown in Figure 33–14 and Edif is the resulting waveform due only to the applied sine wave.

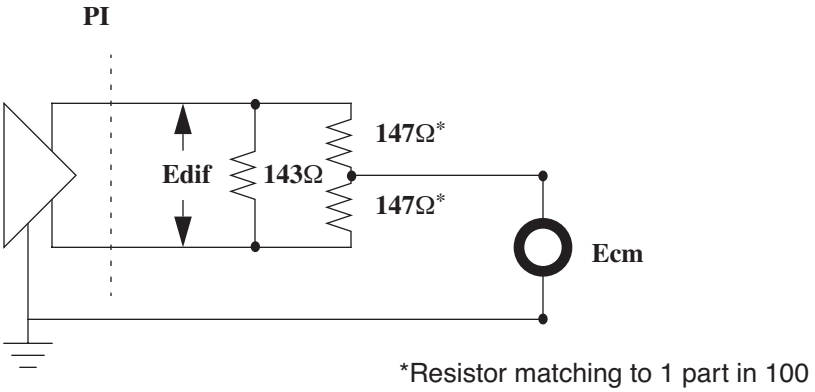


Figure 33–14—PI impedance balance test circuit

33.4.4 Common-mode output voltage

The magnitude of the common-mode AC output voltage measured according to Figure 33–15 and Figure 33–16 at the transmit PI while transmitting data and with power applied, Ecm_out, shall not exceed 50mV peak when operating at 10Mb/s, and 50mV peak-to-peak when operating at 100Mb/s or greater. The magnitude of the common-mode AC voltage shall not exceed 50mV peak-to-peak measured at all other PIs. The frequency of the measurement shall be from 1MHz to 100MHz.

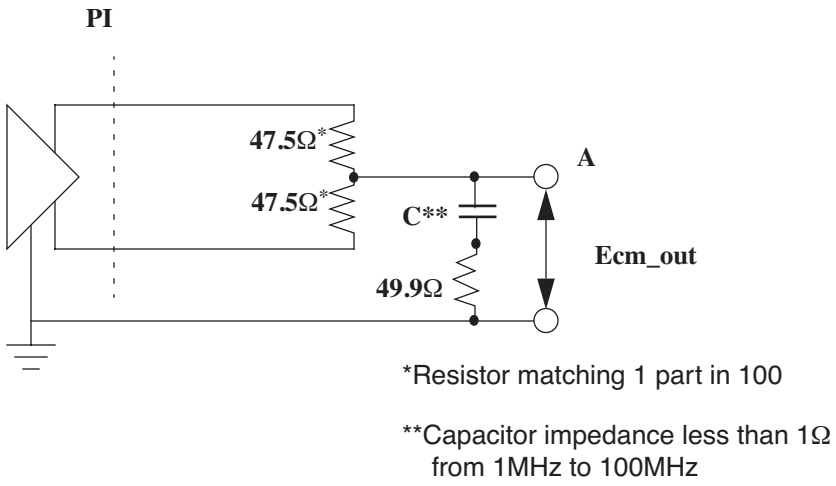


Figure 33–15—Common-mode output voltage test

The PIs shall be tested with the PHY transmitting data, an operating PSE or PD, and with the following PSE load or PD source requirements:

1) When testing a PSE, the PIs that supply power are terminated as illustrated in Figure 33–16. The PSE load, R, in Figure 33–16 is adjusted so that the PSE output current, I_{out}, is 10mA and then 350mA, while measuring Ecm_out on all PIs.
2) While testing a PD, the PIs that require power shall be terminated as illustrated in Figure 33–16. A voltage source, Vsource in Figure 33–16, supplies power to the PD and is adjusted to 36Vdc and 57Vdc, while measuring Ecm_out on all PIs.

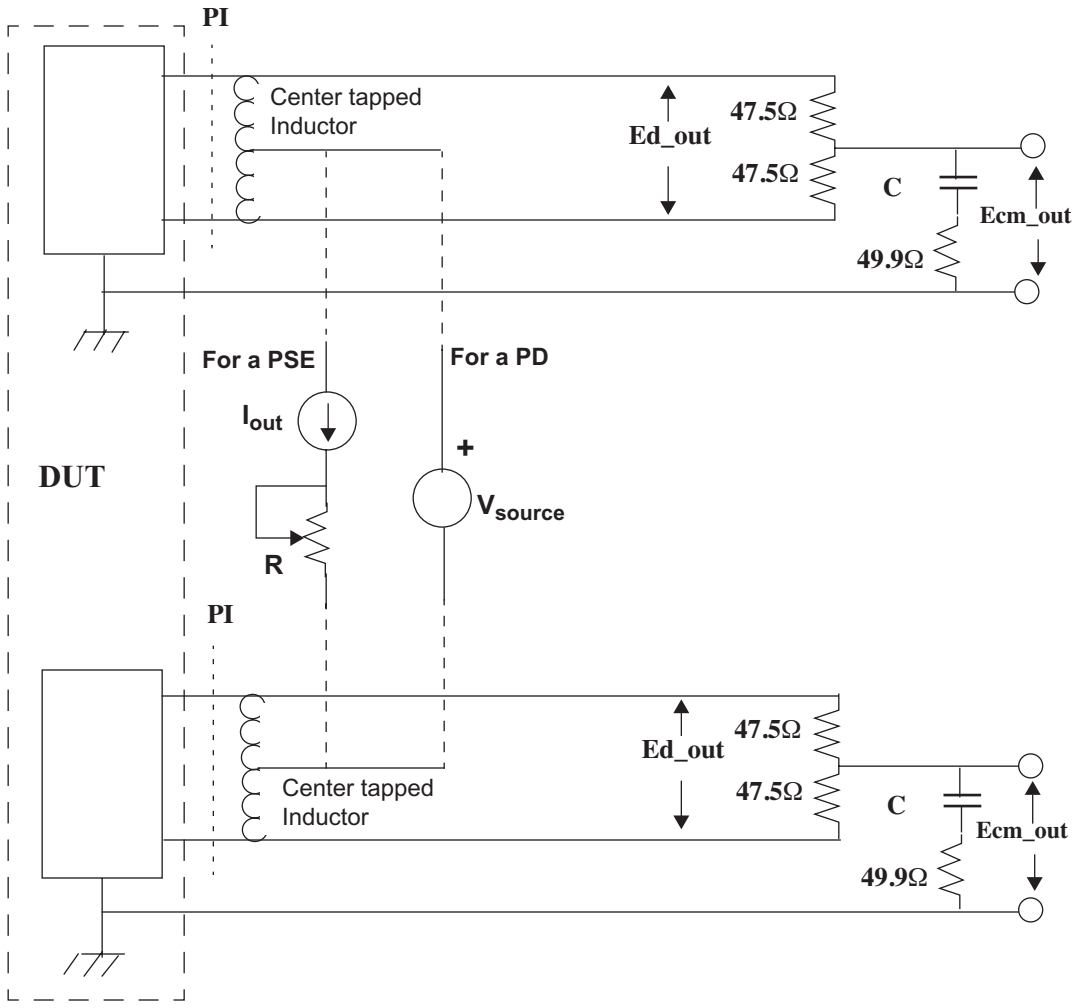


Figure 33–16—PSE and PD terminations for common-mode output voltage test

NOTE—The Implementer should consider any applicable local, national, or international regulations that may require more stringent specifications. One such specification can be found in the European Standard EN 55022:1998.

33.4.5 Pair-to-pair output noise voltage

The pair-to-pair output noise voltage (see Figure 33–17) will be limited by the resulting electromagnetic interference due to this AC voltage. This AC voltage can be ripple from the power supply (Table 33–5, item

3) or from any other source. A system integrating a PSE shall comply with applicable local and national codes for the limitation of electromagnetic interference.

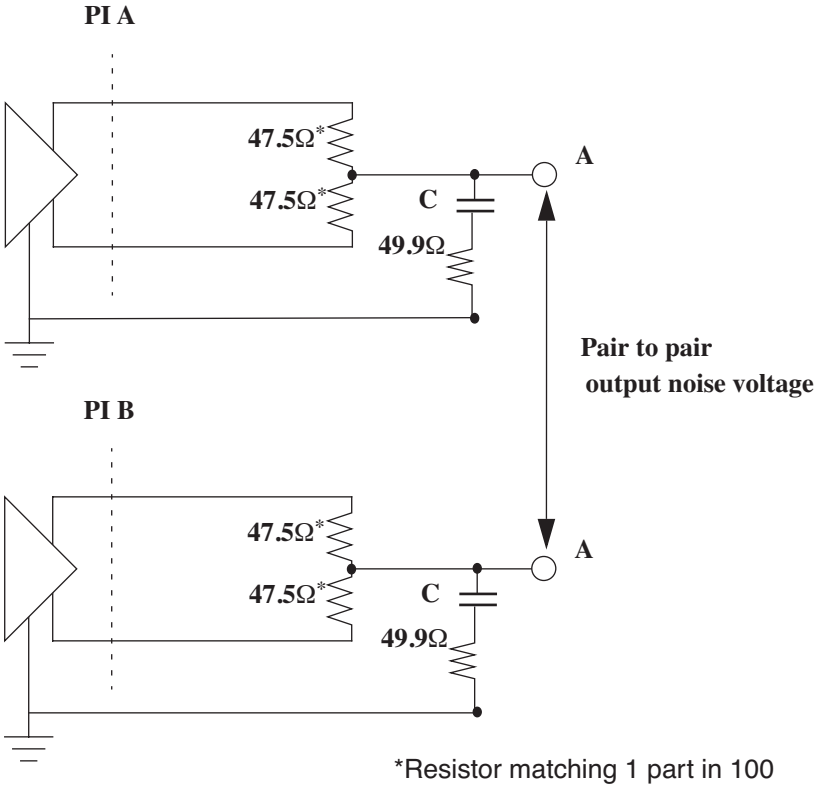


Figure 33–17—Pair to pair output noise voltage test

33.4.6 Differential noise voltage

The coupled noise, Ed_out in Figure 33–16, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10mV peak-to-peak measured from 1MHz to 100MHz.

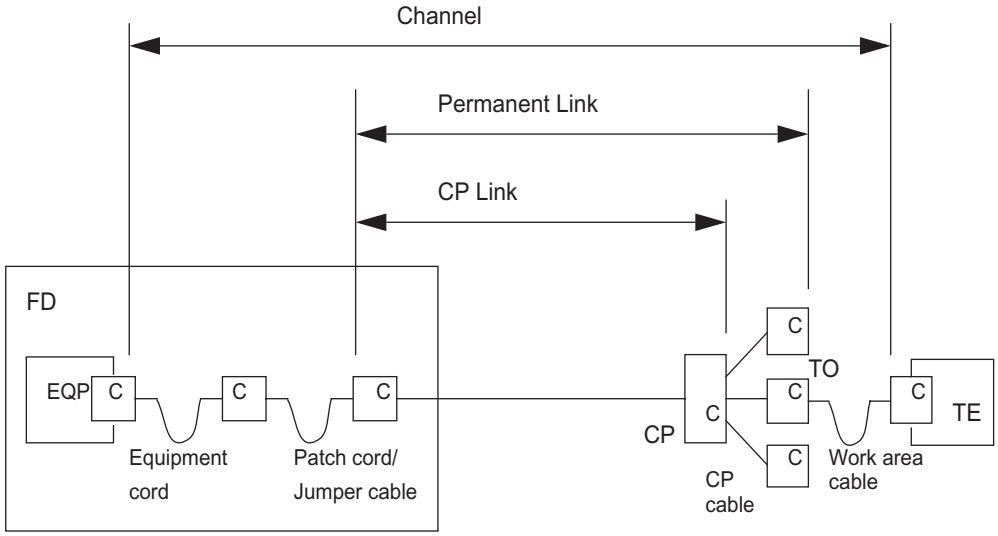
The PSE and PD shall be terminated as illustrated in Figure 33–16 and tested with the PSE and PD conditions as specified in 33.4.4, item 1) and item 2).

33.4.7 Return loss

The differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY. In addition, all pairs terminated at an MDI should maintain a nominal common-mode impedance of 75Ω. The common-mode termination is affected by the presence of the power supply, and this should be considered to ensure proper termination.

33.4.8 Midspan PSE device additional requirements

The cabling specifications for 100Ω balanced cabling are described in ISO/IEC 11801-2002. Some cable category specifications that only appear in earlier editions are also supported. The configuration of "channel" and "permanent link" is defined in Figure 33–18.



FD = floor distributor; EQP = equipment; C = connection (mated pair);
CP = consolidation point; TO = telecommunications outlet;
TE = terminal equipment

Figure 33–18—Floor distributor channel configuration

The ISO/IEC 11801 defines in 5.6.1 two types of Equipment interface to the cabling system: "Interconnect model" and the "cross-connect model." See Figure 33–19.

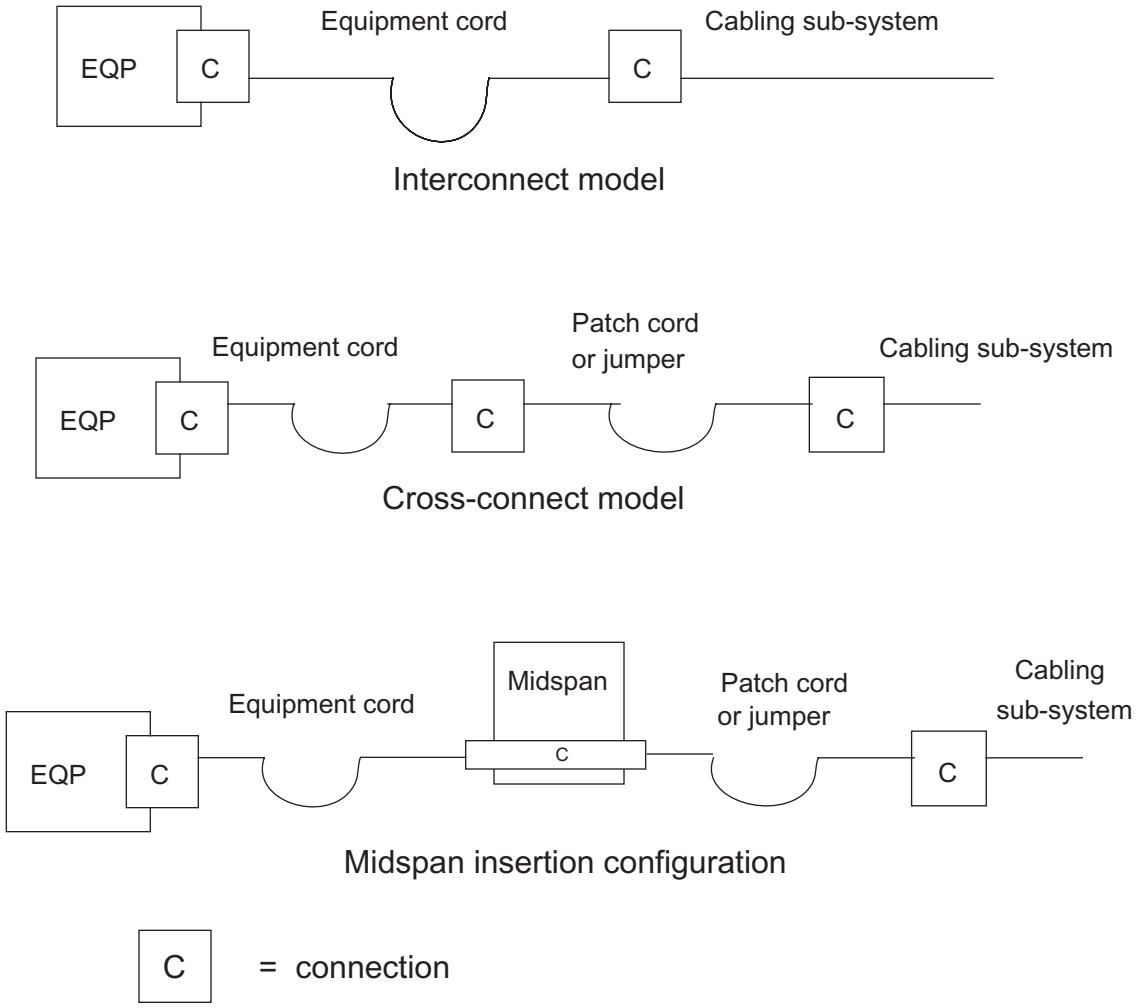


Figure 33–19—Interconnect model, cross-connect model, and midspan insertion configuration

The insertion of a Midspan PSE at the Floor Distributor (FD) shall comply with the following guidelines:

a) If the existing FD configuration is of the "Interconnect model" type, the Midspan PSE can be added, provided it does not increase the length of the resulting "channel" to more than specified 100 meters as defined in ISO/IEC 11801.

b) If the existing FD configuration is of the "Cross-connect model" type, the Midspan PSE needs to be installed instead of one of the connection pairs in the FD. In addition, the installation of the Midspan PSE shall not increase the length of the resulting "channel" to more than specified 100 meters as defined in ISO/IEC 11801.

Configurations with the Midspan PSE in the cabling channel shall not alter the transmission requirements of the "permanent link." A Midspan PSE inserted into a channel shall provide continuity for the signal pairs. A

Midspan PSE shall not provide DC continuity between the two sides of the segment for the pairs that inject power.

The requirements for the two pair category 5 channel are found in 25.4.6.

NOTE—Appropriate terminations may be applied to the interrupted pairs on both sides of the midspan device.

33.4.8.1 "Connector" or "telecom outlet" Midspan PSE device transmission requirements

The Midspan PSE equipment to be inserted as "Connector" or "Telecom outlet" shall meet the following transmission parameters. These parameters should be measured using the test procedures of ISO 11801:2002 for connecting hardware.

33.4.8.1.1 NEXT (Near End Crosstalk)

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. NEXT loss shall be measured for Midspan PSE devices for the transmit and receive pairs from 1MHz to 100MHz and shall meet the values determined by Equation (33–5). However, for frequencies that correspond to calculated values greater than 65dB, the requirement reverts to the minimum requirement of 65dB.

$$NEXT_{conn} \geq 40 - 20\log(f/100)\text{dB} \quad (33–5)$$

33.4.8.1.2 Insertion loss

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. Insertion loss shall be measured for Midspan PSE devices for the transmit and receive pairs from 1MHz to 100MHz, and shall meet the values determined by Equation (33–6). However, for frequencies that correspond to calculated values less than 0.1dB, the requirement reverts to the maximum requirement of 0.1dB.

$$Insertion\_loss_{conn} \leq 0.04\ SQRT(f)\ dB \quad (33–6)$$

33.4.8.1.3 Return loss

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss shall be measured for Midspan PSE devices for the transmit and receive pairs from 1MHz to 100Mhz and shall meet or exceed the values specified in Table 33–14.

Table 33–14—Connector return loss

Frequency	Return loss
1MHz≤f<20MHz	23 dB
20MHz≤f≤100 MHz	14 dB

33.4.8.1.4 Work area or equipment cable Midspan PSE

Replacing the work area or equipment cable with a cable that includes a Midspan PSE should not alter the requirements of the cable. This cable shall meet the requirements of this clause and the specifications for a

Category 5 (jumper) cord as specified in ISO/IEC 11801:2002 for insertion loss, NEXT, and return loss for the transmit and receive pairs.

33.5 Environmental

33.5.1 General safety

All equipment meeting this standard shall conform to IEC 60950-1:2001. In particular, the PSE shall be classified as a Limited Power Source in accordance with IEC 60950-1:2001.

Equipment shall comply with all applicable local and national codes related to safety.

33.5.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns. The list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements. LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification of an existing network.

33.5.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

33.5.4 Patch panel considerations

It is possible that the current carrying capability of a cabling cross-connect may be exceeded by a PSE. The designer should consult the manufacturers' specifications to ensure compliance with the appropriate requirements.

33.5.5 Cabling resistance unbalance

Resistance unbalance is a measure of the difference in resistance between the two conductors in the 100Ω balanced cabling system. The resistance unbalance shall be as specified in IEC 11801 Edition 2, Clause 6.4.8 (reference: 3 percent).

The resistance unbalance as defined in IEC 61156-1 is

((Rmax – Rmin)/(Rmax + Rmin)) × 100 percent, (33–7)

where Rmax is the resistance of the conductor with the highest resistance, and Rmin is the resistance of the conductor with the lowest resistance.

33.5.6 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to a PSE or PD. Other than voice signals, the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56Vdc, applied to the line through a balanced 400Ω source impedance. Ringing voltage is a composite signal consisting of an AC component and a DC component. The AC component is up to 175Vp at 20Hz to 60Hz with a 100Ω source resistance. The DC component is 56Vdc with 300Ω to 600Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Application of any of the above voltages to the PI of a PSE or a PD shall not result in any safety hazard.

33.5.7 Electromagnetic emissions

The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

33.5.8 Temperature and humidity

The PD and PSE powered cabling link segment is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling. Specific requirements and values for these parameters are beyond the scope of this standard.

33.5.9 Labeling

It is recommended that the PSE or PD (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Power classification and power level in terms of maximum current drain over the operating voltage range, 44V to 57V, applies for PD only,
b) Port type (e.g., 100BASE-TX, TIA Category or ISO Class),
c) Any applicable safety warnings, and
d) "PSE" or "PD" as appropriate.

33.6 Management function requirements

Management of the PSE is optional. If the PSE is instantiated in the same physical package as a PHY and a Clause 22 MII or a Clause 35 GMII is physically implemented, then management access shall be via the MII Management interface. Where no physical embodiment of the MII or GMII exists and management is supported, equivalent management capability shall be provided.

33.6.1 PSE registers

A PSE shall use register address 11 for its control and register address 12 for its status functions.

Some of the bits within registers are defined as latching high (LH). When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

33.6.1.1 PSE Control register (Register 11) (R/W)

The assignment of bits in the PSE Control register is shown in Table 33–15. The default value for each bit of the PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

Table 33–15—PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
11.15:4	Reserved	Ignore when read	RO
11.3:2	Pair Control	(11.3) (11.2) 1 1 = Reserved 1 0 = PSE pinout Alternative B 0 1 = PSE pinout Alternative A 0 0 = Reserved	R/W
11.1:0	PSE Enable	(11.1) (11.0) 1 1 = Reserved 1 0 = Force Power Test Mode 0 1 = PSE Enabled 0 0 = PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

33.6.1.1.1 Reserved bits (11.15:4)

Bits 11.15:4 are reserved for future standardization. They shall not be affected by writes and shall return a value of ‘0’ when read. To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of ‘0’ and ignore reserved bits on read.

33.6.1.1.2 Pair Control (11.3:2)

Bits 11.3:2 report the supported PSE Pinout Alternative specified in 33.2.1. A PSE may also provide the option of controlling the PSE Pinout Alternative through these bits. Provision of this option is indicated through the Pair Control Ability (12.0) bit. A PSE that does not support this option shall ignore writes to these bits and shall return the value that reports the supported PSE Pinout Alternative.

When read as ‘01’, bits 11.3:2 indicate that only PSE Pinout Alternative A is supported by the PSE. When read as ‘10’, bits 11.3:2 indicate that only PSE Pinout Alternative B is supported by the PSE.

Where the option of controlling the PSE Pinout Alternative through these bits is provided, setting bits 11.3:2 to ‘01’ shall force the PSE to use only PSE Pinout Alternative A and setting bits 11.3:2 to ‘10’ shall force the PSE to use only PSE Pinout Alternative B.

If bit 12.0 is ‘1’, writing to these register bits shall set mr_pse_alternative to the corresponding value: ‘01’ = A and ‘10’ = B. The combinations ‘00’ and ‘11’ for bits 11.3:2 are reserved and will never be assigned. Reading bits 11.3:2 will return an unambiguous result of ‘01’ or ‘10’ that may be used to determine the presence of the PSE Control register.

33.6.1.1.3 PSE Enable (11.1:0)

The PSE function shall be disabled by setting bits 11.1 to logic zero and 11.0 to logic zero. When the PSE function is disabled, the MDI shall function as it would if it had no PSE function. The PSE function shall be enabled by setting bits 11.1 to a logic zero and 11.0 to a logic one. When bit 11.1 is a logic one, and bit 11.0 is a logic zero, a test mode is enabled. This test mode supplies power without regard to PD detection.

Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power. The combination '11' for bits 11.1:0 has been reserved for future use.

NOTE—Caution, test mode may damage connected non-PD, legacy, twisted pair Ethernet devices or other non-Ethernet devices, especially in split application wiring schemes.

33.6.1.2 PSE Status register (Register 12) (R/W)

The assignment of bits in the PSE Status register is shown in Table 33–16.

33.6.1.2.1 Reserved bits (12.15:13)

Bits 12.15:13 are reserved for future standardization. They shall not be affected by writes and shall return a value of '0' when read. To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of '0' and ignore reserved bits on read.

33.6.1.2.2 Power Denied (12.12)

When read as a logic one, bit 12.12 indicates that power has been denied. This bit shall be set to '1' when the PSE state diagram (Figure 33–6) enters the state 'POWER_DENIED'. The Power Denied bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.3 Valid Signature (12.11)

When read as a logic one, bit 12.11 indicates that a valid signature has been detected. This bit shall be set to '1' when mr_valid_signature transitions from FALSE to TRUE. The Valid Signature bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.4 Invalid Signature (12.10)

When read as a logic one, bit 12.10 indicates that an invalid signature has been detected. This bit shall be set to '1' when the PSE state diagram (Figure 33–6) enters the state 'SIGNATURE_INVALID'. The Invalid Signature bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.5 Short Circuit (12.9)

When read as a logic one, bit 12.9 indicates that a short circuit condition has been detected. This bit shall be set to '1' when the PSE state diagram (Figure 33–6) enters the state 'ERROR_DELAY_SHORT'. The Short Circuit bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.6 Overload (12.8)

When read as a logic one, bit 12.8 indicates that an overload condition has been detected. This bit shall be set to '1' when the PSE state diagram (Figure 33–6) enters the state 'ERROR_DELAY_OVER'. The Overload bit shall be implemented with latching high behavior as defined in 33.6.1.

Table 33–16—PSE Status register bit definitions

Bit(s)	Name	Description	R/W[a]
12.15:13	Reserved	Ignore when read	RO
12.12	Power Denied	1 = Power has been denied 0 = Power has not been denied	RO/ LH
12.11	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
12.10	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
12.9	Short Circuit	1 = Short circuit condition detected 0 = No short circuit condition detected	RO/ LH
12.8	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
12.7	MPS Absent	1 = MPS absent condition detected 0 = No MPS absent condition detected	RO/ LH
12.6:4	PD Class	(12.6) (12.5) (12.4) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Reserved 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Class 0	RO
12.3:1	PSE Status	(12.3) (12.2) (12.1) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Implementation specific fault 1 0 0 = Test error 0 1 1 = Test mode 0 1 0 = Delivering power 0 0 1 = Searching 0 0 0 = Disabled	RO
12.0	Pair Control Ability	1 = PSE pinout controllable by Pair Control bits 0 = PSE pinout Alternative fixed	RO

[a]RO = Read Only, LH = Latched High

33.6.1.2.7 MPS Absent (12.7)

When read as a logic one, bit 12.7 indicates that an MPS Absent condition has been detected. The MPS Absent bit shall be set to ‘1’ when the PSE state diagram (Figure 33–6) transitions directly from the state POWER_ON to IDLE due to tpmdo_timer_done being asserted. The MPS Absent bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.8 PD Class (12.6:4)

Bits 12.6:4 report the PD Class of a detected PD as specified in 33.2.6 and 33.2.7. The value in this register is valid while a PD is connected, i.e., while the PSE Status (12.3:1) bits are reporting Delivering Power. The combinations '101', '110' and '111' for bits 12.6:4 have been reserved for future use.

33.6.1.2.9 PSE Status (12.3:1)

Bits 12.3:1 report the current status of the PSE. When read as '000', bits 12.3:1 indicate that the PSE state diagram (Figure 33–6) is in the state DISABLED. When read as '010', bits 12.3:1 indicate that the PSE state diagram is in the state POWER_ON. When read as '011', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_MODE. When read as '100', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_ERROR. When read as '101', bits 12.3:1 indicate that the PSE state diagram is in the state IDLE due to the variable error_condition = true. When read as '001', bits 12.3:1 indicate that the PSE state diagram is in a state other than those listed above.

The combinations '111' and '110' for bits 12.3:1 have been reserved for future use.

33.6.1.2.10 Pair Control Ability (12.0)

When read as a logic one, bit 12.0 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.1) is used for PD detection and power through the Pair Control (11.3:2) bits. When read as a logic zero, bit 12.0 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2) bits.

33.7 Protocol Implementation Conformance Statement (PICS) proforma for Clause 33, DTE Power via MDI

33.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3af-2003, DTE Power via MDI, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

33.7.2 Identification

33.7.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	

1—Required for all implementations

2—May be completed as appropriate in meeting the requirements for the identification.

3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).

33.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3af-2003, Clause 33, DTE Power via MDI
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to the standard.)	
Date of Statement	

33.7.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDCL	PD Classification	33.3.4	PD supports classification	O	Yes [ ] No [ ]

33.7.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*CL	Implementation supports classification	33.2.7	Optional	O	Yes [ ] No [ ]
*END	Endpoint PSE	33.2.1	PSE implemented as an end-point device	O/1	Yes [ ] No [ ]
*ENDA	Alternative A Endpoint PSE	33.2.1	PSE implements Alternative A	END:O.2	Yes [ ] No [ ]
*ENDB	Alternative B Endpoint PSE	33.2.1	PSE implements Alternative B	END:O.2	Yes [ ] No [ ]
*MAN	PSE supports management registers accessed through MII Management Interface	33.6	Optional	O	Yes [ ] No [ ]
*MID	Midspan PSE	33.2.1	PSE implemented as a mid-span device	O/1	Yes [ ] No [ ]
*PA	Power Allocation	33.2.9	PSE implements power supply allocation	O	Yes [ ] No [ ]
*PCA	Pair control ability - PSE supports the option to control which PSE Pinout is used	33.6.1.1.3	Optional	O	Yes [ ] No [ ]
*AC	Monitor AC MPS	33.2.10.1.1	PSE monitors for AC MPS	O.3	Yes [ ] No [ ]
*DC	Monitor DC MPS	33.2.10.1.2	PSE monitors for DC MPS	O.3	Yes [ ] No [ ]

33.7.3 PICS proforma tables for DTE Power via MDI

33.7.3.1 Common device features

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Compatibility Considerations.	33.1.2	PDs and PSEs compatible at their PIs.	M	Yes [ ]

33.7.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location.	33.2.1	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated.	M	Yes [ ]
PSE2	Alternative B.	33.2.1	Only implementation allowed for Midspan.	MID:M	Yes [ ] N/A [ ]
PSE3	Alternative A and Alternative B.	33.2.2	Not operate on same link segment simultaneously.	END:M	Yes [ ] N/A [ ]
PSE4	PSE behavior.	33.2.3	In accordance with state diagrams shown in Figure 33–6 and Figure 33–7.	M	Yes [ ]
PSE5	Detection, classification and turn on timing.	33.2.3.1	In accordance with Table 33–5.	M	Yes [ ]
PSE6	Turn on power.	33.2.3.1	After valid detection in less than Tpon.	M	Yes [ ]
PSE7	Not apply power within Tpon.	33.2.3.1	Must initiate and successfully complete a new detection cycle before applying power.	M	Yes [ ]
PSE8	Alternative B backoff cycle.	33.2.3.1	Must wait no less than T_{dbo} as specified in Table 33–5 before attempting another detection.	M	Yes [ ]
PSE9	Backoff voltage.	33.2.3.1	Not greater than 2.8Vdc.	M	Yes [ ]
PSE10	Applying power.	33.2.4	Not until a PD requesting power has been successfully detected.	M	Yes [ ]
PSE11	Power pairs.	33.2.4	Power must be supplied on the same pairs as those used for detection.	M	Yes [ ]
PSE12	Detecting PDs.	33.2.5	Performed via the PSE PI.	M	Yes [ ]
PSE13	Open circuit voltage.	33.2.5	Item 1 in Table 33–2.	M	Yes [ ]
PSE14	Short circuit current.	33.2.5	Item 2 in Table 33–2.	M	Yes [ ]
PSE15	Backdriven current.	33.2.5	Not be damaged by up to 5mA over the range of Vport.	M	Yes [ ]
PSE16	Output capacitance.	33.2.5	Item 18 in Table 33–5.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE17	Exhibit Thevenin equivalence to one of the detection circuits in all detection states.	33.2.5	Figure 33–8 or Figure 33–9.	M	Yes [ ]
PSE18	V_{detect} with a valid PD signature connected.	33.2.5.1	Item 3 in Table 33–2.	M	Yes [ ]
PSE19	Two measurements with V_{detect}.	33.2.5.1	At least 1 V difference between consecutive measurements.	M	Yes [ ]
PSE20	Control slew rate when switching detection voltages.	33.2.5.1	Item 6 in Table 33–2.	M	Yes [ ]
PSE21	Polarity of $V_{detect.}$	33.2.5.1	Match polarity of V_{Port} defined in 33.2.1.	M	Yes [ ]
PSE22	Probe link to detect all PDs which present a valid signature.	33.2.6.1	(19KΩ to 26.5KΩ DC resistance) and (120nF capacitance or less) and (Voltage offset of up to 2.0 volts DC) and (Current offset of up to 12μA).	M	Yes [ ]
PSE23	Reject PDs that present an invalid signature.	33.2.6.2	(Less than 15 KΩ DC resistance) or (More than 33 KΩ DC resistance) or (More than 10μF capacitive load).	M	Yes [ ]
PSE24	Default classification.	33.2.7	Assign to Class 0 if PD cannot be classified as Class 1, 2, 3, or 4.	M	Yes [ ]
PSE25	Classification power levels	33.2.7.1	PDs classified as Class 4 will be treated as Class 0.	M	Yes [ ]
PSE26	Provide $V_{Class.}$	33.2.7.2	Between 15.5 and 20.5 volts, limited to 100 mA or less at the PI.	CL:M	Yes [ ] N/A [ ]
PSE27	Classification polarity	33.2.7.2	Same as V_{Port}.	CL:M	Yes [ ] N/A [ ]
PSE28	Classification timing	33.2.7.2	Item 20 in Table 33–5.	CL:M	Yes [ ] N/A [ ]
PSE29	Measure $I_{Class.}$	33.2.7.2	Classify PD according to Table 33–4.	CL:M	Yes [ ] N/A [ ]
PSE30	Classification default.	33.2.7.2	Assign PD to Class 0 if I_{class} is greater than or equal to 51mA.	CL:M	Yes [ ] N/A [ ]
PSE31	Power supply output.	33.2.8	Provide power to the PI according to Table 33–5, Figure 33–6, and Figure 33–7.	M	Yes [ ]
PSE32	Output Voltage	33.2.8.1	The specification for V_{Port} includes line and temperature variations.	M	Yes [ ]
PSE33	V_{Port} measurement.	33.2.8.1	Measured between any conductor of one power pair and any conductor of the other power pair.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE34	Load regulation.	33.2.8.2	Specified as 0.44W to 15.4W load step at a rate of change of 35mA/μs max.	M	Yes [ ]
PSE35	Voltage transients	33.2.8.2	Limited to 3.5V/μs max.	M	Yes [ ]
PSE36	Power feeding ripple and noise	33.2.8.3	Met for common-mode and/or pair-to-pair noise values for power outputs from 0.44W to 15.4W at operating V_{Port}.	M	Yes [ ]
PSE37	Maximum current at minimum voltage	33.2.8.4	For $V_{Port} > 44V$, the minimum value for I_{Port_max} in Table 33–5 shall be $15.4W/V_{Port}$	M	Yes [ ]
PSE38	AC current waveform parameters	33.2.8.4	I_{Peak} = 0.4A minimum for 50ms minimum and 5% duty cycle minimum. For $V_{Port} > 44V$, $I_{Peak} = 17.6W/V_{Port}$.	M	Yes [ ]
PSE39	Specifications for I_{Inrush} current	33.2.8.5	Meet conditions specified in 33.2.8.5 items a) through e).	M	Yes [ ]
PSE40	Overload current detection range	33.2.8.6	If $I_{port} > I_{CUT}$ for $T > T_{ovld}$ the PSE shall remove power. Item 8 in Table 33–5	M	Yes [ ]
PSE41	Overload time limit.	33.2.8.7	Item 9 in Table 33–5	M	Yes [ ]
PSE42	Short circuit current	33.2.8.8	Item 10 in Table 33–5.	M	Yes [ ]
PSE43	Short circuit time limit	33.2.8.9	Item 11 in Table 33–5.	M	Yes [ ]
PSE44	Turn off time	33.2.8.10	Applies to the discharge time from V_{Port} to 2.8Vdc with a test resistor of 320KΩ attached to the PI.	M	Yes [ ]
PSE45	Turn off voltage	33.2.8.11	Applies to the PI voltage in the IDLE State.	M	Yes [ ]
PSE46	Current unbalance	33.2.8.12	Item 15 in Table 33–5.	M	Yes [ ]
PSE47	Power turn on time	33.2.8.13	Item 16 in Table 33–5.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE48	Power provision.	33.2.9	Do not initiate if PSE is unable to provide maximum power level requested by PD based on PD's classification.	PA:M	Yes [ ] N/A [ ]
PSE49	Power allocation.	33.2.9	Not be based solely on historical data of power consumption of the attached PD.	PA:M	Yes [ ] N/A [ ]
PSE50	PSE AC MPS component requirements.	33.2.10.1.1	Meet requirements specified in item 1 and item 3 in Table 33–6	AC:M	Yes [ ] N/A [ ]
PSE51	PSE AC MPS component present.	33.2.10.1.1	Meets requirements specified in item 4a in Table 33–6.	AC:M	Yes [ ] N/A [ ]
PSE52	PSE AC MPS component absent.	33.2.10.1.1	Meets requirements specified in item 4b in Table 33–6.	AC:M	Yes [ ] N/A [ ]
PSE53	Power removal.	33.2.10.1.1	When AC MPS has been absent for a time duration greater than T_{PMDO}.	AC:M	Yes [ ] N/A [ ]
PSE54	PSE DC MPS component present.	33.2.10.1.2	Meet requirements specified in item 6 and item 7b in Table 33–5.	DC:M	Yes [ ] N/A [ ]
PSE55	PSE DC MPS component absent.	33.2.10.1.2	Meet requirements specified in item 6 in Table 33–5.	DC:M	Yes [ ] N/A [ ]
PSE56	Power removal.	33.2.10.1.2	When DC MPS has been absent for a time duration greater than T_{PMDO}.	DC:M	Yes [ ] N/A [ ]
PSE57	Not remove power.	33.2.10.1.2	When the DC current is greater than or equal to I_{Min2} max for at least T_{MPS} every $T_{MPS} + T_{MPDO}$, as defined in Table 33–5	DC:M	Yes [ ] N/A [ ]

33.7.3.3 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power.	33.3.1	On either set of PI conductors.	M	Yes [ ]
PD2	Polarity insensitive	33.3.1	Both Mode A and Mode B per Table 33–7.	M	Yes [ ]
PD3	Source power.	33.3.1	The PD will not source power on its PI.	M	Yes [ ]
PD4	Voltage tolerance.	33.3.1	Withstand 0V to 57V at the PI indefinitely without permanent damage.	M	Yes [ ]
PD5	PD behavior.	33.3.2	According to state diagram shown in Figure 33–13.	M	Yes [ ]
PD6	Valid detection signature.	33.3.3	Presented on each set of pairs defined in 33.3.1 if not powered via the PI.	M	Yes [ ]
PD7	Non-valid detection signature.	33.3.3	Presented on each set of pairs defined in 33.3.1 if not powered via the PI and will not accept power via the PI.	M	Yes [ ]
PD8	Non-valid detection signature.	33.3.3	When powered, present an invalid signature on the set of pairs not drawing power.	M	Yes [ ]
PD9	Valid detection signature.	33.3.3	Characteristics defined in Table 33–8.	M	Yes [ ]
PD10	Non-valid detection signature.	33.3.3	Exhibit one or both of the characteristics described in Table 33–9.	M	Yes [ ]
PD11	Return Class 0 to 3 classification.	33.3.4	Implement classification selection according to maximum power draw specified in Table 33–10.	PDCL:M	Yes [ ] N/A [ ]
PD12	Classification signature.	33.3.4	As defined in Table 33–11.	PDCL:M	Yes [ ] N/A [ ]
PD13	Classification signature.	33.3.4	One classification signature during classification.	PDCL:M	Yes [ ] N/A [ ]
PD14	PD power supply.	33.3.5	Operate within the characteristics in Table 33–12.	M	Yes [ ]
PD15	PD turn on voltage.	33.3.5.1	PD will turn on at a voltage less than V_{On}.	M	Yes [ ]
PD16	PD stay on voltage.	33.3.5.1	Must stay on for all voltages in the range of V_{Port}.	M	Yes [ ]
PD17	PD turn off voltage.	33.3.5.1	Must turn off at a voltage less than V_{Port} minimum and greater than V_{Off}.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD18	Input average power.	33.3.5.2	Applies for input power as specified in Table 33–12 averaged over one second.	M	Yes [ ]
PD19	Input inrush current.	33.3.5.3	Limited by the PD if C_{port} is greater than or equal to 180μF so that I_{Inrush} max is satisfied.	M	Yes [ ]
PD20	Peak operating current.	33.3.5.4	Not to exceed P_{Port} max/V_{Port} for more than 50ms max and 5% duty cycle max.	M	Yes [ ]
PD21	Peak current.	33.3.5.4	Not to exceed I_{Port} max.	M	Yes [ ]
PD22	RMS, DC, and ripple current.	33.3.5.4	Bounded by $Irms = [(Idc)^2 + (Iac)^2]^{1/2}$.	M	Yes [ ]
PD23	Maximum operating DC and RMS current.	33.3.5.4	Defined by the following equation: I_{Port_max} [mA] =12950/ V_{Port}.	M	Yes [ ]
PD24	PI capacitance during normal powering mode.	33.3.5.5	As specified in subclause 33.3.5.5.	M	Yes [ ]
PD25	Ripple and noise.	33.3.5.6	As specified in Table 33–12 for the common-mode and/or differential pair-to-pair noise at the PD PI.	M	Yes [ ]
PD26	Ripple and noise specification.	33.3.5.6	For all operating voltages in the range defined by Table 33–12 item 1.	M	Yes [ ]
PD27	Ripple and noise presence.	33.3.5.6	Must operate correctly when connected to a PSE generating ripple and noise levels specified in Table 33–5 item 3.	M	Yes [ ]
PD28	Power supply turn on/turn off voltages.	33.3.5.7	As specified in Table 33–12 when connected to a PSE through a 20Ω series resistor.	M	Yes [ ]
PD29	Startup oscillations	33.3.5.7	Shall turn on or off without startup oscillations and within the first trial at any load value.	M	Yes [ ]
PD30	Classification stability.	33.3.5.8	Classification signature will remain valid within T_{class} and remain valid for the duration of the classification period.	M	Yes [ ]
PD31	Backfeed voltage	33.3.5.10	Mode A and Mode B per 33.3.5.10.	M	Yes [ ]
PD32	Maintain power signature.	33.3.6	(current draw) and (AC impedance) defined in Table 33–13.	M	Yes [ ]
PD33	No longer require power.	33.3.6	Remove both components of the Maintain Power Signature.	M	Yes [ ]

33.7.3.4 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Electrical isolation	33.4.1	Electrical isolation will be in accordance with subclause 6.2 of IEC 60950-1:2001	M	Yes [ ]
EL2	Strength tests for electrical isolation.	33.4.1	Withstand at least one of the electrical strength tests specified in 33.4.1.	M	Yes [ ]
EL3	Isolation and grounding requirements.	33.4.1	Conductive link segments that have different requirements must have those requirements provided by the port-to-port isolation of the NID.	M	Yes [ ]
EL4	Environment A requirements for multiple instances of PSE and/or PD.	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated.	!MID:M	Yes [ ] N/A [ ]
EL5	Environment A requirement.	33.4.1.1.1	Switch more negative conductor.	M	Yes [ ]
EL6	Environment B requirements for multiple instances of PSE and/or PD.	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated.	M	Yes [ ]
EL7	Fault tolerance for PSEs and PDs encompassed within the MDI.	33.4.2	Meet requirements of the appropriate specifying clause.	!MID:M	Yes [ ] N/A [ ]
EL8	Fault tolerance for PSEs and PDs not encompassed within an MDI.	33.4.2	Meet the requirements of 33.4.2.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
EL9	Common-mode fault tolerance.	33.4.2	Each wire pair will withstand a 1000V common-mode impulse applied at Ecm of either polarity without damage.	M	Yes [ ]
EL10	The shape of the impulse for item common-mode fault tolerance.	33.4.2	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of the half value).	M	Yes [ ]
EL11	Impedance balance for transmit and receive pairs.	33.4.3	Exceed: - 29-17 log 10 (f/10)dB from 1.0 to 20MHz for 10Mb/s PHYs - 34-19.2 log 10 (f/50)dB from 1.0 to 100MHz for 100Mbits/s or greater PHYs.	M	Yes [ ]
EL12	Common-mode output voltage.	33.4.4	Magnitude while transmitting data and with power applied will not exceed 50mV peak when operating at 10Mbits/s and 50mV peak-to-peak when operating at 100Mbits/s or greater.	M	Yes [ ]
EL13	Common-mode AC voltage.	33.4.4	Magnitude at all other ports will not exceed 50mV peak-to-peak.	M	Yes [ ]
EL14	Frequency range for common-mode AC voltage measurement.	33.4.4	At all other ports will be from 1MHz to 100MHz.	M	Yes [ ]
EL15	Common-mode output voltage test configuration.	33.4.4	Must be performed with the PHY transmitting data and an operating PSE or PD and with the PSE load or PD source requirements specified in 33.4.4 items 1) or 2).	M	Yes [ ]
EL16	Noise from an operating PSE or PD to the differential transmit and receive pairs.	33.4.6	Will not exceed 10mV peak-to-peak measured from 1MHz to 100MHz.	M	Yes [ ]
EL17	Differential noise voltage test setup.	33.4.6	The PSE and PD shall be terminated as illustrated in Figure 33–16 and tested with the PSE and PD conditions as specified in 33.4.4.	M	Yes [ ]
EL18	Return loss requirements.	33.4.7	Specified in 14.3.1.3.4 for a 10Mb/s PHY, in ANSI X3.263:1995 for a 100Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY.	M	Yes [ ]

33.7.3.5 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	PSE electrical isolation.	33.4.1	Provided between port device circuits, frame ground and PI leads.	M	Yes [ ]
PSEEL2	Short circuit fault tolerance.	33.4.2	Any wire pair will withstand any short circuit to any other pair for an indefinite amount of time.	M	Yes [ ]
PSEEL3	Magnitude of short circuit current.	33.4.2	Not to exceed maximum value of I_{LIM}.	M	Yes [ ]
PSEEL4	Limitation of electromagnetic interference.	33.4.5	PSE will comply with applicable local and national codes.	M	Yes [ ]
PSEEL5	Insertion of Midspan at FD.	33.4.8	Comply with the guidelines specified in 33.4.8 items a) and b).	MID:M	Yes [ ] N/A [ ]
PSEEL6	Resulting “channel”.	33.4.8	Installation of a Midspan PSE will not increase the length to more than 100 meters as defined in ISO/IEC 11801.	MID:M	Yes [ ] N/A [ ]
PSEEL7	Configurations with Midspan PSE.	33.4.8	Must not alter transmission requirements of the “permanent link”.	MID:M	Yes [ ] N/A [ ]
PSEEL8	Midspan PSE insertion in the channel.	33.4.8	Must provide continuity for signal pairs.	MID:M	Yes [ ] N/A [ ]
PSEEL9	Midspan continuity in non-data pairs.	33.4.8	Will not provide DC continuity between the two sides of the segment for the pairs that inject power.	MID:M	Yes [ ] N/A [ ]
PSEEL10	Midspan PSE inserted as a “Connector” or “Telecom outlet.”	33.4.8.1	Meet transmission parameters NEXT, insertion loss and return loss.	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE NEXT.	33.4.8.1.1	$NEXT_{conn} \geq 40 - 20\log(f/100)$dB (equation 33–5) but not greater than 65dB from from 1MHz to 100MHz.	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE Insertion Loss.	33.4.8.1.2	$Insertion\_loss_{conn} \leq 0.04$ SQRT(f) dB [Equation (33–6)] but not less than 0.1dB from from 1MHz to 100MHz.	MID:M	Yes [ ] N/A [ ]
PSEEL13	Midspan PSE Return Loss.	33.4.8.1.3	$1MHz \leq f < 20MHz$: 23dB $20MHz \leq f \leq 100MHz$: 14 dB (Table 33–14) for transmit and receive pairs.	MID:M	Yes [ ] N/A [ ]
PSEEL14	Work area or equipment cable Midspan PSE.	33.4.8.1.4	Meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 for insertion loss, NEXT, and return loss for all transmit and receive pairs.	MID:M	Yes [ ] N/A [ ]

33.7.3.6 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD electrical isolation.	33.4.1	Provided between all external conductors, including frame ground, and all PI leads.	M	Yes [ ]
PDEL2	PD common-mode test requirement.	33.4.4	The PIs that require power shall be terminated as illustrated in Figure 33–16.	M	Yes [ ]

33.7.3.7 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety.	33.5.1	Conform to IEC publication 60950-1:2001.	M	Yes [ ]
ES2	Safety.	33.5.1	Comply with all applicable local and national codes.	M	Yes [ ]
ES3	Telephony voltages.	33.5.6	Application thereof described in 33.5.6 not result in any safety hazard.	M	Yes [ ]
ES4	Limitation of electromagnetic interference.	33.5.7	Comply with applicable local and national codes.	M	Yes [ ]

33.7.3.8 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety.	33.5.1	Limited Power Source in accordance with IEC publication 60950-1:2001.	M	Yes [ ]
PSEES2	Resistance unbalance.	33.5.5	As specified in IEC 11801 Edition 2 Clause 6.4.8 (reference: 3 percent).	M	Yes [ ]

33.7.3.9 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management capability.	33.6	Access via MII, GMII, or equivalent.	MAN:M	Yes [ ] N/A [ ]
MF2	PSE registers.	33.6.1	Register address 11 for control functions and register address 12 for status functions.	MAN:M	Yes [ ] N/A [ ]
MF3	Register bits latching high (LH).	33.6.1	Remain high until read via the management interface.	MAN:M	Yes [ ] N/A [ ]
MF4	Register bits read.	33.6.1	Bit assumes a value based on the current state of the condition it monitors.	MAN:M	Yes [ ] N/A [ ]
MF5	PSE Control register reserved bits (11.15:4).	33.6.1.1.1	Not affected by writes and return a value of zero when read.	MAN:M	Yes [ ] N/A [ ]
MF6	Pair Control Ability not supported.	33.6.1.1.2	Ignore writes to bits 11.3:2.	MAN∗ !PCA:M	Yes [ ] N/A [ ]
MF7	Writes to 11.3:2 when Pair Control Ability not supported.	33.6.1.1.2	Return the value that reports the supported PSE Pinout Alternative.	MAN∗ !PCA:M	Yes [ ] N/A [ ]
MF8	Bits 11.3:2 set to '01'.	33.6.1.1.2	Forces the PSE to use Alternative A.	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF9	Bits 11.3:2 set to '10'.	33.6.1.1.2	Forces the PSE to use Alternative B.	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF10	Pair control ability bit, (12.0).	33.6.1.1.2	A value of ‘1’ sets the mr_pse_alternative variable.	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF11	PSE function disabled	33.6.1.1.3	Setting PSE Enable bits 11.1:0 to a logic ‘00’, also the MDI shall function as it would if it had no PSE function.	MAN:M	Yes [ ] N/A [ ]
MF12	PSE function enabled.	33.6.1.1.3	Setting PSE Enable bits 11.1:0 to a logic ‘01’.	MAN:M	Yes [ ] N/A [ ]
MF13	PSE enable bits (11.1:0).	33.6.1.1.3	Writing to these register bits shall set mr_pse_enable to the corresponding value: 00 = disable, 01 = enable and 10 = force power.	MAN:M	Yes [ ] N/A [ ]
MF14	Reserved bits (12.15:13).	33.6.1.2.1	Not affected by writes and shall return a value of zero when read.	MAN:M	Yes [ ] N/A [ ]
MF15	Power denied bit (12.12).	33.6.1.2.2	A value of ‘1’ indicates power has been denied.	MAN:M	Yes [ ] N/A [ ]
MF16	Power denied bit implementation.	33.6.1.2.2	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MF17	Valid signature bit (12.11).	33.6.1.2.3	Logic ‘1’ indicates a valid signature has been detected.	MAN:M	Yes [ ] N/A [ ]
MF18	Valid signature bit implementation.	33.6.1.2.3	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]
MF19	Invalid signature bit (12.10).	33.6.1.2.4	Logic ‘1’ indicates an invalid signature has been detected.	MAN:M	Yes [ ] N/A [ ]
MF20	Invalid signature bit implementation.	33.6.1.2.4	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]
MF21	Short circuit bit (12.9).	33.6.1.2.5	Logic ‘1’ indicates a short circuit condition has been detected.	MAN:M	Yes [ ] N/A [ ]
MF22	Short circuit bit implementation.	33.6.1.2.5	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]
MF23	Overload bit (12.8).	33.6.1.2.6	Set to ‘1’ when PSE state diagram enters the state ‘ERROR_DELAY_OVER’.	MAN:M	Yes [ ] N/A [ ]
MF24	Overload bit implementation.	33.6.1.2.6	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]
MF25	MPS absent bit (12.7).	33.6.1.2.7	Read as logic 1 indicates either or both elements of the MPS is absent for a duration greater than T_{MPDO} as specified in 33.2.10.	MAN:M	Yes [ ] N/A [ ]
MF26	MPS Absent bit implementation.	33.6.1.2.7	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]

Annex 33A

(informative)

PSE Detection of PDs

The capacitance of the maximum cabling plant and maximum PD signature is included in the PSE detection requirement.

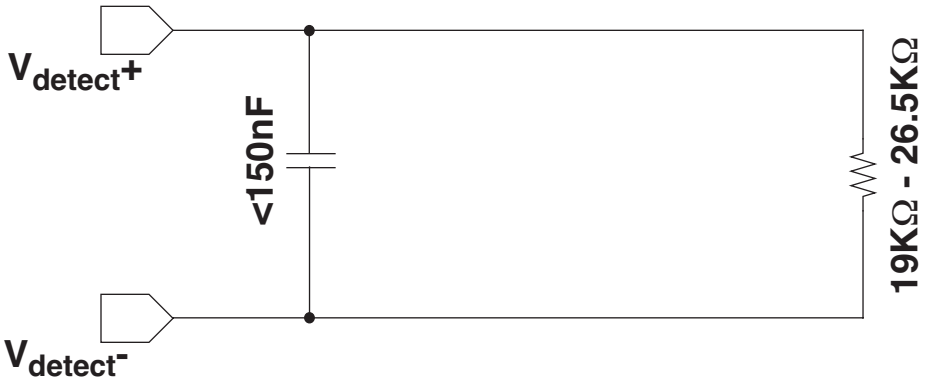


Figure 33A.1—PD detection signature

PDs contain an autopolarity circuit that may result in a DC offset in the signature, as illustrated in Figure 33A.2.

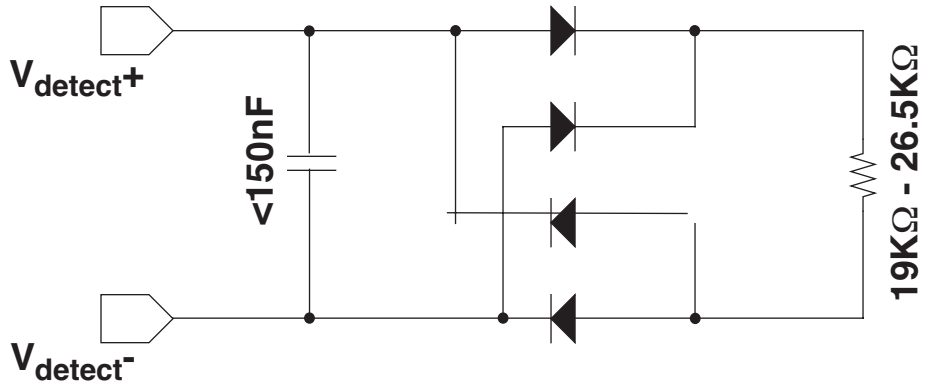


Figure 33A.2—PD detection signature with polarity guard

The circuits in Figure 33A.3, Figure 33A.4, and Figure 33A.5 are recommended as test benchmarks for rejection by a compliant PSE.

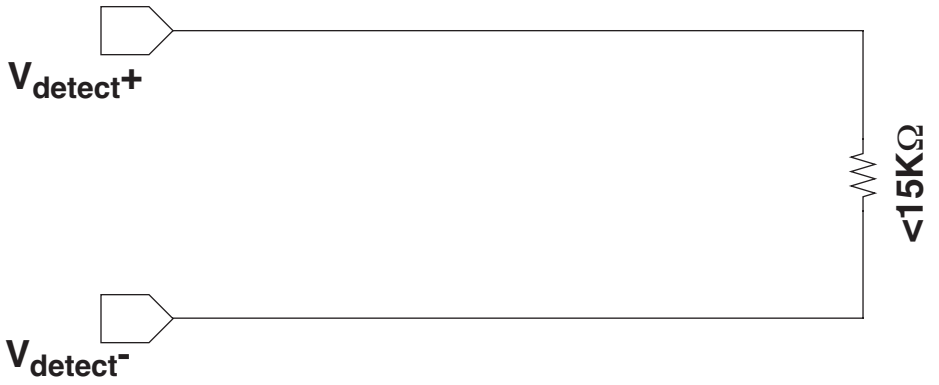


Figure 33A.3—Invalid detection signature, impedance low

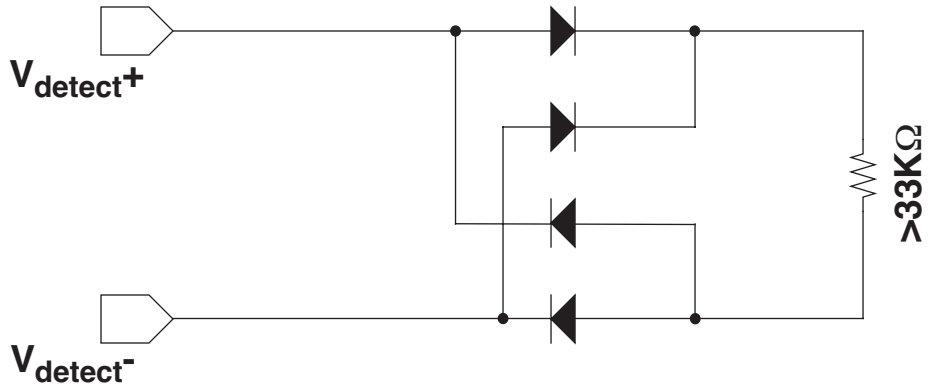


Figure 33A.4—Invalid detection signature, impedance high

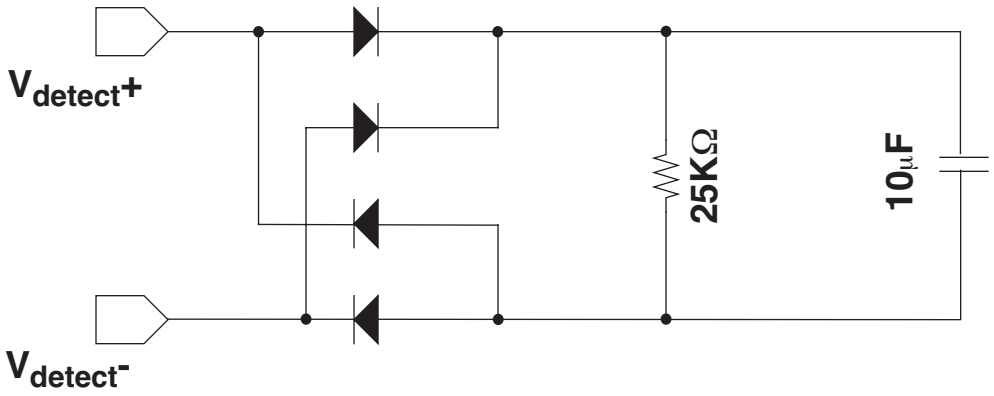


Figure 33A.5—Invalid detection signature, capacitance high

The circuit in Figure 33A.6 is an example of the presentation of a classification signature by a PD.

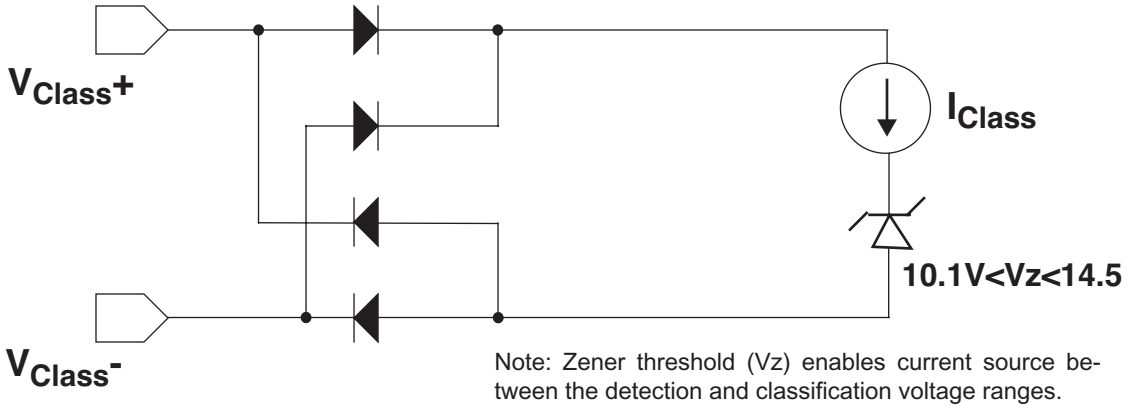


Figure 33A.6—PD classification signature

Annex 33B

(informative)

Cabling guidelines

DTE power via MDI is intended to operate over a 100 Ω balanced cabling infrastructure as described in ISO/IEC 11801-2000. Although initial implementations are expected to make use of Clause 33 to provide powered IP telephones and wireless access points, Clause 33 is intended to address a much larger family of low power devices whose applications require connection to local area networks.

It is expected that in the future as building cabling infrastructures begin to support more building automation systems (BAS), additional cabling guidelines will be implemented. BAS systems are used for controlling building systems such as fire alarm, security, and access control (e.g., closed circuit television), and energy management systems (e.g., heating, ventilation, and air conditioning, and lighting control). One such standard that is to be published to support these systems with a cabling infrastructure in EIA/TIA is the Building Automation Cabling Standard for Commercial Buildings. This standard will specify a generic cabling system for building automation systems used in commercial buildings for a multi-product, multi-vendor environment. The purpose of the standard is to enable the planning and installation of a structured cabling system for building automation system applications that are required for use in new or renovated construction of commercial buildings. It is significantly less expensive to integrate all of the major voice, data, and BAS applications by utilizing a fully-integrated structured cabling infrastructure.

For planning purposes, a sufficient number of horizontal cabling links should be provided for voice, data, and building automation services over the average floor space. It is recommended that a minimum of two outlets be provided per work area as specified in the current standards in ISO/IEC.

Annex 33C

(informative)

Recommended test configurations and procedures

The test figures in this annex are intended to illustrate recommended testing procedures for verifying compliance with Clause 33. In each case, a behavioral circuit is shown along with one possible schematic to implement a test circuit. Other test circuits are possible, as long as compliance with the Clause 33 requirements are adequately demonstrated.

In each PSE Test Configuration of this annex, the terminals a, b, c, and d correspond to PI pin assignments according to Table 33C.1.

Table 33C.1—PSE PI pin assignments for PSE Test Configurations

Terminal	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
a	3	1	4
b	6	2	5
c	1	3	7
d	2	6	8

In each PD Test Configuration of this annex, the terminals a, b, c, and d correspond to PI pin assignments according to Table 33C.2.

Table 33C.2—PD PI pin assignments for PD Test Configurations

Terminal	Mode A (MDI)	Mode A (MDI-X)	Mode B (All)
a	3	1,3	4
b	6	2,6	5
c	1	3,1	7
d	2	6,2	8

33C.1 Recommended PSE output test procedures

33C.1.1 Test Procedure PSE-1 (output polarity, output voltage, and continuous output power)

Test Procedure PSE-1 is used for testing the following:

a) Output voltage polarity (Table 33–1)
b) V_{Port} (Table 33–5, item 1)
c) I_{Port_max} (Table 33–5, item 4, 33.2.8.4)
d) P_{Port} (Table 33–5, item 14)

Test Procedure PSE-1 uses Test Configuration PSE-A as shown in Figure 33C.1. In this test configuration, terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

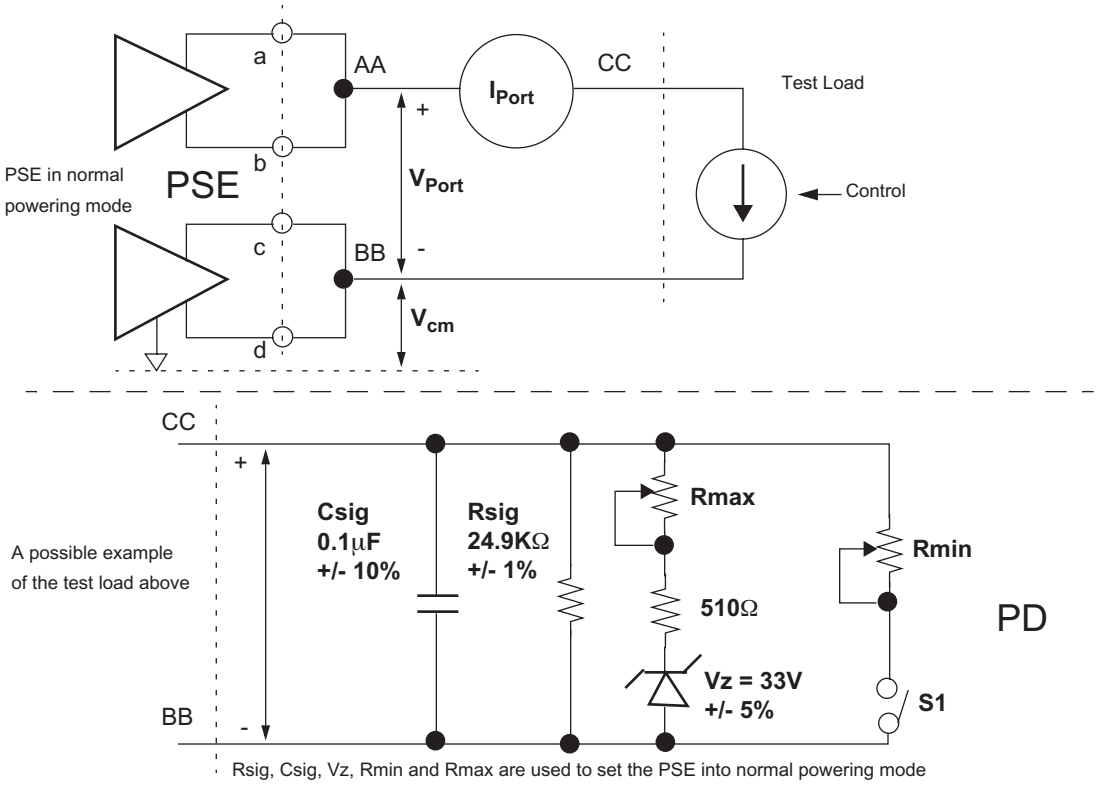


Figure 33C.1—Test configuration PSE-A

Test Procedure PSE-1 is as follows:

1) Wait 1 second minimum and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Wait 1 second minimum and measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.

33C.1.2 Test Procedure PSE-2 (load regulation)

Test Procedure PSE-2 is used for testing load regulation, i.e., voltage transients during load changes (Table 33–5, item 2).

Test Procedure PSE-2 uses Test Configuration PSE-B as shown in Figure 33C.2. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

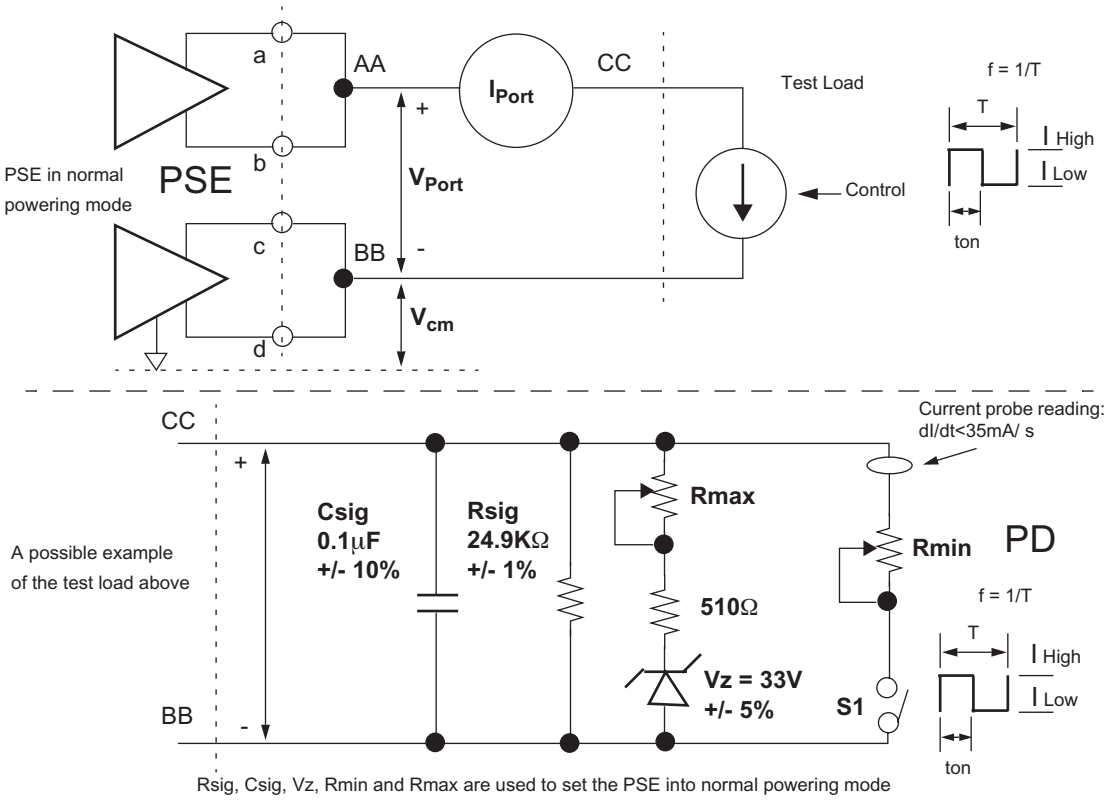


Figure 33C.2—Test configuration PSE-B

Test Procedure PSE-2 is as follows:

1) Wait 1 second minimum and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Wait 1 second minimum and measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.
3) Change load from Rmax to Rmin and from Rmin to Rmax at f = 10Hz,
   for a 30% to 70% duty cycle, while monitoring V_{Port}.

33C.1.3 Test Procedure PSE-3 (ripple and noise)

Test Procedure PSE-3 is used for testing ripple and noise (Table 33–5, item 3), 33.4.5 and 33.4.6.

Test Procedure PSE-3 uses Test Configuration PSE-A as shown in Figure 33C.1. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

Test Procedure PSE-3 is as follows:

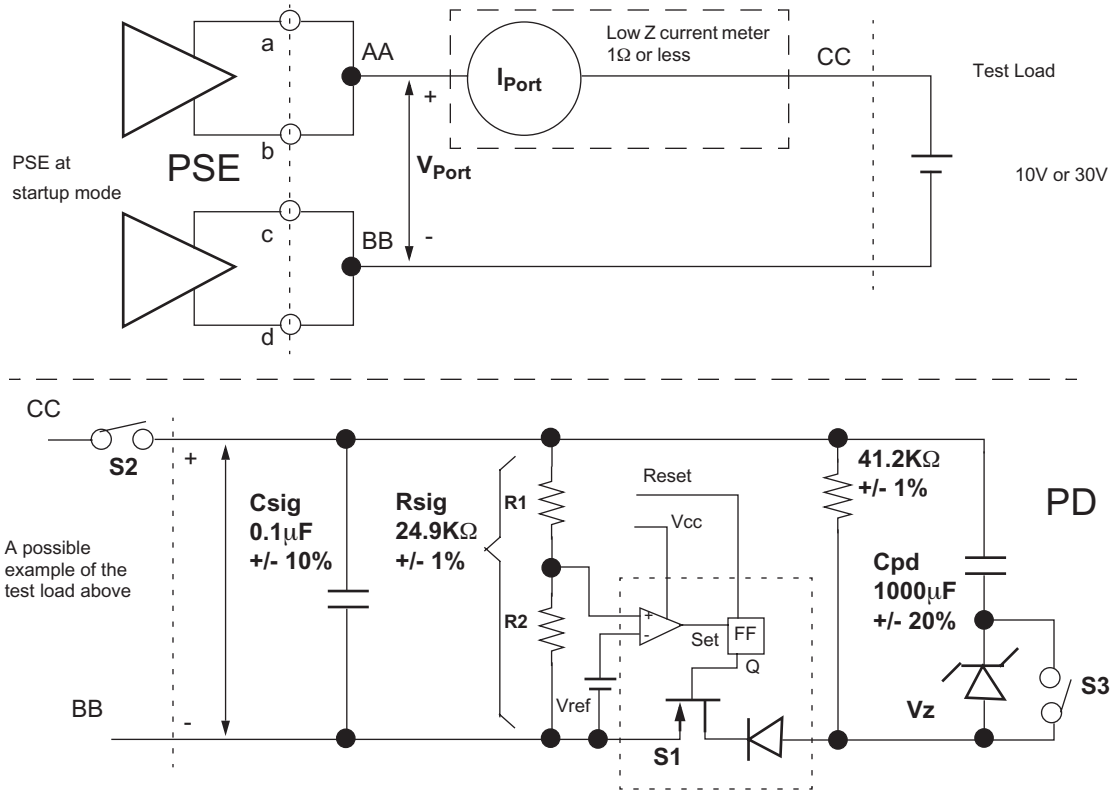
1) Wait 1 second minimum and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Wait 1 second minimum and measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.
3) Measure V_{Port} ac noise and ripple at Rmax (S1 open) and at Rmin (S1 closed) by using spectrum analyzer or equivalent equipment.

33C.1.4 Test Procedure PSE-4 (output current in startup mode)

Test Procedure PSE-4 is used for testing the following:

a) I_{Inrush} (Table 33–5, item 5) and
b) T_{LIM} (Table 33–5, item 11).

Test Procedure PSE-4 uses Test Configuration PSE-C as shown in Figure 33C.3. In this test configuration, terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.



Example test setup principles:

1. The function of S1 is to connect a large capacitive load when the port voltage is either 0V or 42V.
2. S1 is to allow the transition from OFF to ON in less than 50μs.
3. The capacitive load value is chosen to emulate a short-circuit condition for more than 75ms.
4. The test can be repeated only if the capacitive load is discharged and S1 is reset.

Figure 33C.3—Test configuration PSE-C

Test Procedure PSE-4 is as follows:

1) Wait 1 second minimum and measure V_{Port}.
2) Set Vz to 30V.
3) Verify that I_{Port} is within limits shown in Figure 33C.4.
4) Discharge capacitive load and reset S1.
5) Set Vz to 10V.
6) Verify that $I_{Port} > 60mA$.

NOTE—Test setup (as for any other test setup in Annex 33) may be modified in order to reflect different PSE implementations in order to be able to test according to the results expected per Figure 33C.4.

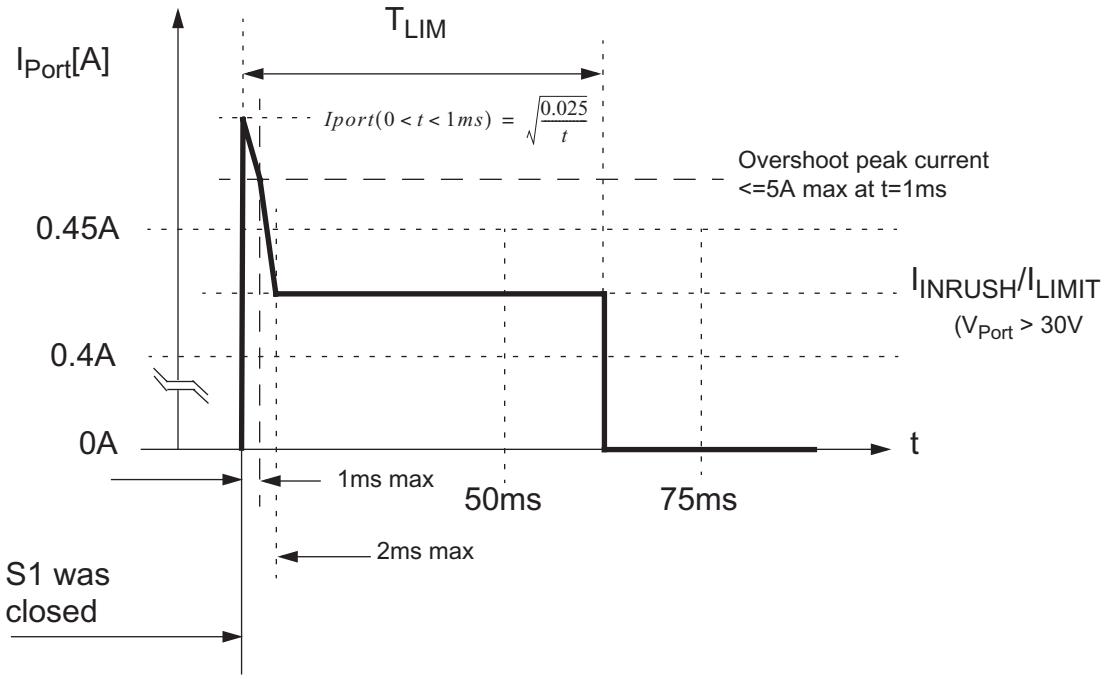


Figure 33C.4—I_{Port} current and timing limits in startup and short-circuit conditions

33C.1.5 Test Procedure PSE-5 (IDLE state current)

Test Procedure PSE-5 is used for testing the following:

a) I_{Min1} (Table 33–5, item 6a) and
b) T_{PMDO} (Table 33–5, item 7a),

when monitoring the DC MPS component (33.2.10.1.2).

Test Procedure PSE-5 uses Test Configuration PSE-D as shown in Figure 33C.5. In this test configuration, terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

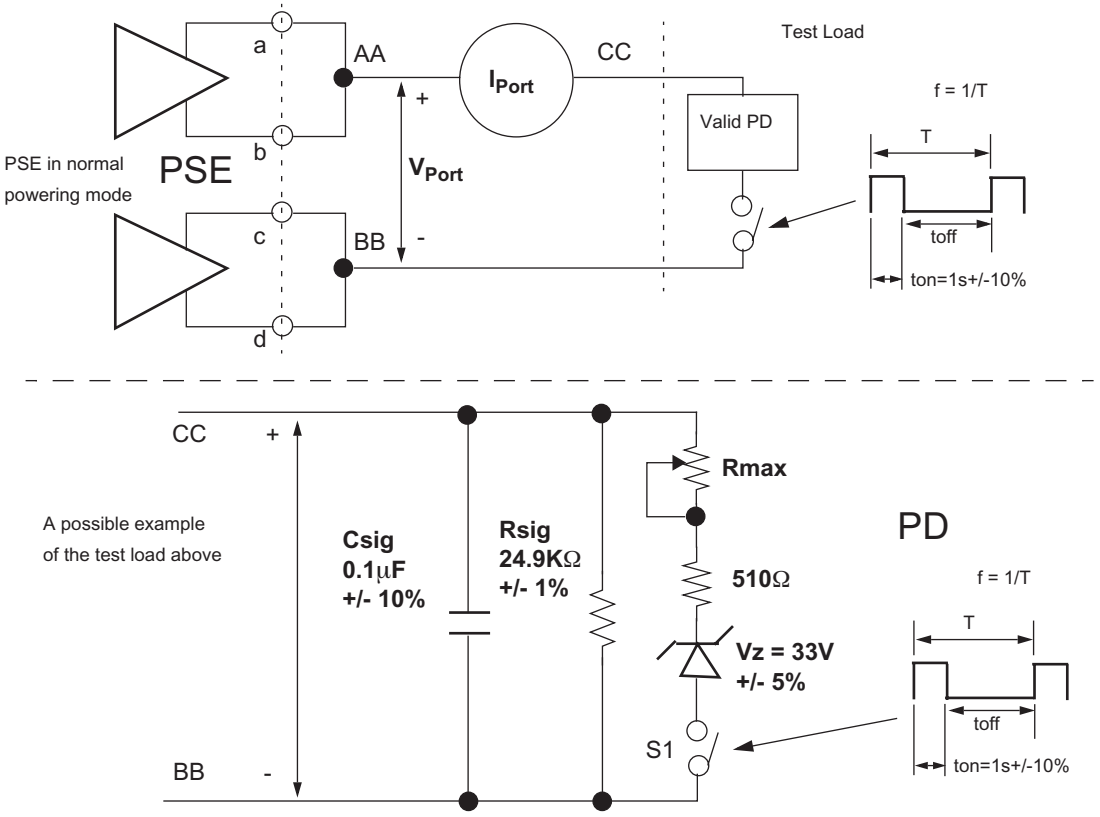


Figure 33C.5—Test configuration PSE-D

Test Procedure PSE-5 is as follows:

1) Wait 1 second minimum and measure V_{Port} at Rmax (S1 closed).
   Verify that 44V <= V_{Port} <= 57V.
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Increase Rmax and verify that the power is removed from the port.
3) Repeat step 1.
4) Increase toff from 0 to 400ms and verify that V_{Port} is stable and within its initial value for toff <= 300ms.
5) Verify that V_{Port} was removed for toff = 400ms from the time that S1 was opened.

33C.1.6 Test Procedure PSE-6 (overload current detection range and overload timings)

Test Procedure PSE-6 is used for testing the following:

a) I_{CUT} (Table 33–5, item 8) and
b) T_{ovld} (Table 33–5, item 9).

Test Procedure PSE-6 uses Test Configuration PSE-B as shown in Figure 33C.2. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

Test Procedure PSE-6 is as follows:

1) Set Rmax (S1 open) and Rmin (S1 closed).
   (Rmax is adjusted to generate I_{Port} min = 10mA.)
   Verify that 44V <= V_{Port} <= 57V.
2) Close S1. Decrease Rmin slowly until power is removed from the port and note the actual value of I_{CUT}.
3) Verify that (15.4/V_{Port}) < I_{CUT} < 400mA.
4) Repeat step 1.
   Adjust S1 control to: I_{Port} > I_{CUT}. S1 on time: 50.0 ms.
   Verify that power is not removed from the port.
   Adjust S1 control to: I_{Port} > I_{CUT}. S1 on time: 75.0 ms.
   Verify that power is removed from the port.

The relationships between overload detections and timings are shown in Figure 33C.6.

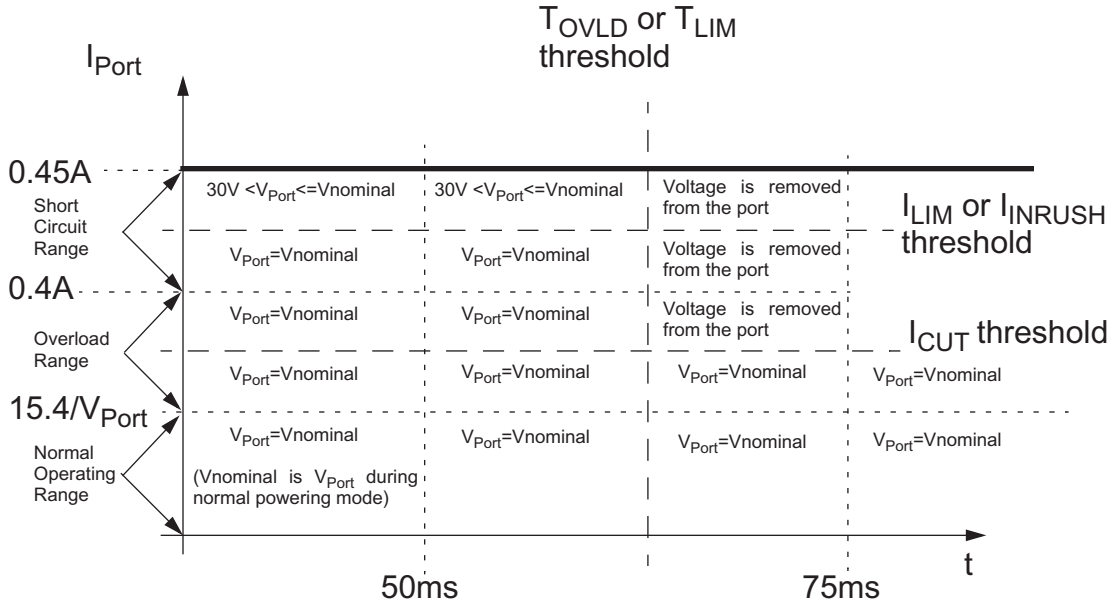


Figure 33C.6—Port voltage requirements during normal powering mode, overload and short-circuit conditions, as functions of I_{Port} current and time duration

33C.1.7 Test Procedure PSE-7 (short circuit current and timing)

Test Procedure PSE-7 is used for testing the following:

a) I_{LIM} (Table 33–5, item 10) and
b) T_{LIM} (Table 33–5, item 11).

Test Procedure PSE-7 uses Test Configuration PSE-E as shown in Figure 33C.7. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

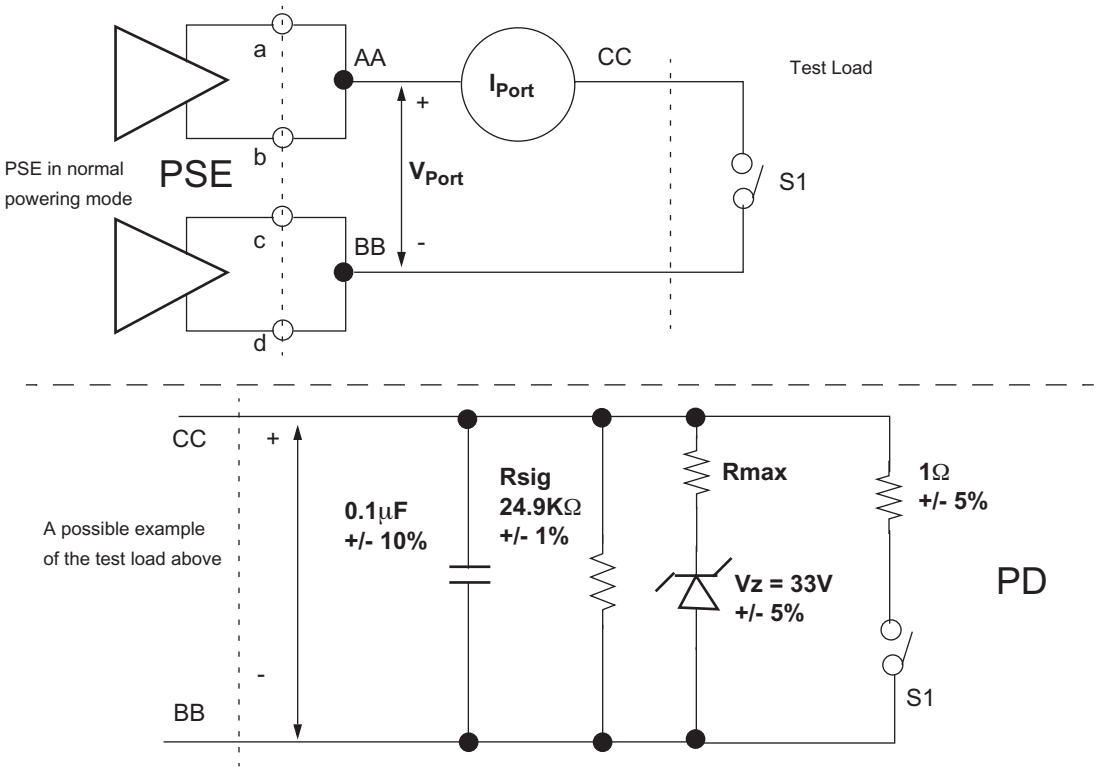


Figure 33C.7—Test configuration PSE-E

Test Procedure PSE-7 is as follows:

1) Wait 1 second minimum and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
   Verify that 44V < V_{Port} < 57V.
2) Close S1 and observe I_{Port} .
3) Verify that I_{Port} is within limits shown in Figure 33C.4.

33C.1.8 Test Procedure PSE-8 (turn on rise time)

Test Procedure PSE-8 is used for testing T_{Rise} (Table 33–5, item 12).

Test Procedure PSE-8 uses Test Configuration PSE-A as shown in Figure 33C.1. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

Test Procedure PSE-8 is as follows:

1) Measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
   Measure rise time from 10% of V_{Port} to 90% of V_{Port}.
   See Figure 33C.11.
2) Measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.
   Measure rise time from 10% of V_{Port} to 90% of V_{Port}.
   See Figure 33C.11.

33C.1.9 Test Procedure PSE-9 (turn off time)

Test Procedure PSE-9 is used for testing T_{Off} (Table 33–5, item 13a).

Test Procedure PSE-9 uses Test Configuration PSE-F as shown in Figure 33C.8. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

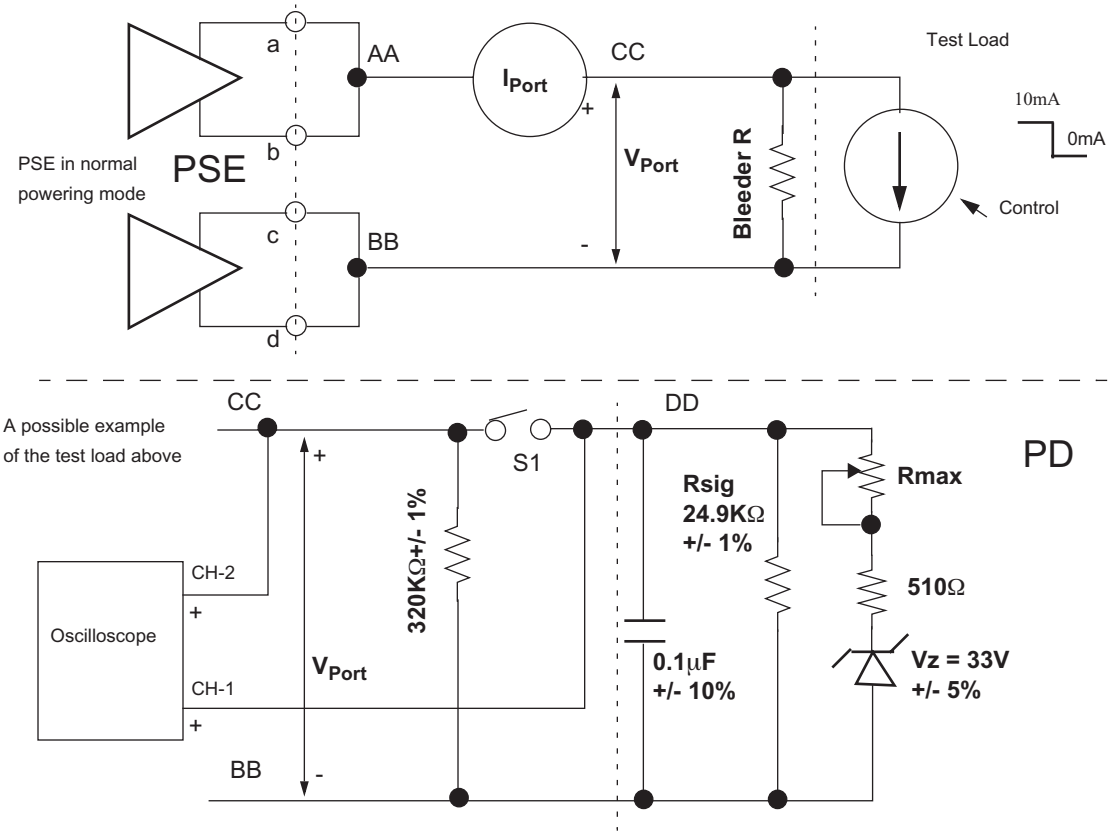


Figure 33C.8—Test configuration PSE-F

Test Procedure PSE-9 is as follows:

1) Measure V_{Port} at Rmax (S1 closed).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Monitor V_{Port} at PSE side (CC) and at PD side (DD).
   Disconnect PD load by turning off S1 at T_0.

Use CH-1 as the trigger signal for measuring the timings.
Verify that V_{Port} has not changed during the first 300 ms (T_1) from T_0.
Verify that power is removed from the port within 400 ms (T_2) from T_0.
Verify that V_{Port} is less than 2.8Vdc within 500 ms max from tx.
The turn off timing relationships are illustrated in Figure 33C.9.

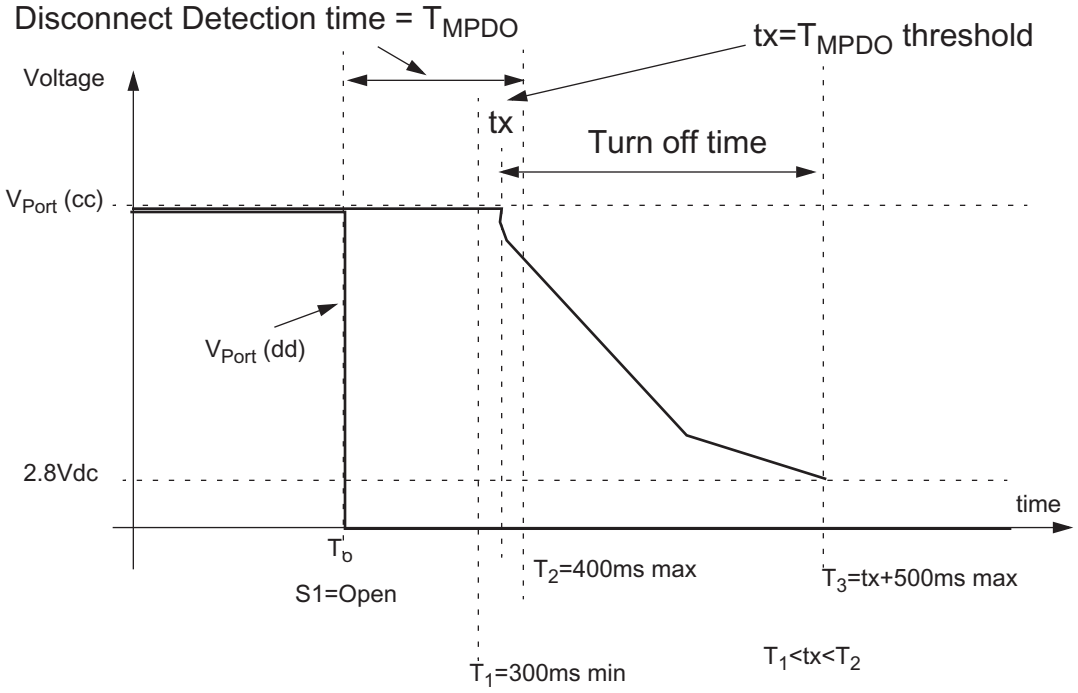


Figure 33C.9—Turn off timing relationships

33C.1.10 Test Procedure PSE-10 (turn on, detection and classification time)

Test Procedure PSE-10 is used for testing the following:

a) T_{pon} (Table 33–5, item 16),
b) T_{det} (Table 33–5, item 19), and
c) T_{pdc} (Table 33–5, item 20).

Test Procedure PSE-10 uses Test Configuration PSE-F1 as shown in Figure 33C.10. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

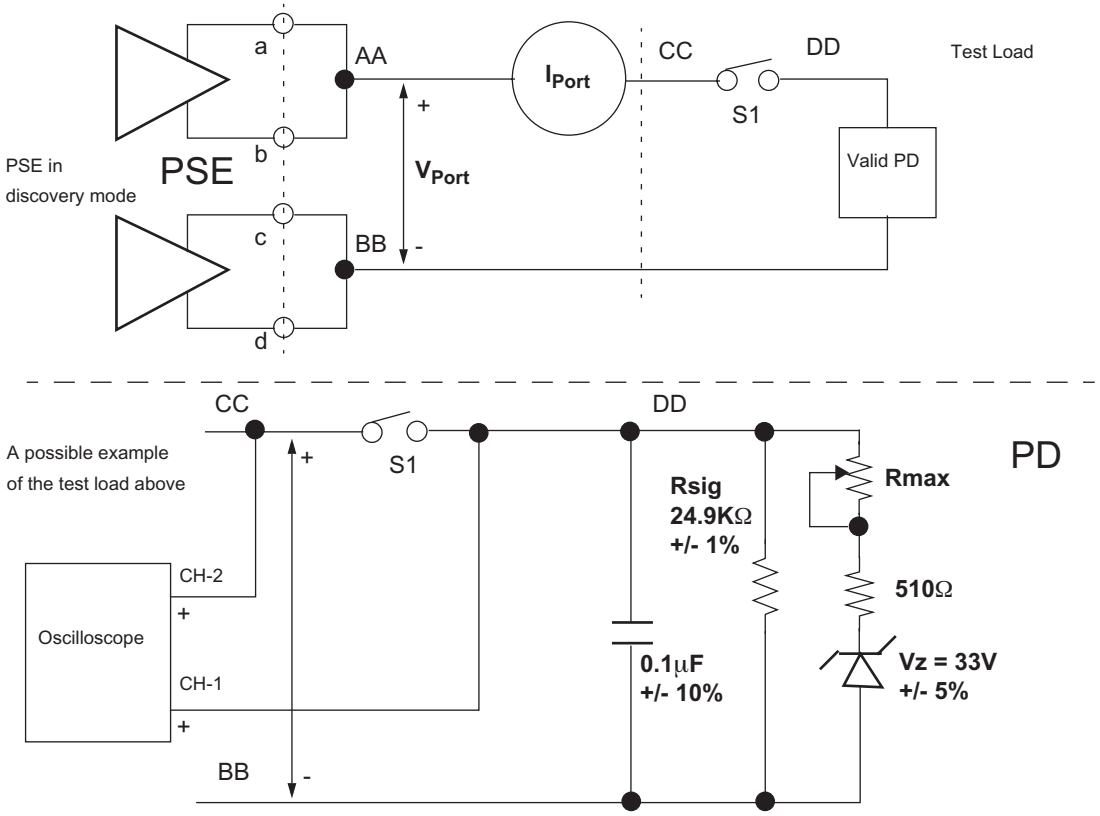


Figure 33C.10—Test configuration PSE-F1

Test Procedure PSE-10 is as follows:

1) Wait 1 second minimum and measure V_{Port} at Rmax (S1 closed).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Open S1. Repeat step 1 and monitor the events vs. timings as illustrated in Figure 33C.11.

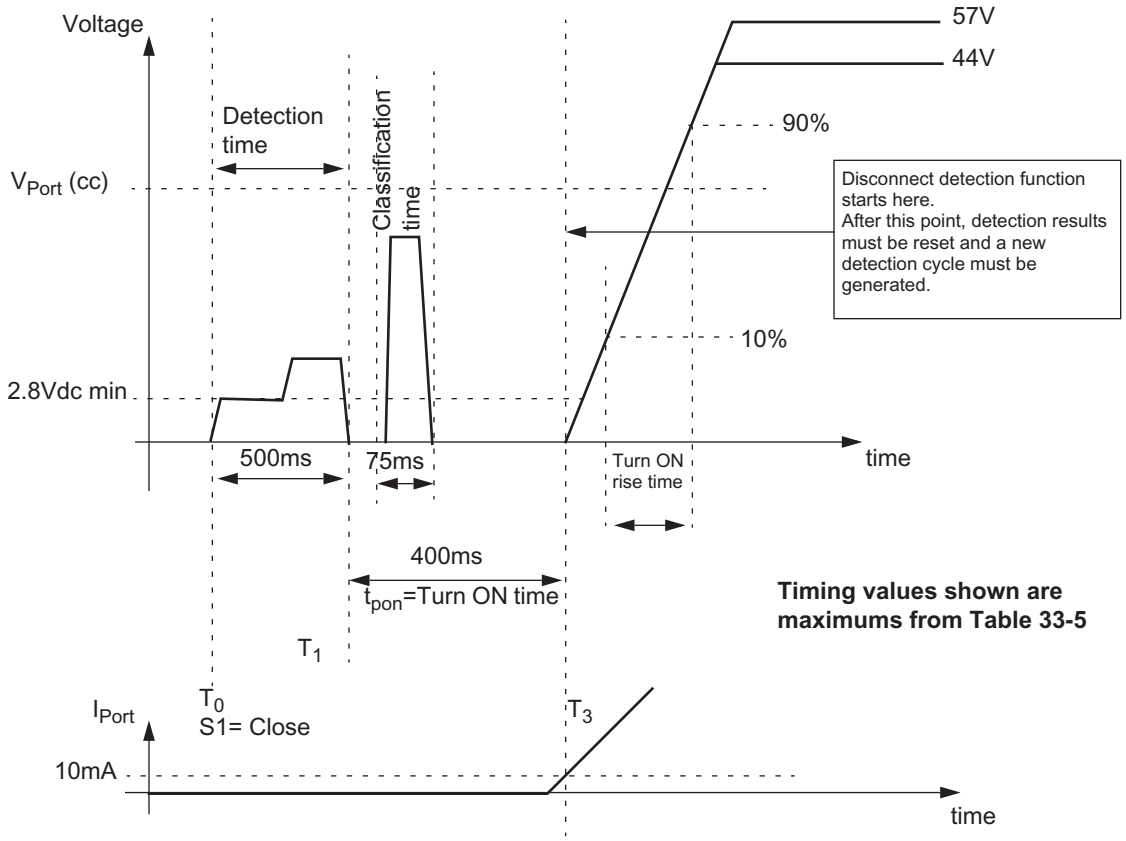


Figure 33C.11—Detection, classification, turn on, and total cycle timing relationships

33C.1.11 Test Procedure PSE-11 (detection backoff time)

Test Procedure PSE-11 is used for testing T_{dbo} (Table 33–5, item 17) for a PSE that performs Alternative B as specified in 33.2.3.1 and R_{open} (Table 33–2, item 9).

Test Procedure PSE-11 uses Test Configuration PSE-G as shown in Figure 33C.12. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

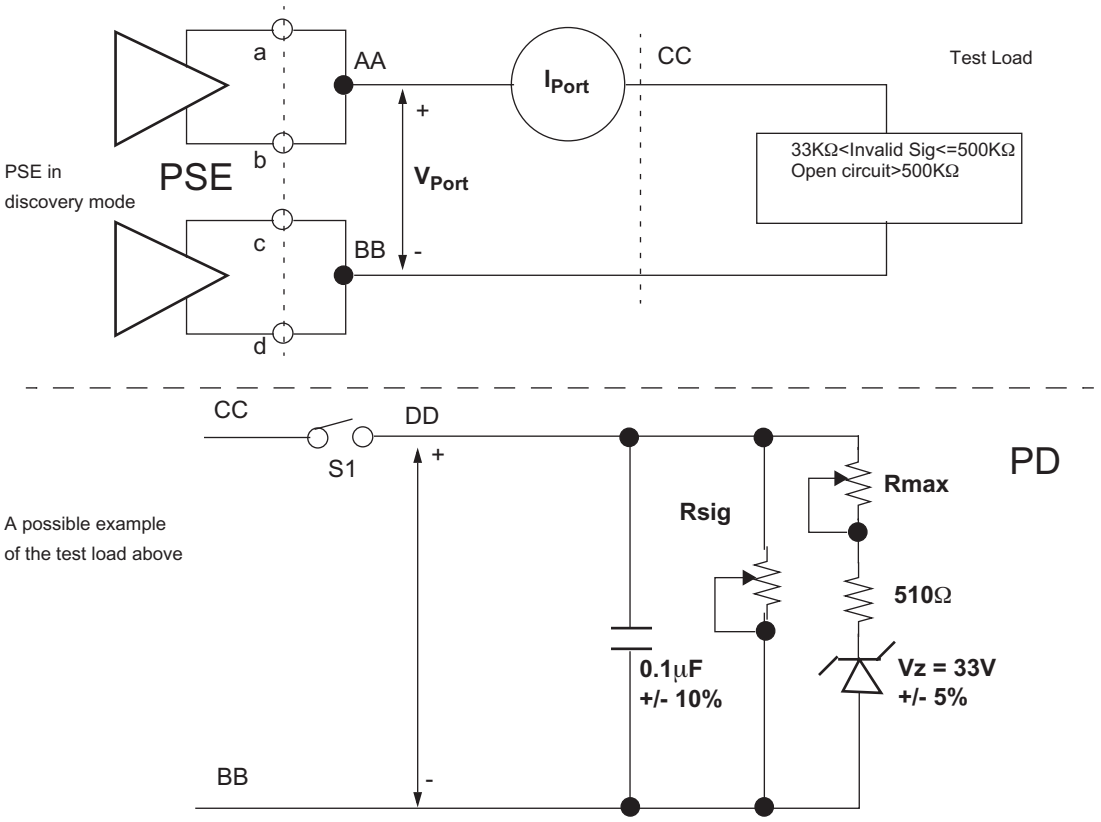


Figure 33C.12—Test configuration PSE-G

Test Procedure PSE-11 is as follows:

1) Set Rsig to 24.9KΩ+/-1%. Close S1.
   Measure V_{Port} at Rmax.
   Rmax is adjusted to generate I_{Port} min = 10mA at V_{Port} .
2) Open S1.
   Adjust Rsig=34KΩ+/-1%.
   Close S1.
   Verify that V_{Port} is less than 2.8V for 2 second minimum after the detection sequence has been completed.
3) Open S1.
   Adjust Rsig=510KΩ+/-1%.
   Close S1.
   Verify that V_{Port} voltages and timings are as defined in Figure 33C.11.

33C.1.12 Test Procedure PSE-12 (port capacitance during detection)

Test Procedure PSE-12 is used for testing C_{out} (Table 33–5, item 18).

Test Procedure PSE-12 uses Test Configuration PSE-H as shown in Figure 33C.13. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

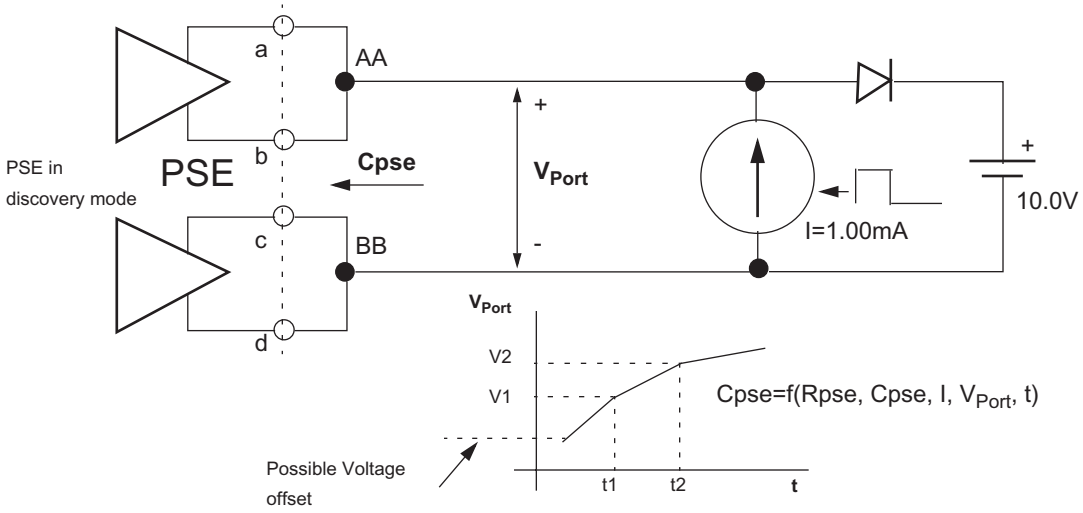


Figure 33C.13—Test configuration PSE-H

Test Procedure PSE-12 is as follows:

1) Set PSE port to IDLE state.
   Connect switched current source, I, to the PSE port.
   The current source voltage is clamped to 10V.
   Calculate port capacitance (Cpse) by measuring Rpse (port resistance) and using it in a typical differential equation solution.

33C.2 Recommended PSE AC disconnect-detection test procedures

33C.2.1 Test Procedure PSE-13 (ac disconnect pulse parameters)

Test Procedure PSE-13 is used for testing the following:

a) $V_{\_close}$ (Table 33–6, item 3a),
b) $V_{\_open}$ (Table 33–6, item 1a),
c) F_p (Table 33–6, item 1b),
d) SR (Table 33–6, item 1c),
e) T_{PMDO} (Table 33–6, item 3c) when monitoring the AC MPS component (33.2.10.1),
f) V_{Port} (Table 33–6, item 3b), and
g) Z_{ac1} and Z_{ac2} (Table 33–6, item 4a and item 4b).

Test Procedure PSE-13 uses Test Configuration PSE-I as shown in Figure 33C.14. In this test configuration, terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

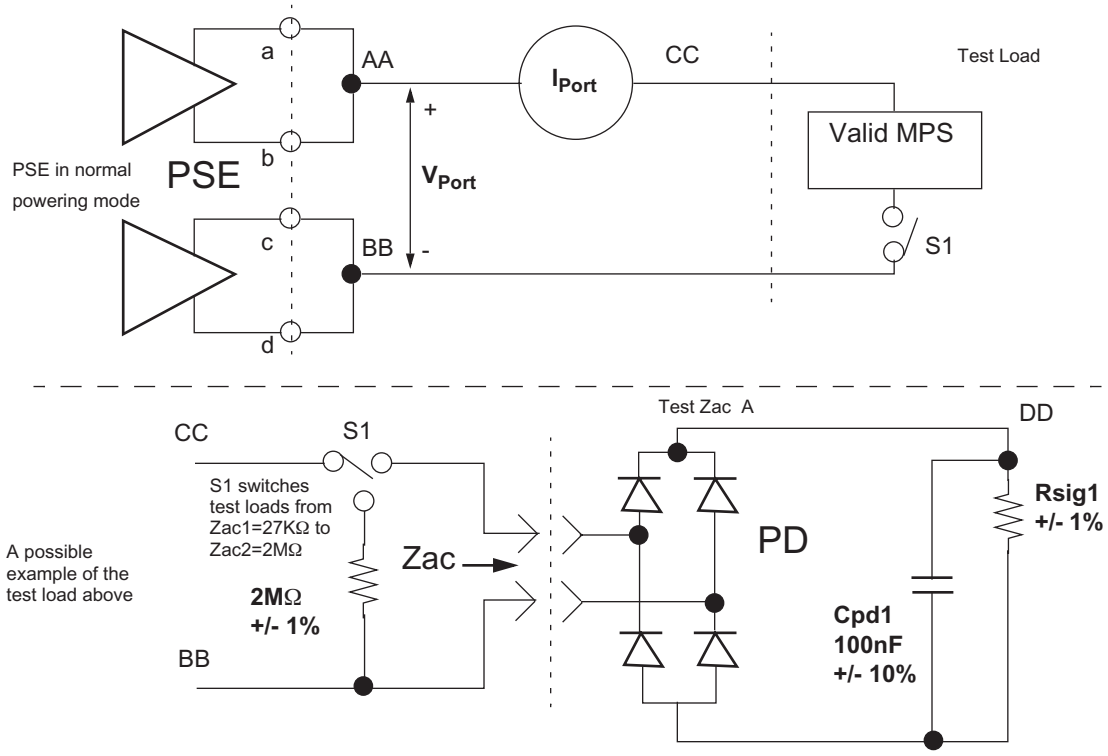


Figure 33C.14—Test configuration PSE-I

Test Procedure PSE-13 is as follows:

1) Set Rsig1 value to have total of Zac = 27KΩ.
   Measure V_{Port} and verify that V_{Port} is within the normal operating voltage range.
   Verify that the ac ripple voltage is less than 0.5Vpp.
   This requirement should be verified with test Zac "A".
2) Monitor V_{Port} at the PSE side (CC) and at the PD side (DD).
3) Disconnect PD by turning off S1 at T_o.
   Use S1 opening as the trigger signal for measuring the timings.
4) Verify that power is not removed during the first 300ms (T_1) from T_o.
5) Verify that power is removed from the port within 400ms (T_2) max from T_o.
6) Measure $V_{\_open}$, F_p and SR. Refer to Figure 33C.15.
7) Steps 1 through 6 should be conducted for both test Zac configurations as indicated in Figure 33C.14.

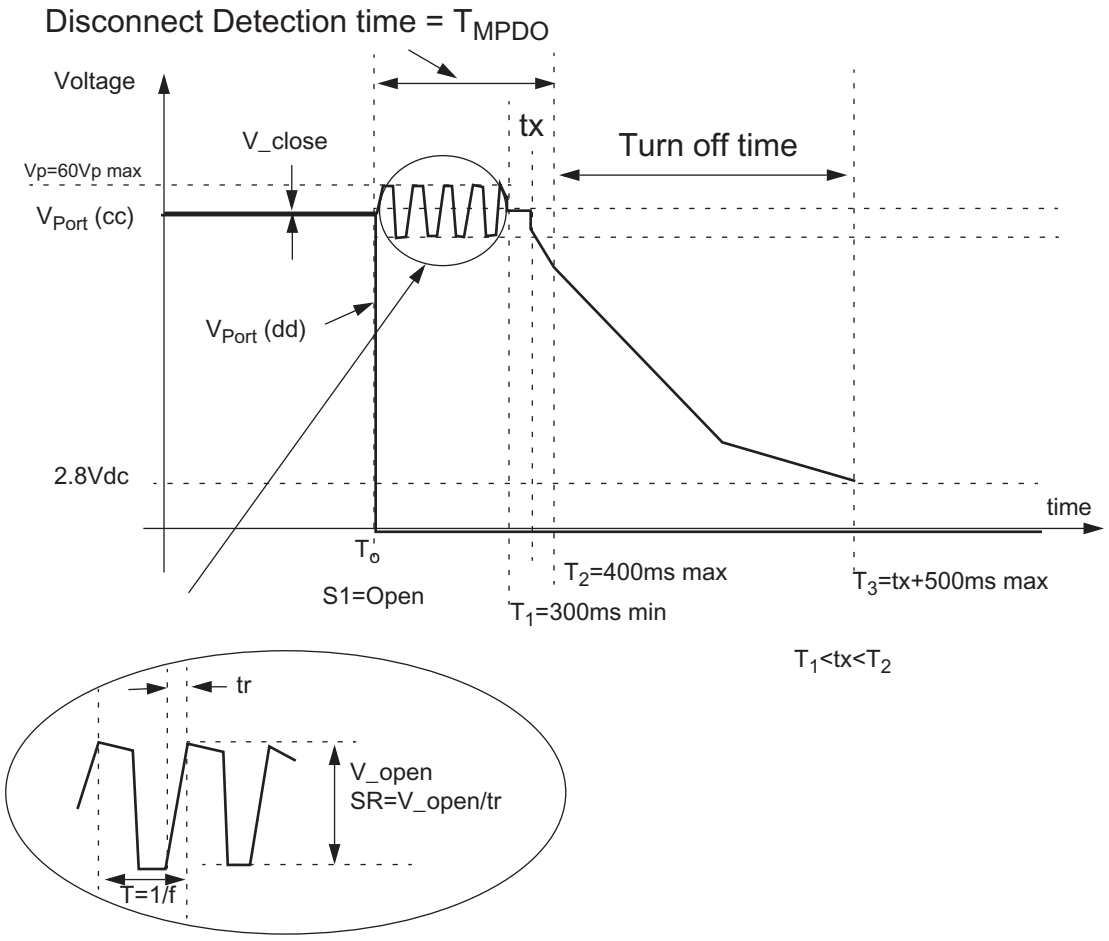


Figure 33C.15—AC disconnect timing relationships

33C.2.2 Test Procedure PSE-14 (port impedance)

Test Procedure PSE-14 is used for testing the following:

a) $I_{\_sac}$ (Table 33–6, item 2a) when monitoring the AC MPS component (33.2.10.1.1),
b) $R_{\_rev}$ (Table 33–6, item 2b) when monitoring the AC MPS component (33.2.10.1.1)
(If 33.2.10.1.2 is used, this test may be used when testing 33.2.5 according to Figure 33–8),
c) Z_{source} (Figure 33–8 and Figure 33–9), and
d) Detection short circuit (33.2.5).

Test Procedure PSE-14 uses Test Configuration PSE-J as shown in Figure 33C.16. In this test configuration terminals a, b, c, and d correspond to pin assignments according to Table 33C.1.

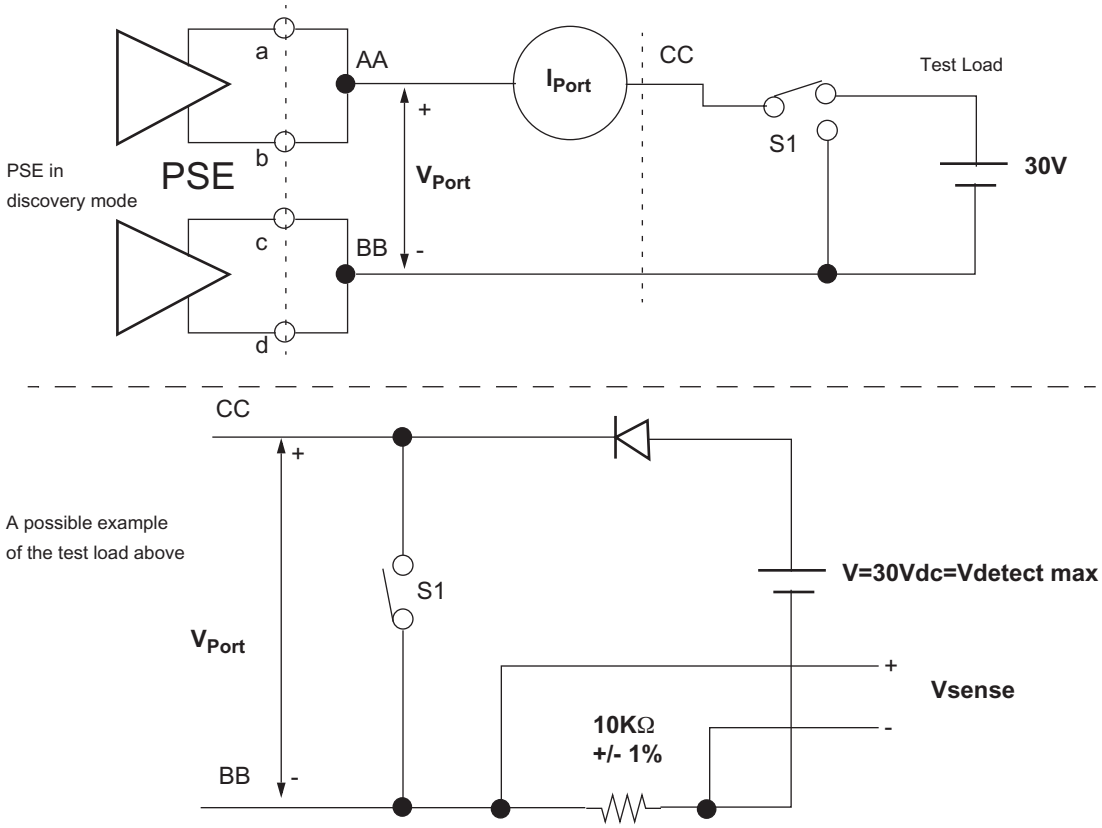


Figure 33C.16—Test configuration PSE-J

Test Procedure PSE-14 is as follows:

1) Set S1 = close. Monitor I_{Port} and verify that I_{Port} is less than 5mA over a 2 second period. (Ignore results of first 1ms).
2) Verify that I_{Port} at frequency Fp is less than 5mA over a 2 second period. (Ignore results of first 1ms).
3) Set S1 = open.
4) Verify that Vsense<5.27Vp (i.e., (30V – Vd) × 10K/(10K + 45K)) over a 2 second period. Vd is the forward diode voltage drop assumed to be 1V in this example.

33C.3 Recommended PSE detection signature test procedures

33C.3.1 Test Procedure PSE-15 (signature detection parameters)

Test Procedure PSE-15 is used for testing the following:

a) PSE port impedance during detection (see 33C.2.2),
b) Parallel diode across the port (33.2.5, Figure 33-8 and Figure 33-9),

c) V_{oc} (Table 33–2, item 1),
d) I_{sc} (Table 33–2, item 2),
e) V_{valid} (Table 33–2, item 3),
f) ΔV_{test} (Table 33–2, item 4),
g) R_{good}, (Table 33–2, item 7)
h) R_{bad} (Table 33–2, item 8),
i) C_{bad} (Table 33–2, item 11),
j) V_{slew} (Table 33–2, item 6),
k) Detection and power on the same leads (33.2.4), and
l) V_{OS} (Table 33–2, item 12).

Test Procedure PSE-15 uses Test Configuration PSE-K. In this test configuration, terminals a, b, c, and d correspond to pin assignments according to Table 33C.1. The behavioral description is shown in Figure 33C.17.

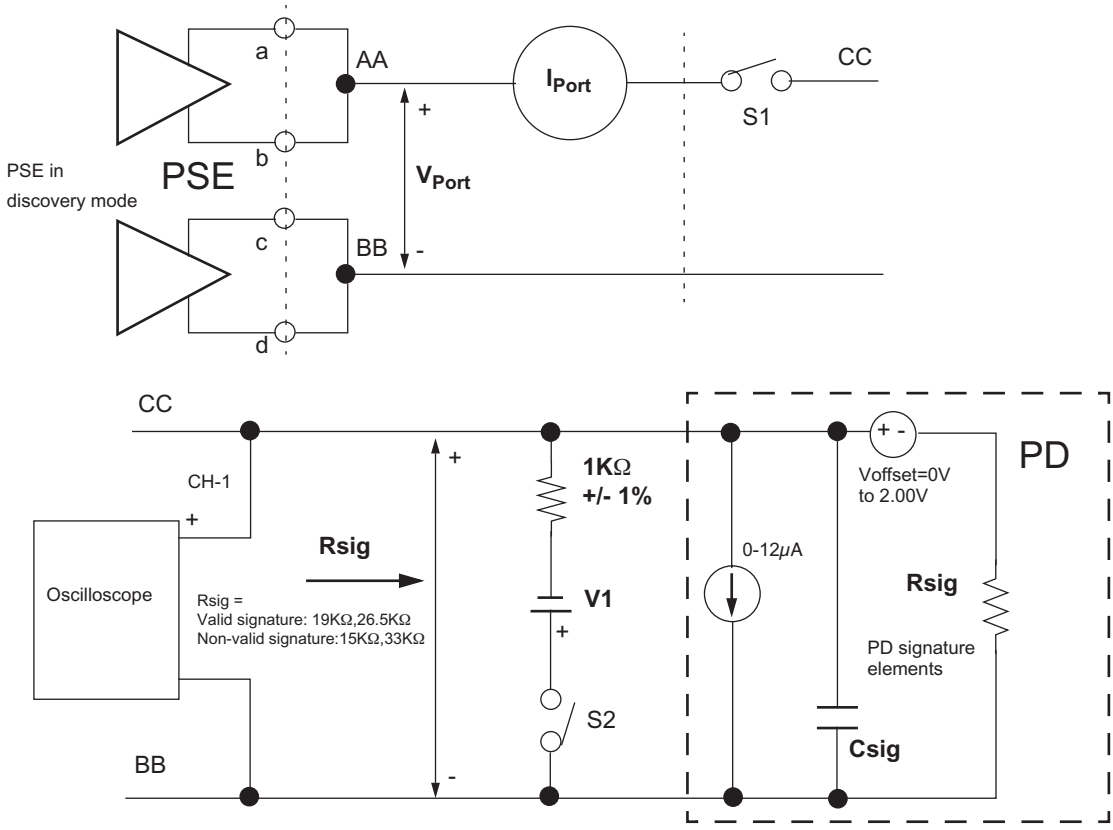


Figure 33C.17—Test configuration PSE-K

An example of a possible test circuit is shown in Figure 33C.18.

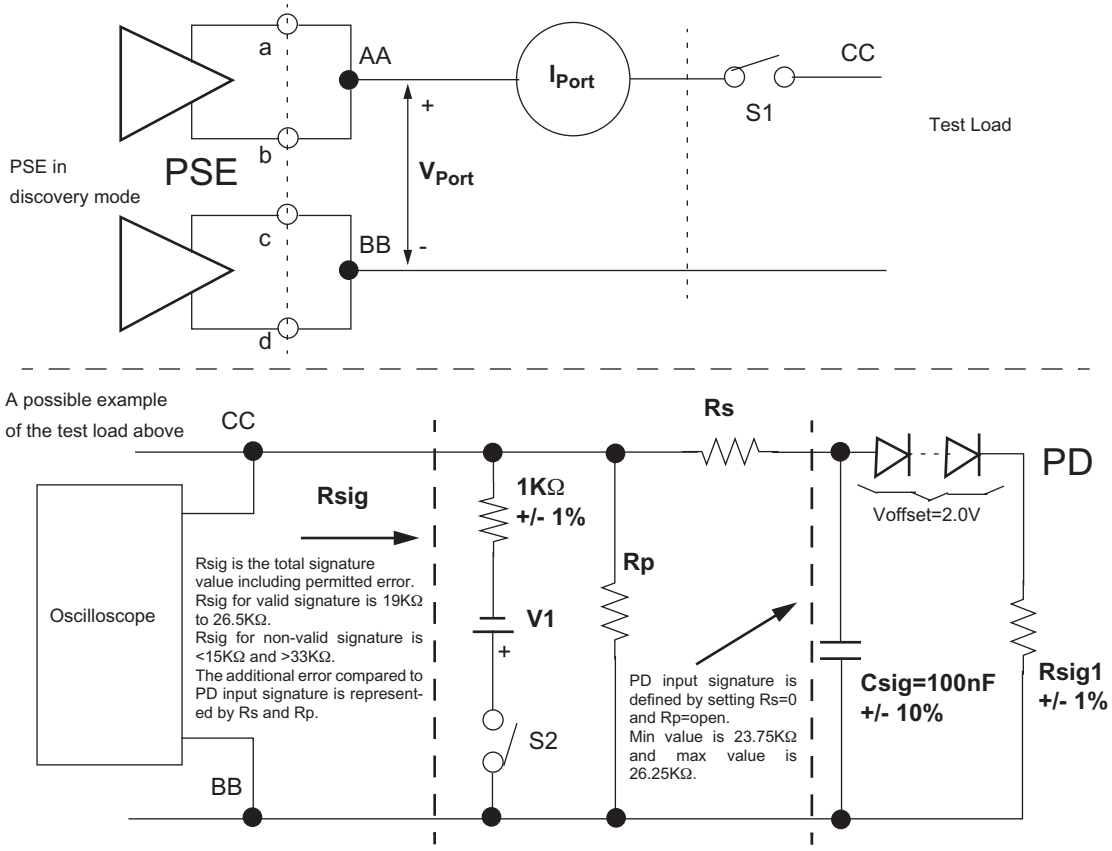


Figure 33C.18—Example of circuit for PSE-K

Test Procedure PSE-15 is as follows:

1) Parallel diode across the port (33.2.5, Figure 33-8 and Figure 33-9).
   a) Set S1 and S2 to OFF.
   b) Turn system OFF (No voltages across PSE port). Set V1 to 10.0V. Set S1 and S2 to ON.
   c) Measure I_{Port}. Verify that I_{Port} > 3mA.
   d) Reverse V1 polarity. Verify that I_{Port} < 40 μA.
   e) Set S2 to OFF.
2) Detection open circuit voltage (33.2.5).
   a) Set S1 and S2 to OFF.
   b) Verify that V_{Port} < 30Vp during the detection phase for 500ms max out of T_{tot} period as specified in Figure 33C.11.
      Verify that V_{Port} average is <=2.8Vdc when the PSE is not in detection phase.
   c) Verify that the voltage slew rate is less than 0.1V/μs.
   d) It is allowed to have no detection signals or to have single-point detection if the PSE identifies that the port is open.
3) Detection short circuit current (33.2.5).
   See Test Procedure PSE-14.
4) Detection minimum/maximum voltages (33.2.5.1),
   Two-point detection voltage difference (33.2.5.1),
   Detection criteria (33.2.6.1),
   Rejection criteria (33.2.6.2),

Detection voltage slew rate (33.2.5.1), and
Detection and power on the same leads (33.2.5.1).

a) Part 1.
   i) Set Rs=0. Adjust V_{OFFSET} to 0V.
   ii) Set Rsig1 to 23.75KΩ. Adjust Rsig to 19.0KΩ by adjusting Rp.
   iii) Adjust V_{OFFSET} to 2.0V.
b) Part 2.
   i) Set S1 to ON. Set S2 to OFF.
   ii) Monitor V_{Port} and measure detection voltages Vdet1 and Vdet2.
   Verify that Vdet1 and Vdet2 are between 2.8V and 10V and |Vdet2 - Vdet1|>=1V.
   iii) Verify that 44V min is present across the port for 299ms min.
   iv) Verify that the slew rates of all the switched voltages are less than 0.1V/ μs.
c) Part 3.
   i) Adjust V_{OFFSET} to 0V.
   ii) Set Rsig1 to 26.25KΩ. Set Rp=Open. Adjust Rsig to 26.5KΩ. by adjusting Rs.
   iii) Adjust V_{OFFSET} to 2.0V.
   iv) Repeat step 4ii.
d) Part 4.
   i) Adjust V_{OFFSET} to 0V.
   ii) Set Rs=0. Set Rp=open. Set Rsig1 to 14.7KΩ+/-1%.
   iii) Set S1 to ON. Set S2 to OFF.
   iv) Verify that power is not applied to the port.
e) Part 5.
   i) Adjust V_{OFFSET} to 0V.
   ii) Set Rs=0. Set Rp=Open. Set Rsig1 to 34KΩ+/-1%.
   iii) Set S1 to ON. Set S2 to OFF.
   iv) Verify that power is not applied to the port.
f) Part 6.
   i) Set Rsig1 to 24.9KΩ. Set Rp=Open. Set Rsig=0. Set Csig=10.0μF.
   ii) Adjust V_{OFFSET} to 2.0V.
   iii) Set S1 to ON. Set S2 to OFF.
   iv) Verify that power is not applied to the port.
   v) Repeat steps ii to v with Rsig1=open.

33C.4 Recommended PD detection signature test procedures

33C.4.1 Test Procedure SIG-1 (PD signature characteristics)

Test Procedure SIG-1 is used for testing the following:

a) V-I slope (Table 33–8),
b) V offset (Table 33–8),
c) Input capacitance (Table 33–8), and
d) PD classification current (Table 33–11).

Test Procedure SIG-1 uses Test Configuration SIG-A as shown in Figure 33C.19. In this test configuration, terminals a, b, c, and d correspond to pin assignments according to Table 33C.2

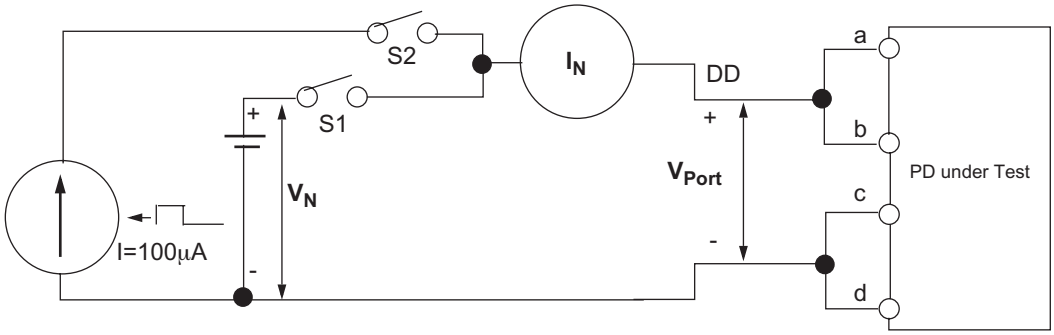


Figure 33C.19—Test configuration SIG-A

Test Procedure SIG-1 is as follows:

1) Set S1 to ON. Set S2 to OFF. Limit the current of V_N to between 4 and 5 mA.
2) Change V_N from 2.70V to 10.1V in steps of 1.00V and measure I_N for each V_N value.
3) Calculate $Rsig_N = (V_{N+1} - V_N)/(I_{N+1} - I_N)$.
4) Verify that 23.75KΩ<=RsigN <= 26.25KΩ. Find the current/voltage offset by calculating the intersection of the line between the (V_N, I_N) and (V_{N+1}, I_{N+1}) data points and the V/I axis. Verify that the current offset is less than 10 μA and the voltage offset is less than 1.9V.
   NOTE— The concept of this setup is to measure the equivalent Rsig as seen at the PD port and includes all possible errors caused by series diode drops (V offset) and component accuracy.
   Rsig is calculated with a minimum of two measurements to simulate PSE operation.
5) Change V_N from 0.00V to 2.70V in steps of 0.20V and measure I_N.
6) Plot the results of I_N vs. V_N from steps 1 and 5 and find V offset. See Figure 33C.20.
7) Set S1 to OFF. Set S2 to ON. Ignore any data points above 10V.
8) Activate the switched current source.
   NOTE—The concept of this setup is to calculate the capacitance value by ramping the capacitance voltage with a constant current source and using the equation I × t = V × C. This method is useful when series diodes are present.
9) Calculate the port capacitance (Cpd) by measuring Rpd (port resistance) and using it in the typical differential equation solution.
10) Verify that the PD port capacitance is between 50nF and 120nF.
11) Set the voltage source to sweep from 14.5V to 20.5V.
12) Observe the current at I_N and verify that it falls in the valid range per Table 33–11.

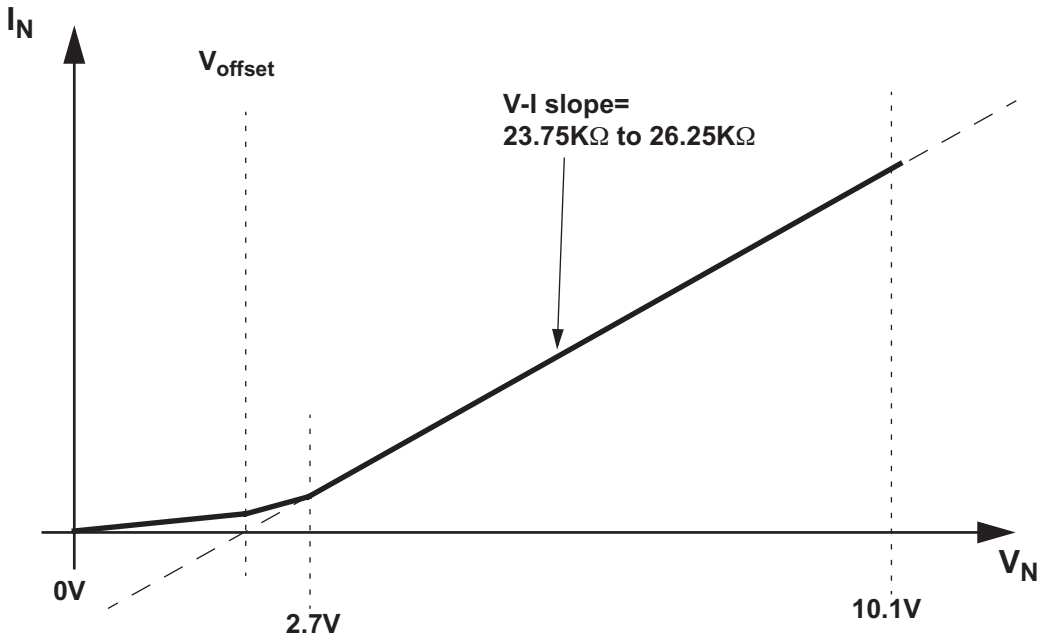


Figure 33C.20—Signature voltage offset

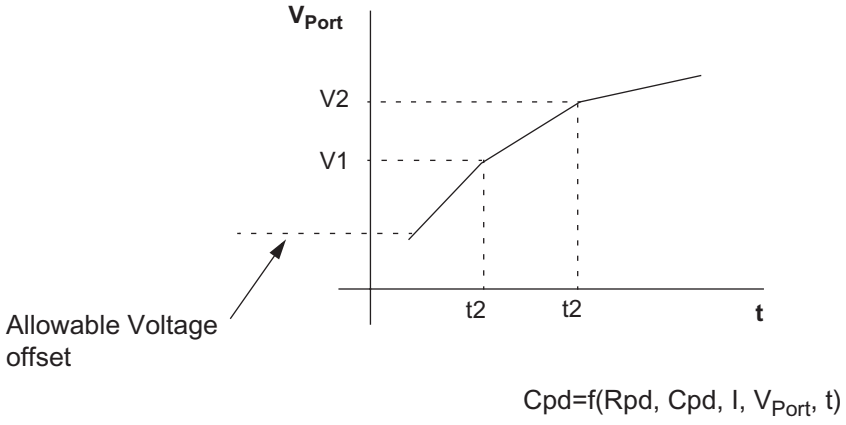


Figure 33C.21—Signature input capacitance

33C.5 Recommended PD power supply test procedures

33C.5.1 Test Procedure PD-1 (all parameters)

Test Procedure PD-1 is used for testing the following:

a) V_{Off} (Table 33–12, item 8b),
b) V_{On} (Table 33–12, item 8a),
c) I_{Port} (max input current during startup) at Vpse=44Vdc (Table 33–12, item 5),
d) I_{Port} (max input current during startup) at Vpse=57Vdc (Table 33–12, item 5),
e) I_{Port} (max average input current during normal powering mode at V_{Port}=37Vdc) (Table 33–12, item 3),
f) P_{Port} (max input power at 37Vdc) (Table 33–12, item 2),
g) Max input peak current at V_{Port}=37Vdc and max load (Table 33–12, item 2),
h) I_{Port} (max average input current during normal powering mode at V_{Port}=57Vdc) (Table 33–12, item 3),
i) P_{Port} (max input power at 57Vdc) (Table 33–12, item 2),
j) Max input peak current at V_{Port}=57Vdc and max load (Table 33–12, item 2),
k) I_{Port} (min input current at V_{Port}=37Vdc) (Table 33–13, item 1),
l) I_{Port} (min input current at V_{Port}=57Vdc) (Table 33–13, item 1),
m) Polarity insensitivity when PD implements Auto-MDI-X (33.3.1), and
n) PD false underload timing limitations (33.3.6.1).

Test Procedure PD-1 uses Test Configuration PD-A as shown in Figure 33C.22. In this test configuration, terminals a, b, c, and d correspond to pin assignments according to Table 33C.2.
CL is a controlled current limit device with two threshold settings, CL1 and CL2.
CL1 and CL2 are time-limited to TCL1 and TCL2.
If I_{Port} > = CL1 for t > TCL1, then S1 is opened and test is failed.

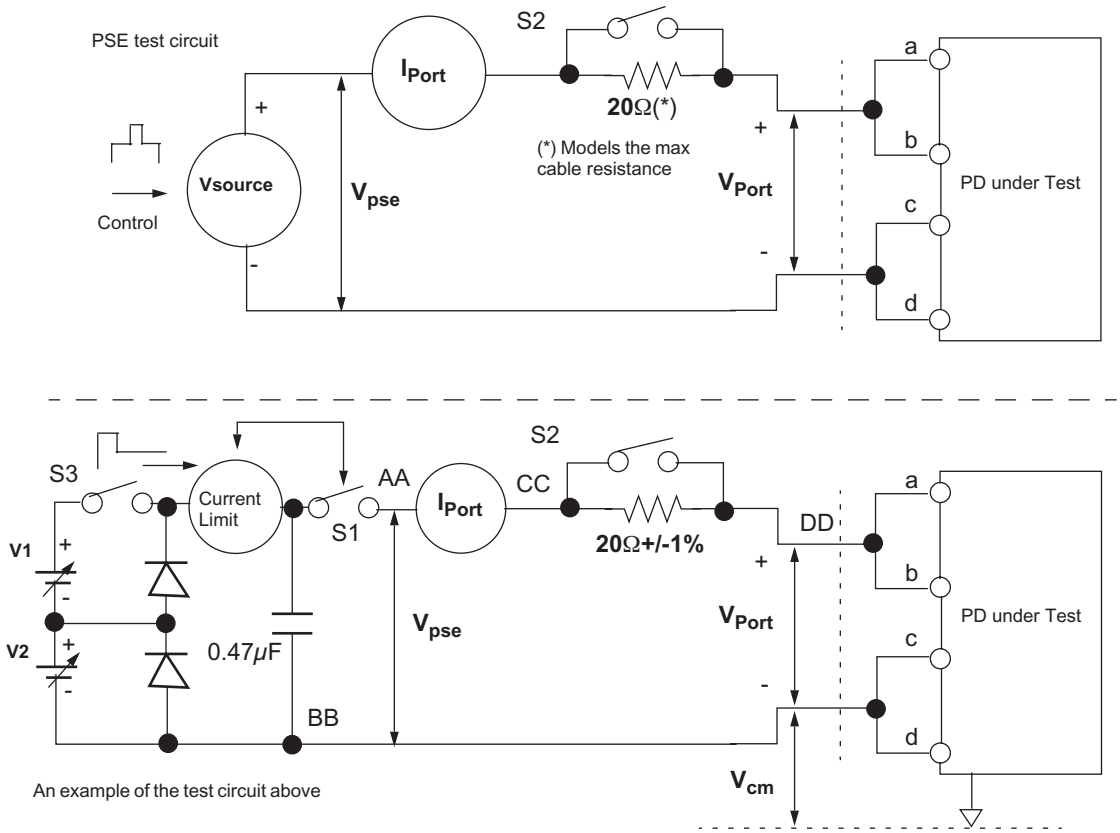


Figure 33C.22—Test configuration PD-A

Test Procedure PD-1 is as follows:

1) Set S1 to OFF. Set S2 to ON. Set V1 to 30.0V. Set CL1=CL2=1.0A.
2) Set S1 to ON. Wait 1sec and verify that I_{Port}< 1.14mA(=30V/26.25KΩ)
3) Set S1 to OFF. Set S2 to OFF. Set V1 to 44.0V. Set V2=0.0V. Set CL1=CL2=0.4A,TCL1=50ms, CL2=350.0mA and TCL2=5sec. Set PD for max load mode.
4) Set S1 to ON.
5) Record the following parameters: I_{Inrush}, T_{Inrush}, V_{on}. See Figure 33C.23.
6) Set S1 to OFF.
7) Set V1 to 57.0V. Set S1 to ON and record the following parameters: I_{Inrush}, T_{Inrush}, V_{on}. See Figure 33C.23.
8) Set S2 to ON. Set V1 = 37.0V, V2 = 0.0V, CL1 = 0.4A, TCL1 = 50ms, CL2 = 350.0mA and TCL2=5sec. Set PD for max load mode.
9) Wait 1sec and record Iport_dc and Iport_ac parameters. See Figure 33C.23.
10) Set V1=57V and repeat steps 8,9.
11) Set S2 to ON. Set V1 = 30.0V, V2 = 0.0V, CL1 = 0.4A, TCL1=50ms, CL2=350.0mA and TCL2=5sec. Set PD for max load mode.
12) Increase V1 until PD power supply turns ON. Verify that V1<=Von.

13) Set S1 to OFF. Set S2 to ON. Set V1 = 37.0V, V2 = 0.0V, CL1 = 0.4A, TCL1=50ms, CL2=350.0mA and TCL2=5sec. Set PD to min load if applicable.
14) Set V1=57.0V. Verify that I_{Port}>= 10mA.
15) If the PD implements Auto-MDI-X, repeat steps 3, 4, and 5, and verify PD operation with reverse polarity connection.
16) Set V1=44V and V2=13V. Set PD to its minimum operating load.
17) Wait 1sec until I_{Port} is stable.
18) Set S3 to OFF and monitor I_{Port}. Verify that I_{Port} is less than 10mA for only T_{UNLD}<290ms. If I_{Port} is not less than 10mA for any time duration, then timing requirement is ignored. See Figure 33C.24.
19) To verify PD input capacitance during normal operating mode: Set S1 to OFF. Set S2 to ON. Set V1=57.0V, V2=0.0V, CL1=CL2=1.0A,TCL1=TCL2=10sec. Set PD for constant load.
20) Set S1 to ON.
21) Wait 1sec and measure I_{Port}.
22) Set S1 to OFF while monitoring V_{Port}. Measure the time duration, Tdrop for V_{Port} to drop from 57.0V to 56.0V.
Calculate C=I_{Port} ×Tdrop/1V. Verify that 5μF<C<180μF.
23) If C>180μF, set CL1=CL2=1.0A, TCL1=TCL2=5sec.
Repeat all tests regarding inrush current limitation and verify that inrush current is limited by the PD to 0.4A max.
24) Set V1 to 44V, V2=0V. Set S1 to ON. Measure V_{Port} and Vcm noise level at V_{Port} between 37V and 57V and at all known PD operating conditions.

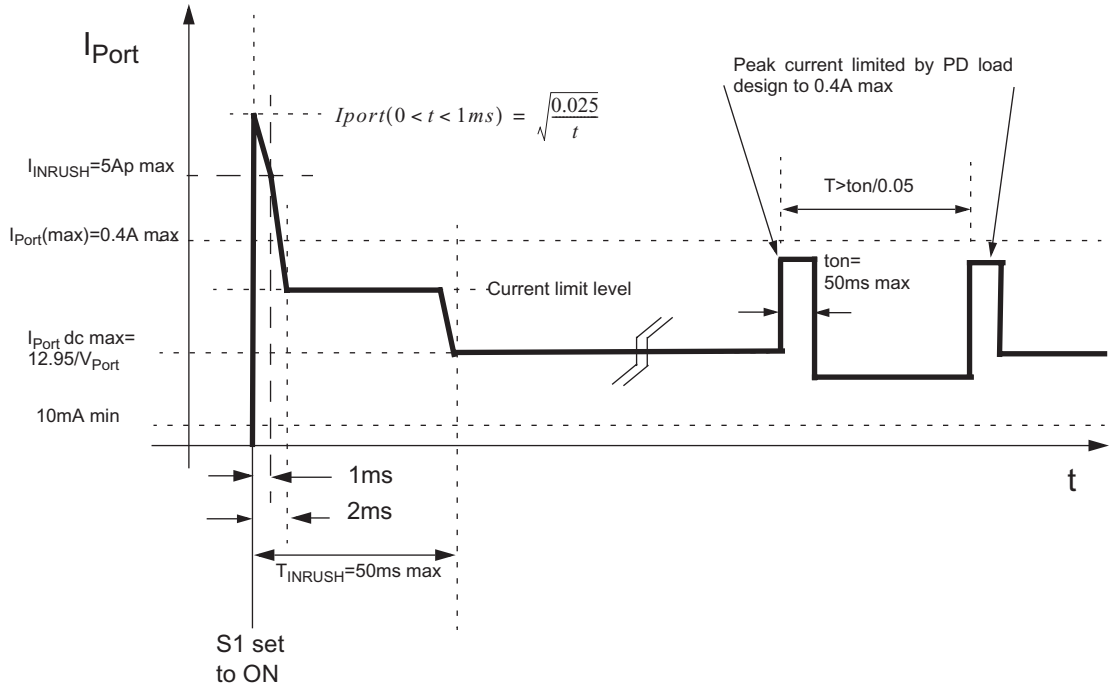


Figure 33C.23—PD inrush current timing and max peak ripple current and time duration at normal powering mode

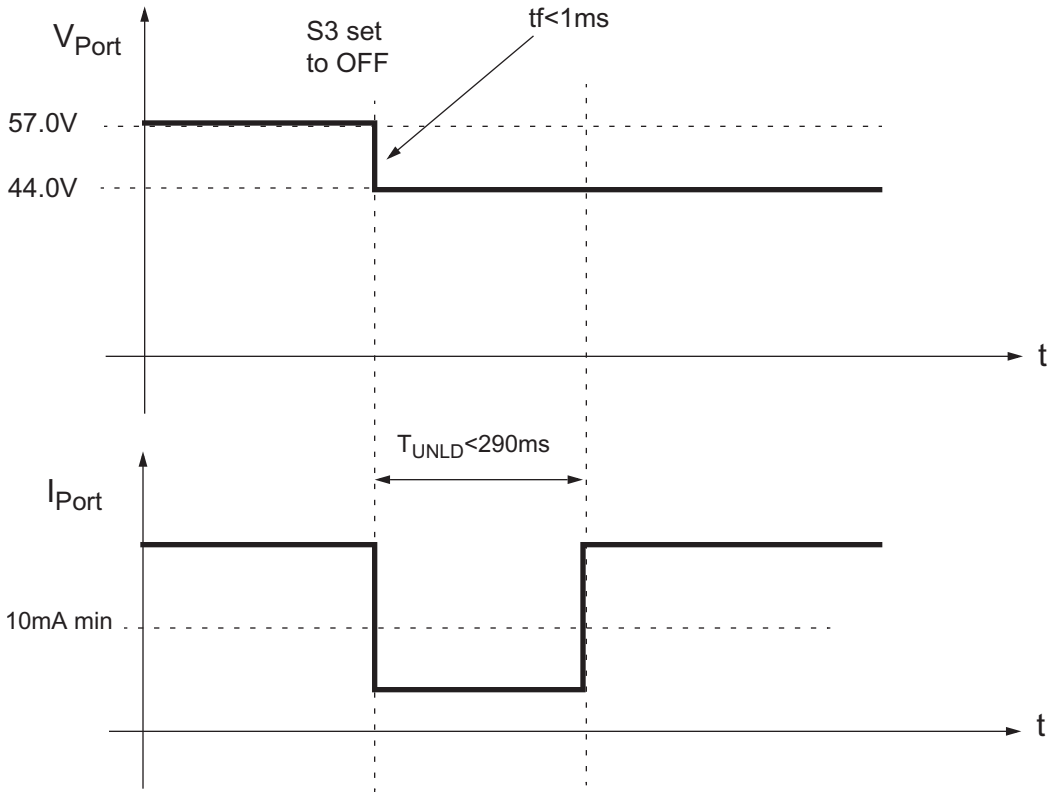


Figure 33C.24—PD underload timing

Annex 33D

(informative)

PSE-PD stability

33D.1 Recommended PSE design guidelines and test setup

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance (Zo_port), the cable impedance (Zc), the PD input port circuitry impedance (Zpd_cir) and the PD EMI output filter impedance (Z_emi) should be lower than the PD power supply input impedance (Zin_ps_pd). This subclause focuses on the PSE part.

Port output impedance consists of two parts:

a) PSE power supply output impedance (Zo_ps), which is function of the load (P_{Port}), and
b) Series elements (Z_ser) which connect the PSE power supply output to the port.

Therefore, the total Port output impedance during normal powering mode is Zo_port=Zo_ps+Z_ser.

In order to maintain PSE-PD stability, the following guidelines apply:

a) Zo_ps max =0.3Ω. at frequencies up to 100KHz at Pport=15.4W.
   Zo_ps can be extracted from Zport by measuring V_{Port}/I_{Port} (with an external power dynamic analyzer system) as a function of frequency and subtracting from Zport the value of Zser (f=DC) which is limited by the value of Zser at DC (low frequency).
b) If Zo_ps<Zo_ser and V_{Port} is kept to 44V min and 57Vmax during dynamic load changes from 10Hz to 100KHz, then the value of Zo_ps is not limited.

Compliance to the above requirements should be made by measuring the port output impedance from 10Hz to 100KHz at 15.4W load at short cable length or by presenting simulation results.

See Figure 33D.1 for the PSE-PD system impedance allocation.

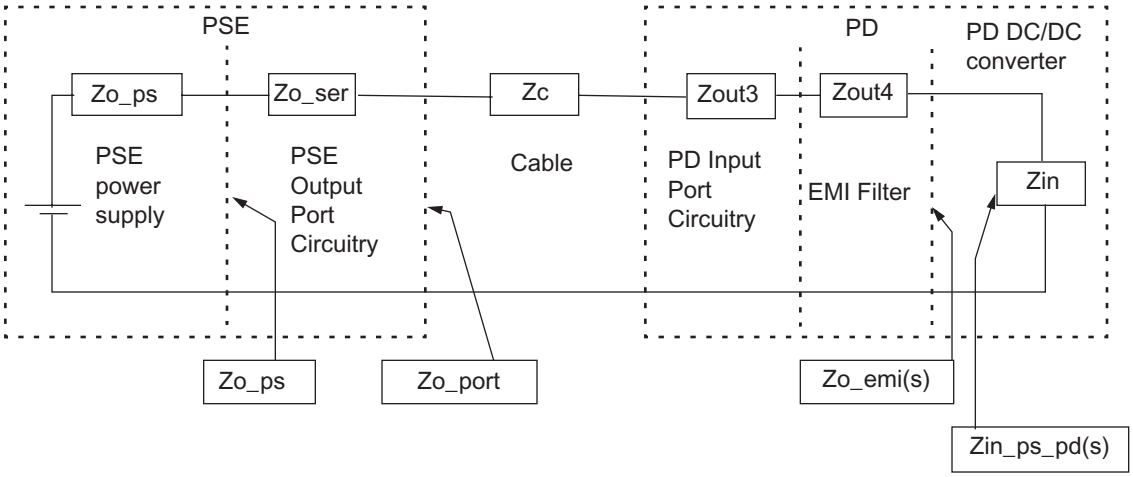


Figure 33D.1—PSE - PD system impedance allocation

See Figure 33D.2 for the test setup and Figure 33D.3 for the test requirements.

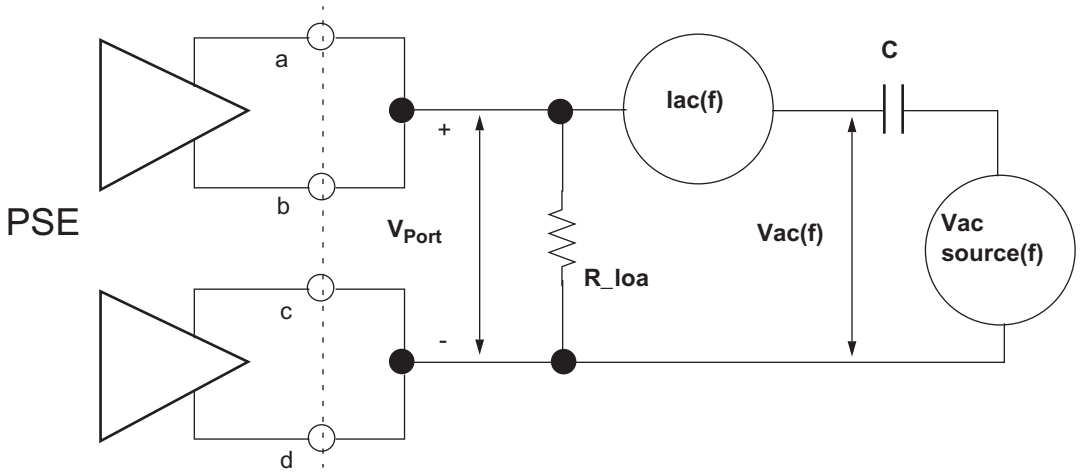


Figure 33D.2—Test setup for measuring Zo_port

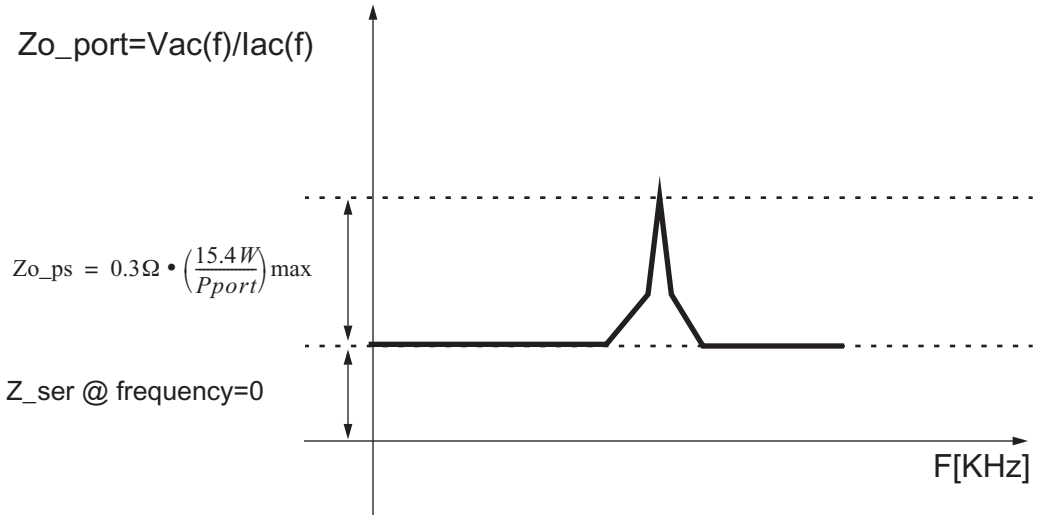


Figure 33D.3—Test requirements for measuring Zo_port

33D.2 Recommended PD design guidelines

PD port input impedance consists of two parts:

a) PD port input circuits including the EMI filter (Zin_ser), and
b) PD power supply input impedance (Zin_ps_pd), which is fed by the output of the EMI filter (Zo_emi).

In order to maintain stability with the PSE, the PD power supply input impedance (Zin_ps_pd) should be higher than the output impedance of the total network including the PD EMI output filter impedance fed by the cable (MDI) output impedance which is fed by the PSE port output impedance.

The worst case scenario is when the cable (MDI) length is zero (in terms of lower damping factor).

The access to the PD input power supply is not possible through the PD port for evaluating the various impedances and derivation of the above parameters. Because of this, measuring the PD input impedance is a complicated task, the following guidelines should be followed by the PD vendor:

c) The PD power supply input impedance (Zin_ps_pd) at max load of P_{port}=12.95W should be higher than 30Ω at any frequency up to the PD power supply crossover frequency. If the PD power supply is consuming less than P_{port}=12.95W, then Zin_ps_pd min=30×12.95/P_{port}.
d) The PD power supply EMI filter output impedance should be Zo_emi=2.7Ω max. If the PD power supply is consuming less than P_{port}=12.95W, then Zo_emi=2.7×12.95/P_{port}.

See Figure 33D.1 for the PSE-PD system impedance allocation.

Annex 33E

(informative)

Cabling resistance unbalance

This standard sets the maximum current that can be continuously drawn by the PD at 350mA total or 175mA per individual conductor of the differential pair. One drawback to implementing this scheme that should always be considered is the resistance unbalance associated with the cabling. The cabling resistance unbalance parameter is specified in this standard in reference to IEC 11801 Edition 2, Clause 6.4.8, (reference: 3 percent).

The 3% cabling resistance unbalance is specified for the ISO/IEC cabling channel illustrated in Figure 33-18. At the maximum current allowed, this resistance unbalance equates to a 10.5mA difference between the two paths.

Significant work on current imbalance in transformers has shown that certain data patterns induced a large baseline wander. Baseline wander induced a DC offset comparable to 6mA. The transformer specification that resulted is 350μH under all conditions of tolerance, temperature, and with 8mA of DC bias.

Using a transformer that can only tolerate this amount of DC bias reduces the maximum current the PSE can deliver without saturating the transformer to:

$$350\text{mA} \times (8\text{mA}/10.5\text{mA}) = 267\text{mA} \quad (33\text{E}–1)$$

In order to restore the current capability to 350mA, some form of ballast circuitry must be employed. Figure 33E.1 details a method for resolving cable and connector unbalances by using two resistors. Note that these ballast resistors are required at each end of both the transmit and receive channels. The addition of the capacitor in parallel with the resistors helps to minimize the signal loss induced by the balancing resistors and should be selected to present a low impedance at the lowest possible signal frequency.

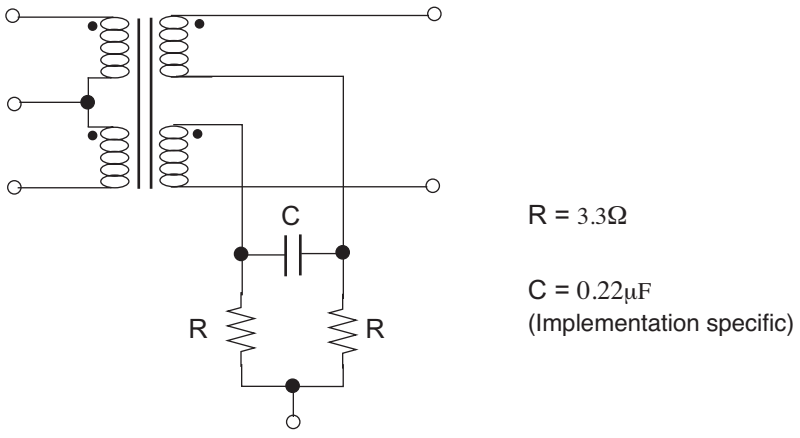


Figure 33E.1—Transformer detail

Table 33E.1 details the resistance of different cable sizes over minimum and maximum temperature ranges. These resistance values are used in calculations to resolve connector unbalance and voltage drops.

Table 33E.1—PSE PI pin assignments for test procedure terminals

AWG	Min at 0 C	Max at 0 C	Nominal Ω	Min at 50 C	Max at 50 C
26	12.18	12.79	13.47	14.70	15.43
24	7.65	8.03	8.42	9.14	9.60
22	4.81	5.05	5.31	5.79	6.08

For purposes of calculating the ballast resistors, a typical maximum configuration of five connectors is used. Each connection point has one contact measuring 0Ω with the other contact measuring 0.02Ω, which is the maximum allowed resistance per IEC 60512-2. Furthermore, a five meter length of 22 AWG cable is used because longer lengths reduce the unbalance. The equations describing this interaction are:

$$\left(\frac{Iout + Iimbal}{2} \times \left(\frac{Rc}{1.03} + \frac{Rb}{1.01}\right)\right) = \left(\frac{Iout - Iimbal}{2} \times (Rc \times 1.03 + Rb \times 1.01 + Rconn)\right) \quad (33E–2)$$

where:

Iout = 350mA (maximum current from the PSE),
Iimbal = 8mA (current difference between the two paths),
Rc = 0.24Ω (5m of 22 AWG cable),
Rb = 6.6Ω (ballast resistance), and.
Rconn = 0.1Ω (total contact resistance for 5 connectors).

Under these conditions the worst case current unbalance is 6.2mA. Using 3.3Ω ballast resistors increases the total voltage drop associated with the cabling by:

$$(175+(6.2/2))\text{mA} \times (4 \times 3.3\text{W}) = 2.35\text{V} \quad (33E–3)$$

According to this standard, the minimum voltage sourced by the PSE must be greater than 44V, and the maximum voltage presented by the PD must be less than 36V. This 8V margin permits up to 45.7Ω of resistance per conductor path to exist between the PSE and PD under maximum current conditions. Even under worst case conditions of temperature and tolerance, using 3.3Ω ballast resistors in series with 100m of 26AWG cable (see Table 33E.1) still provides a margin of:

$$8\text{V} - (175\text{mA} \times (30.86\text{W} \times 1.03 + 0.1 + 4 \times 3.3\text{W} \times 1.01)) = 0.28\text{V} \quad (33E–4)$$

The ballast resistors will dissipate worst case power during an overcurrent condition, which this standard has set at 450mA. In this case the wattage rating of the ballast resistors would be:

$$(450\text{mA}/2)\text{exp}2 \times 3.3\text{W} = 0.17\text{W} \quad (33E–5)$$

Using standard sizes, this becomes 0.25W.