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APPLICATION NOTE

From the Allstar to the Superstar II

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1. INTRODUCTION

CMC Electronics has introduced the ***SUPERSTAR II:*** a breakthrough in low-cost and small-size superior quality GPS receivers for embedded applications. The ***SUPERSTAR II*** is the next generation to the highly popular Superstar and Allstar high-end OEM Receiver and has kept the same robust signal tracking and unsurpassed tracking capability under difficult signal conditions.

The ***SUPERSTAR II*** is a complete GPS OEM sensor that provides 3D navigation on a single compact board with full differential capability. The ***SUPERSTAR II*** is a 12-channel GPS receiver that tracks all in-view satellites. It is fully autonomous such that once power is applied, the ***SUPERSTAR II*** automatically searches, acquires and tracks GPS satellites. When a sufficient number of satellites are tracked with valid measurements, the ***SUPERSTAR II*** produces a 3-D position and velocity output with an associated figure of merit (FOM).

The ***SUPERSTAR II*** has the same architecture as the Superstar and Allstar based on the Zarlink Semiconductor GPS chipset. 1Hz PVT mode is offered as a standard product. The 3.3VDC version of this product is also available.

1.1 Scope

This document provides information on the Superstar II GPS OEM board P/N 220-604090-XXX and 245-604090-XXX. The following sections describe functionality, mechanical and electrical characteristics of the ***SUPERSTAR II*** board and provides the major differences in the Allstar manual for P/N 220-604944-XXX.

To get help, please contact CMC Electronics Inc. at the following coordinates:

Telephone: 514-748-3070
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2. FUNCTIONALITY

2.1 Protocol Selection & Non Volatile Memory

The ***SUPERSTAR II*** offers the NMEA user the option of setting I/O operating mode to NMEA through discrete input levels. Disc_IP2 and Disc_IP_3 have the following functions:

Disc_IP_3 (Protocol Select)	Disc_IP_2 (NVM Control)	Result
OPEN - HI	**OPEN – HI**	**Configuration stored in NVM or Default ROM Configuration if no valid NVM elements**
OPEN - HI	**GND**	**Protocol on Port #1: CMC Binary Baud Rate on Port #1 : 9600 Other elements : Default ROM Configuration**
GND	**OPEN – HI**	**Protocol on Port #1: NMEA Baud Rate on Port #1 : 4800 Other elements : Default ROM Configuration if no valid NVM elements**
GND	**GND**	**Protocol on Port #1: NMEA Baud Rate on Port #1 : 4800 Other elements : Default ROM Configuration**

2.2 Default Configuration if no valid NVM elements:

- Protocol on port #1: CMC Binary
- Baud Rate on port #1: 9600
- Protocol on port #2: RTCM-104
- Baud Rate on port #2: 9600
- DGPS Correction Timeout: 45 seconds

- Default Message List:
  - CMC Binary: Navigation Status User Coordinates (#20) @ 1Hz
  - NMEA : GGA @ 1Hz

- Time Align Mode : ON **(Note : OFF for the ALLSTAR)**

Notes:

1. The data contained in the NVM is always used if the DISC_IP_2 is left unconnected or tied to HI logic.

2. If DISC_IP_2 is tied to LO logic, the default ROM configuration will be used and the following parameters will not be read from NVM:

   - Position
   - Almanac
   - Time
   - UTC Correction and IONO Parameters
   - TCXO Parameters

2.3 Memory Battery Back-Up

The ***SUPERSTAR II*** can perform Warm Start without the need of an external supply source to maintain the data or the time during Power-Off State.
An On-Board supercap allows the time-keeping circuit to be maintained for a period of at least 3 days over the temperature range (1 week typically).

3. MECHANICAL

3.1 Connectors

3.1.1 I/O Connector (J1)

The ***SUPERSTAR II*** connector is a 2mm straight or right angle 2x10 pin header.

Suggested supplier:	Samtec
On-Board connector:	TMM-110-03-T-D.

Interface between ***SUPERSTAR II*** and customer application:

Suggested 2 inch ribbon cable:	TCSD-10-D-2.00-01-N

Or

Suggested 12 inch ribbon cable with only one connector installed:	TCSD-10-S-12.0-01-N
Suggested mating connector:	TCSD-10-01-N.

Or

PCB mounted connector:	SQT-110-01-L-D

Note: 0.340” long standoffs will be required

This information is provided as a guideline only; the latest connector specifications can be obtained from Samtec or other similar manufacturers.

3.1.2 RF Connector (J2)

The standard RF connector is a straight MCX jack connector. A right angle MCX connector is offered as an option.

Suggested supplier:	Johnson Comp
On-Board connector:	133-3701-211

Interface between ***SUPERSTAR II*** and customer application:

Suggested Supplier:	Omni Spectra
Supplier part number:	5831-5001-10

Suggested Supplier:	Suhner
Supplier part number:	11MCX-50-2-10C
Suggested Supplier:	Radiall
Supplier part number:	R113082.

The center conductor will provide power for an active antenna (PREAMP signal from J1-1).

3.2 Dimensions

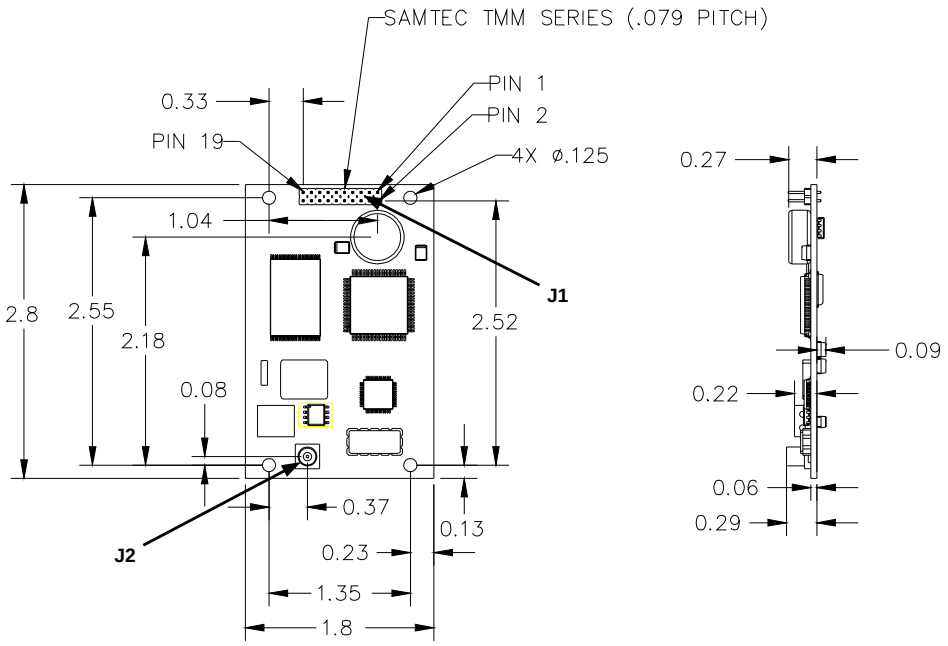

Figure 1-1 ***SUPERSTAR II*** board dimensions

4. ELECTRICAL SPECIFICATIONS

4.1 I/O Electrical Characteristics

All input pins shall have a valid state during reset and operating mode. No connection shall be required if the signal is not used in the application.

Signal Name	Type	Vil Max Volt	Vih min Volt	Vol max Volt	Voh min Volt	Notes
MASTER_RESET	I	0.5	2.0			(1) (4)
DISC_IP_1, _2, _3 RX_No_1, _2	I	0.8	2.5			(3) (4) (6)
DISC_IO_1, _2	I/O	0.8	2.5	0.4	3.0	Iout<=200uA (3),(5),(8)
TX_No_1, _2	O			0.4	3.0	Iout<=200uA (4),(9)
RX_No_3/DISC_IO_3	I/O	0.8	2.0	0.4	3.7	Iout<=200uA (3),(4),(8)
TIMEMARK TX_No_3	O			0.4	3.7	Iout<=200uA (7),(8)

Note 1: A LO pulse of 150ns will invoke a master reset to the Superstar II (Max. 1usec rise & fall time)
Note 2: Conditions: 5V +10%/-5% for all limits
Note 3: Maximum input Voltage is 5.5V
Note 4: All pins are in input mode during reset with pull-up resistor
Note 5: All pins are in input mode during reset with pull-down resistor
Note 6: DISC_IP_1 (Programming Ctrl Pin) is in input mode during reset with pull-down resistor
Note 7: All pins are forced to an output logic level 0 during reset state
Note 8: All outputs shall deliver a maximum current of 2mA

4.2 Interface connector J1 (2X10, 2mm header)

PIN #	Signal Name	Function
1	PREAMP	Power for active antenna (40 mA max)
2	VCC	Primary power (5V +10%/-5%)
3	VBATT	Back-up power for real-time clock device (External series diode required)
4	RX_No_3/DISC_IO_3	Serial port RX #3 / Programmable Discrete I/O pin. Expansion pin for special application
5	MASTER_RESET	Reset Input pin (active LO)
6	DISC_IP_1	Reprogramming Control I/P pin (active HI)
7	DISC_IP_3	Protocol Select Pin (see section 2.1)
8	DISC_IP_2	NVM Control pin (see section 2.1)
9	DISC_IO_1	Programmable Discrete I/O pin Expansion pin for special application
10	GND	
11	TX_No_1	Serial port TX #1
12	RX_No_1	Serial port RX #1
13	GND	
14	TX_No_2	Serial port TX #2
15	RX_No_2	Serial port RX #2
16	GND	
17	DISC_IO_2	Programmable Discrete I/O pin Expansion pin for special application
18	GND	
19	TIMEMARK	1 Pulse Per Second O/P
20	TX_No_3	Serial port TX #3 Expansion pin for special application

4.2.1 Minimum Connections

The minimum number of connections required for the system to operate.

Signal name	Pin #
VCC	J1-2
Ground	J1-10, 13, 16 & 18
TX_No_1	J1-11
RX_No_1	J1-12

If **DGPS corrections** are required for the application, they may be transmitted to the ***SUPERSTAR II*** through the Main Port or through the Auxiliary port

Signal name	Pin #
RX_No_2	J1-15

If an **active antenna** is used:

Signal name	Pin #
PREAMP	J1-1

4.3 Power Requirements

4.3.1 PREAMP (active antenna supply)

Operating Voltage: 12Volts max
Current: 40mA max

4.3.2 VCC

VCC is the main and unique power source for normal operation

Max Operating Voltage: 5.5V
Operating Voltage: 5V [-5% +10%]

Ripple: 50mVp-p max

Power Consumption:	0.75W typical 1.00W max
Standby Power Consumption (Master Reset Applied or VCC < 3.8Volts)	<0.50 W typical

This following information applies to 3.3VDC boards only:

Max Operating Voltage:	3.63V
Operating Voltage:	3.3V [-5% +10%]
Ripple:	50mVp-p max
Power Consumption:	0.50W typical 0.70W max
Standby Power Consumption: (Master Reset Applied or VCC < 2.8Volts)	<0.40 W typical

4.3.3 VBATT

VBATT is an external back-up source for the Time Keeping Circuit. The ***SUPERSTAR II*** already has a supercap device allowing Warm Start for 1 week typically (25 deg C) and 3 days over temperature range (-30 +75 deg C). Therefore, VBATT is required only to extend the time retention period.

Note: An external series diode will be required between J1-3 and external power source to prevent the supercap from discharging into the customer's circuitry.

Max Input Voltage:	5.0 V
Min Input Voltage:	2.0 V
Input Voltage during normal Operation:	VCC - 1 diode drop
Required Current:	0.5uA typical 1.5uA maximum

5. SERIAL DATA INTERFACE

This section shows the differences in the CMC Binary protocol between the ALLSTAR and ***SUPERSTAR II*** OEM boards. The NMEA protocol is identical for both products.

RECEIVER TO HOST CPU MESSAGES

A. MESSAGE SUMMARY

ID	DEFINITION	MESSAGE TYPE	RATE (/SEC)	# BYTES
43	DGPS Configuration	UR		27
45	Hardware/Software identification request	UR	1	101
49	Receiver Status request	DR	1	12
51	Initiated BIT result	UR		40

LEGEND: CM: Command Message
DR: Data Request
PM: Protocol Message
UR: Upon Request

B. MESSAGE CONTENT - RECEIVER TO HOST CPU

MESSAGE	BYTE	DESCRIPTION	UNIT	TYPE
43 DGPS Configuration	5	Bit 0 : Enable (0=OFF, 1=On) Bits 1-6: **Reserved** Bit 7 : Port (0=Main, 1=Dedicated)	N/A	N/A
	6	Differential Coast Time	seconds	unsigned char
	7	Reserved	N/A	N/A
	8	Baud Rate (1=300, ... 32=9600, ... 64=19200)	300 bauds	N/A
	9-16	Messages requested for Retransmission (Bitmap: bit0 = 1, bit63 = 64) see message ID #83	N/A	N/A
	17-25	**Reserved**	N/A	N/A
45 Software Identification Information	5-18	Operational S/W Part number (XXX-XXXXXX-XXX)	N/A	char [14]
	19-32	First configuration Parameter block Part Number (XXX-XXXXXX-XXX)	N/A	char [14]
	33-36	First Configuration Parameter Block Checksum	N/A	unsigned long
	37-50	Boot S/W Part number (xxx-xxxxxx-xxx)	N/A	char [14]
	51	**Number of Config Block**	N/A	unsigned char
	52-54	**Variation block number 2**	N/A	unsigned char
	55-57	**Variation block number 3**	N/A	unsigned char
	58-60	**Variation block number 4**	N/A	unsigned char
	61-63	**Variation block number 5**	N/A	unsigned char
	64-66	**Variation block number 6**	N/A	unsigned char
	67-69	**Variation block number 7**	N/A	unsigned char
	70-72	**Variation block number 8**	N/A	unsigned char
	73-90	Reserved	N/A	N/A
	91-94	Boot Checksum	N/A	N/A
	95-98	Operational Checksum	N/A	N/A
	99	**Unit type** **Bit 0-2: Unit type** **000b : Allstar** **010b: Superstar 1** **100b: Superstar II**	N/A	N/A

MESSAGE	BYTE	DESCRIPTION	UNIT	TYPE
49 Receiver status data	5	Bit **0: System Mode** **0 - Acquisition** **1 - Navigation** **Bit 1-3: Reserved** **Bit 4-5: Power Up Mode** **0: Normal Power Up** **1: PLL lock** **2: Watch Dog Reset** Bit 6: Satellite tracking mode 0 - All SVs in view (based on current Almanac, position and time) 1 - Sky Search Bit 7 : NVM Controller State 0 - Idle (no process in progress) 1 - Busy (Erase and/or Store data process in progress)	N/A	N/A
	6	Bit 0 = 0: Tropo model enabled Bit 1 = 0: MSL model enabled Bit 2-3: Last Power-up Modes 0 – Cold Start (Invalid almanac, time or position) 1- Warm Start (Valid almanac, Time and Position) 2: Hot Start (Valid almanac, Time, Position and Ephemeris) Bit 4: Reserved Bit 5-7: Time Source 0 – Initialization required 1 – External 2 – SV without Nav 3 – SV with Nav	N/A	N/A
	7-8	Almanac Week of Collection	N/A	unsigned short
	9-10	Week number	N/A	unsigned short
	11-14	SV Deselect bitmap, Byte 11: bit 0 = SV1 … Byte 14: bit 7=SV32	N/A	N/A
	15-16	Channel Deselection bitmap, Byte 15: bit 0 = Ch1 … Byte 16: bit 7 - Ch12	N/A	N/A
	17-23	Reserved		
	24-25	Mask Angle	0.01 degree	**signed short**

MESSAGE	BYTE	DESCRIPTION	UNIT	TYPE
49 (Cont'd)	26	Discrete Inputs Bit 0: DISC_IP1 Bit 1: DISC_IP2 Bit 2: DISC_IP3 Bit 3: DISC_IO1 Bit 4: DISC_IO2 Bit 5: DISC_IO3 Bit 6-7: Reserved		
	27-28	TCXO Error Estimate	Hz	signed short
	29	TCXO Aging	0.1 ppm	unsigned char
	30-33	Search Noise	dB	short float
	34	Nav Mode (see message #20 byte 71 for description)	N/A	
	35-44	Reserved	N/A	N/A
51 Initiated BIT Result	5	Bit 0-7 : Copy of the Initiated BIT request message 0: Power Up BIT result 1: Initiated BIT result	N/A	N/A
	6	General Results (0=fail, 1=Pass) Bit 0 : RAM Bit 1 : Flash Bit 2 : EEPROM Bit 3 : UART Bit 4 : Real Time Clock Bit 5 : Correlator & RF Bit 6-7 : Reserved	N/A	N/A
	7-9	Reserved	N/A	N/A
	10	Memory Test Results (0=ok, 1=failure) Bit 0 : Bad Boot S/W Checksum Bit 1 : Bad Operational S/W Checksum Bit 2-4: FLASH Error Code if different of 000 : Receiver can not be reprogrammed Bit 5-7: Reserved	N/A	N/A
	11	EEPROM Status **Bit 0: Link error** **Bit 1: Memory location error**	N/A	N/A
	12	Primary Port (UART) results Bit 0 : UART not ready or UART busy Bit 1 : TX not full flag error Bit 2 : No Data received during internal loop tests Bit 3 : Framing or Parity error Bit 4 : RX not full flag error **Bit 5-7 : Reserved**	N/A	N/A
	13	Auxiliary Port (UART) results **(see byte 12 description)**	N/A	N/A

MESSAGE	BYTE	DESCRIPTION	UNIT	TYPE
	14	RTC results **Bit 0 :Serial link error** **Bit 1: Date error** **Bit 2: Time error** **Bit 3: Data retention** Bit 5-7 : Reserved	N/A	N/A
51 (Cont'd)	15	RF Test Results Bit 0: MAG LO limit error Bit 1: MAG HI limit error Bit 2: SIGN LO limit error Bit 3: SIGN HI limit error Bit 4: I_Q Test error Bit 5: PLL lock not valid Bit 6-7: Reserved.	N/A	N/A
	16	Global Correlator test results #1 Bit 0 : Channel 0 error in I&Q test … Bit 7 : Channel 7 error in I&Q test	N/A	N/A
	17	Global Correlator test results #2 Bit 0 : Channel 0 error in I&Q test … Bit 7 : Channel 7 error in I&Q test	N/A	N/A
	18	Global Correlator test results #3 Bit 0 : Channel 9 error in I&Q test Bit 1 : Channel 10 error in I&Q test Bit 2 : Channel 11 error in I&Q test Bit 3 : Channel 12 error in I&Q test Bit 4 : Channel 9 error in Measurement test Bit 5 : Channel 10 error in Measurement test Bit 6 : Channel 11 error in Measurement test Bit 7 : Channel 12 error in Measurement test	N/A	N/A
	19-30	Reserved		
	31	**Serial port #3 (UART) results (see byte 12 description)**	N/A	N/A
	32-40	Reserved		