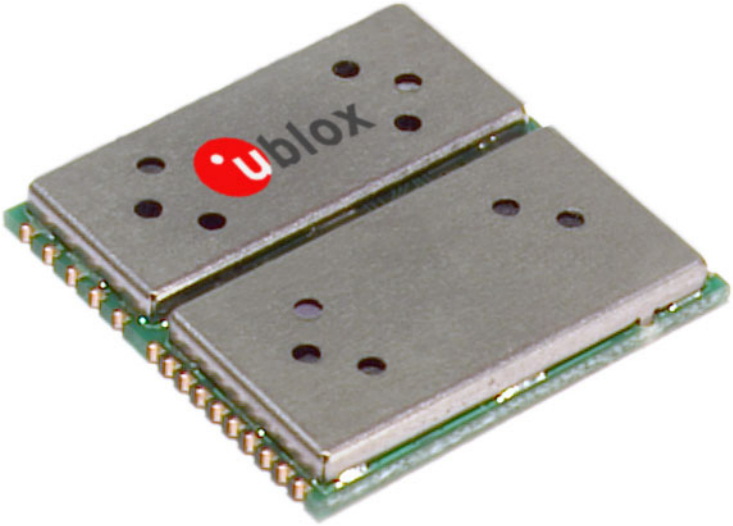
u-blox AG
Zürcherstrasse 68
8800 Thalwil
Switzerland
www.u-blox.com

Phone +41 1722 7444
Fax +41 1722 7447
info@u-blox.com

TIM-LP
GPS Receiver Macro Component

Data Sheet



Abstract

This document describes the features and specifications of the TIM-LP macro-component, an ultra-low power GPS receiver macro-component. Based on the ANTARIS™ GPS technology, it offers best GPS performance at very low power.

your position is our focus

Data Sheet

Title	TIM-LP		
Subtitle	GPS Receiver Macro Component		
Doc Type	Data Sheet		
Doc Id	GPS.G3-MS3-02010-A		
Revision Index	**Date**	**Name**	**Status / Comments**
Initial Version	2. Apr 03	GzB	First release
A	16. Jun 03	GzB	Updated electrical and performance characteristics

For most recent documents, please visit www.u-blox.com

Contents

1 Functional Description

1.1 Overview

The TIM-LP is an ultra-low power GPS receiver macro component. Based on the ANTARIS™ GPS positioning engine jointly developed by Atmel and u-blox, it offers excellent GPS performance. The TIM-LP can run custom applications on the on-board processor and offers two 3V serial ports and a set of configurable 3V input / output ports. With its innovative packaging technology the TIM-LP GPS receiver is the ideal solution for a broad range of high-volume applications.

The TIM-LP GPS receiver macro component is another milestone in the miniaturization of GPS receiver modules. Innovative packaging technology has opened the door for a thin and compact GPS receiver unique to the market. The TIM-LP macro component is SMT solderable and can be handled by standard pick-and-place equipment. This allows a fully automatic assembly process. The height of 3mm (~120mil) and the size of 25.4 x 25.4 mm (1" x 1") make it the ideal GPS solution for applications with stringent space requirements.

1.2 Block Diagram

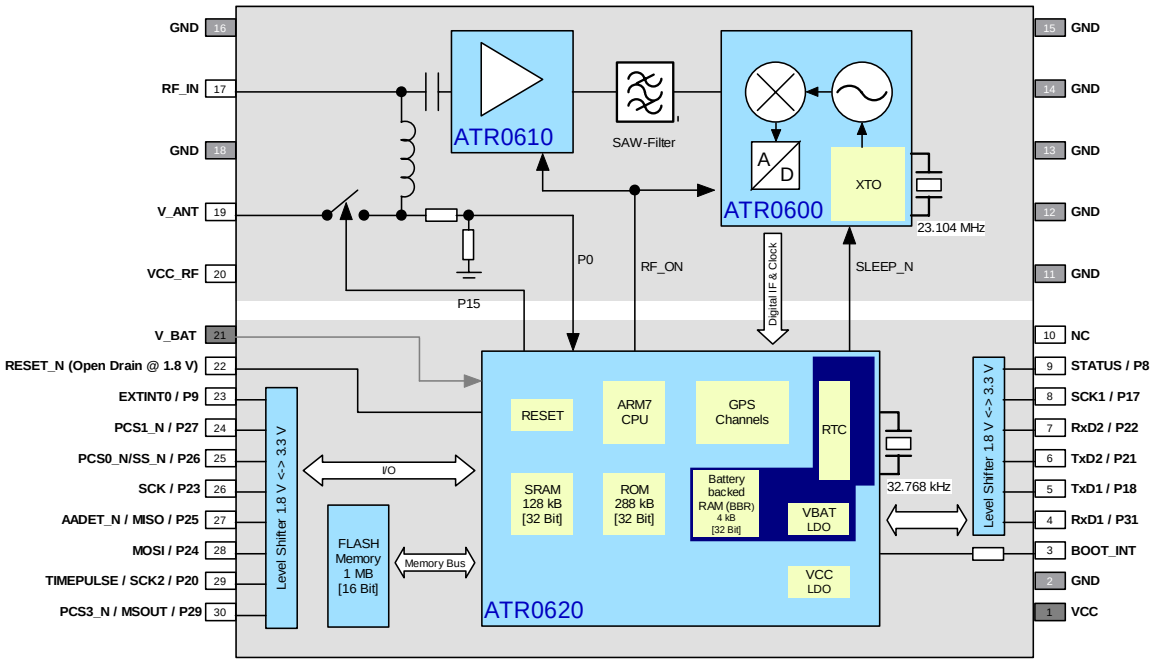


Figure 1: Block Diagram

1.3 Benefits

- Fully self-contained GPS receiver (PVT output)
- Ultra low power consumption
- Excellent GPS performance
  - Excellent navigation accuracy
  - Fast Time-to-first-fix
- Macro component
  - Very compact design
  - Automatic pick and place assembly
  - Reflow solderable
- High Flexibility
  - Extensively configurable
  - Integration of custom application code
- Fully EMI shielded
- Passive and active antenna support

1.4 Features

- 16 channel GPS receiver
- 8192 simultaneous time-frequency search bins
- 4 Hz position update rate
- Based on the ANTARIS™ GPS Technology
  - ATR0600 RF front-end IC
  - ATR0620 Baseband IC with integrated ARM7TDMI
  - ATR0610 Low Noise Amplifier
- 8 MBit FLASH memory
- Available resources for custom applications
  - SRAM
  - FLASH
  - GPIOs
  - SPI
  - CPU power
- FixNOW™ power saving mode ideally suited for mobile and battery-driven tracking applications
- Operating voltage 2.7…3.3 V
- Battery supply pin for internal backup memory and real time clock
- Industrial operating temperature range –40…85°C
- Small size
  - Size 25.4mm x 25.4mm
  - Height 3mm
  - Weight 3g

1.5 Operating Modes

The ANTARIS ™ GPS Technology defines the following Operating Modes:

Operating Modes	Description
Continuous Tracking Mode (CTM)	The Continuous Tracking Mode is configured for optimal position accuracy. This mode is optimized for power consumption based on the ANTARIS™ Autonomous Power Management (APM) saving as parts of the receiver are switched off when they are not required; also the CPU clock speed is reduced when the CPU is not loaded. There is no need for a user to configure this mode as it is built into the architecture of the module.
Power Saving Modes	
FixNOW™ (FXN)	FixNOW™ Mode allows an application a navigation solution on request. It includes additional Power Saving Functions and is the best mode for any Mobile, Tracking Unit application where low power consumption requirements are primary consideration. This mode can be configured to meet application requirements.

Table 1: Operating Modes

For specification of the various protocols see the *System Integration Manual [1].*

1.6 Protocols

The TIM-LP supports different serial protocols. These can be assigned to any serial interface port.

Protocol	Type	Runs on
NMEA	Input/output, ASCII, 0183, 2.3	All Serial ports
UBX	Input/output, binary, u-blox proprietary	All Serial ports
RTCM	Input, message 1,2,3,9	All Serial ports

Table 2: Available Protocols

For specification of the various protocols see the *Protocol Specification [2].*

1.7 Available Resources

Following resources are available for user-specific applications. The ANTARIS™ SCKit is required to utilize them.

Resources		Characteristics
Processor	ARM7TDMI running at 23 MHz	3.75 - 9 MIPS [1] @ 1 Hz navigation update rate
Memory	Flash EPROM SRAM	500 kB 8 kB
Interfaces	USARTs, synchronous and asynchronous operation SPI (Master and slave operation)	2 interfaces, 3 V levels 3 chip-select signals, 3 V levels
Digital I/Os	9 GPIOs, 1 GPIO, interrupt-capable	3 V levels 3 V levels (Pin EXTINT0 / P9)

Table 3: Available Resources

[1] "VAX MIPS", calculated using Dhrystone, available for user code

2 Performance Specification

Parameter	Specification	
Receiver Type		L1 frequency, C/A Code, 16-Channels 8192 search bins
Max Update Rate		4 Hz
Accuracy (Selective Availability off)	Position Position DGPS	3 m CEP[2] <2 m CEP[3]
Acquisition	Cold Start Warm Start Hot Start	41.5 s (typical) 33 s (typical) <3.5 s (typical)
Signal Reacquisition		<1 s
Sensitivity (Acquisition)	Fast acquisition mode Normal mode High sensitivity mode	-131 dBm (typical) -134 dBm (typical) -137 dBm (typical)
Sensitivity (Tracking)	Fast acquisition mode Normal mode High sensitivity mode	-139 dBm (typical) -141 dBm (typical) -141 dBm (typical)
Timepulse Accuracy		± 100ns (maximum) ± 50ns (RMS)
Dynamics		≤ 4 g
Operational Limits		COCOM restrictions

Table 4: Performance Specification

[2] CEP = Circular Error Probability: The radius of a horizontal circle, centered at the antenna's true position, containing 50% of the fixes.
[3] Depends on accuracy of DGPS system

3 Mechanical Specification

3.1 Dimensions

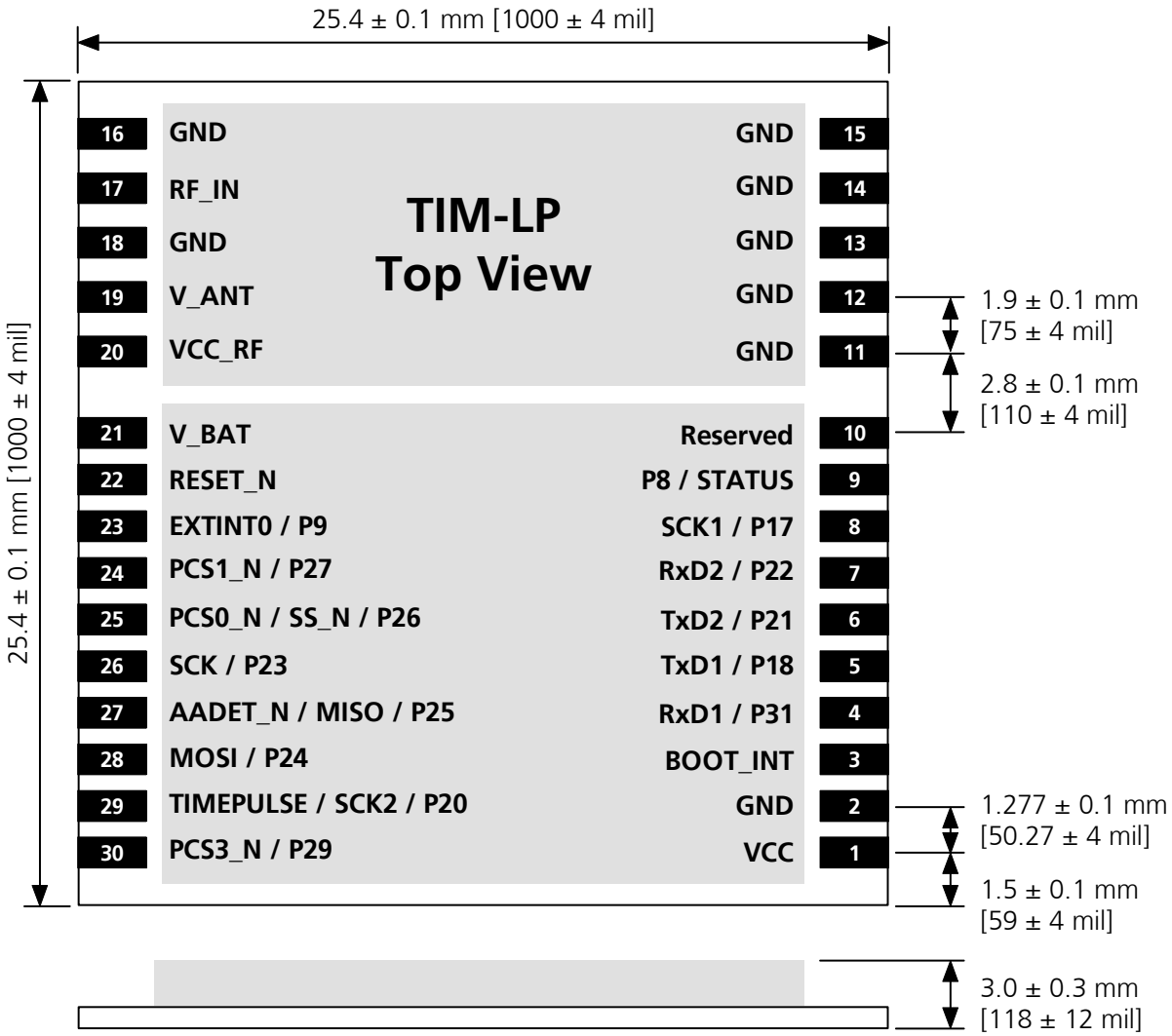


Figure 2: TIM-LP Dimensions

3.2 Specification

Parameter	Specification	Tolerance	Unit
Length	25.4	±0.1	mm
Width	25.4	±0.1	mm
Thickness	3.0	±0.3	mm
Pitch RF pins	1.9	±0.1	mm
Pitch Digital pins	1.277	±0.1	mm
Weight	3		g

Table 5: Mechanical Specification

3.3 Pinout

Standard Function				Alternate Functions[4]			Remarks
No	Name	I/O	Description	Name	I/O	Description	
1	VCC	I	Supply voltage				
2	GND	I	Ground				
3	BOOT_INT	I	Boot mode				Leave open if not used (normal operation)
4	RxD1	I	Serial Port 1	P31	I/O	GPIO	Pull up if not used
5	TxD1	O	Serial Port 1	P18	I/O	GPIO	Leave open if not used
6	TxD2	O	Serial Port 2	P21	I/O	GPIO	Leave open if not used
7	RxD2	I	Serial Port 2	P22	I/O	GPIO	Pull up if not used
8	P17	I/O	GPIO	SCK1	I/O	synch. serial port 1 clock	Default config. to input with internal pull-up, leave open if not used
9	STATUS	O	GPS Status	P8	I/O	GPIO	Default config. to output, leave open if not used
10	Reserved		Not connected				Leave open if not used
11 – 16	GND	I	Ground				
17	RF_IN	I	GPS signal input				Apply no DC through this pin
18	GND	I	Ground				
19	V_ANT	I	Antenna Bias voltage				Connect to GND if not used
20	VCC_RF	O	Output Voltage RF section				May be connected to V_ANT
21	V_BAT	I	Backup voltage supply				Connect to GND if not used
22	RESET_N	I/O	Reset (Active low)				Leave open if not used
23	EXTINT0	I	External Interrupt Pin	P9	I/O	GPIO	Default config. to input with internal pull-up, leave open if not used
24	P27	I/O	GPIO	PCS1_N	O	SPI Chip Select 1	Default config. to input with internal pull-up, leave open if not used
25	P26	I/O	GPIO	SS_N PCS0_N	I O	SPI Slave Select SPI Chip Select 0	Default config. to input with internal pull-up, leave open if not used
26	P23	I/O	GPIO	SCK	I/O	SPI clock	Default config. to input with internal pull-up, leave open if not used
27	AADET_N	I	Active Antenna Detect	P25 MISO	I/O I/O	GPIO SPI MISO	Default config. to input with internal pull-up, leave open if not used
28	P24	I/O	GPIO	MOSI	I/O	SPI MOSI	Default config. to input with internal pull-up, leave open if not used
29	TIMEPULSE	O	Timepulse signal	P20 SCK2	I/O I/O	GPIO Synch. serial port 2 clock	Default config. to output, leave open if not used
30	P29	I/O	GPIO[5]	PCS3_N	O	SPI Chip Select 3	Default config. to input with internal pull-up, leave open if not used

Table 6: Signals and Module Interface

[4] ANTARIS™ Software Customization Kit needed to explore alternate functions
[5] Standard software allows this pin to be connected to GND externally

4 Electrical Specification

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power Supply (VCC and V_BAT)				
Power supply voltage	Vcc	-0.3	3.6	V
Input Pins				
Input pin voltage (all except RESET_N)	Vin	-0.3	Vcc + 0.3	V
Input pin voltage of RESET_N	Vin_reset	-0.3	1.95	V
Voltage Supply output for Active Antenna and RF Section				
VCC_RF output current	Iccrf		50	mA
RF Input				
Antenna bias voltage (applied via V_ANT)	Vant	0	8	V
Antenna bias current (applied via V_ANT)	Iant		100	mA
Input power at RF_IN (source impedance 50Ω, continuous wave)	Prfin		-17	dBm
Environment				
Storage temperature	Tstg	-40	125	°C

Table 7: Absolute Maximum Ratings

! **Warning** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

4.2 Operating Conditions

Parameter[6]	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Power supply voltage	Vcc		2.7		3.3	V
Power supply voltage ripple	Vcc_PP				50	mV
Sustained supply current [7]	Icc	Vcc = 3.0 V		56		mA
Peak supply current [8]	Iccp	Vcc = 3.3 V			125	mA
Sleep mode current	Iccs	Vcc = 3.0 V		1.6		mA
Backup battery voltage	Vbat		1.95		3.6	V
Backup battery current	Ibat	Vbat = 3.3 V		16	40 (prelim.)	µA
Digital I/O (All signals except RESET_N)						
Input pin voltage range	Vin		0V		Vcc	V
Input pin Low voltage	Vin_low				0.15	V
Input pin high voltage	Vin_high		Vcc – 0.4			V
Output pin voltage range	Vout		0V		Vcc	V
Output pin low voltage	Vout_low	Iout < 1mA (sink)			0.4	V
Output pin high voltage	Vout_high	Iout < 20µA (source)	0.67 × Vcc			V
Output pin current at low voltage	Iout_low	Vout_low = 0.4 V			1	mA
Output pin current at high voltage	Iout_high	Vout_high = 0.67 x Vcc			20	µA
RESET_N Input						
Input Pin voltage range	VinR		0		1.8	V
Input pin low voltage	Vin_lowR				0.45	V
Input pin high voltage	Vin_highR		1.4			V
BOOT_INT Pin						
Input Pin voltage range	VinB		0		Vcc	V
Input pin low voltage	Vin_lowB				0.4	V
Input pin high voltage	Vin_highB		2.7	Vcc		V
RF input						
Input power	Prfin				-61	dBm
V_ANT antenna bias voltage (must connect to ground if not used)	Vant		1.8		8	V
Antenna bias voltage drop	Vant_drop	Iant=10mA			50	mV
VCC_RF voltage	Vccrf			Vcc – 0.1		V
Environment						
Operating temperature	Topr		-40		85	°C

Table 8: Operating Conditions

Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability. The technical data apply to products where standard ANTARIS™ firmware is running.

[6] All specification are at an ambient temperature of 25°C.
[7] Average current drawn during Continuous Tracking Mode with 1 Hz update rate, using 6 satellites for tracking and navigation. Use this figure to determine required battery capacity
[8] Peak current drawn during initial acquisition phase. Use this figure to dimension maximum current capability of power supply

5 Environmental Specification

Detailed description of the test series:

Test		Standard
Visual inspection		IPC-A-610 "Acceptability of electronic assemblies" I.T.R.I. Publication No. 700 IPC-SM-840B Class 2.
Thermal shock	-40°C...+125°C	IEC 68-2-14
Function at various temperatures	-40°C/2 hours; RT/2 hours; +85°C/2 hours; function tests at stable temperature	IEC 68-2-1 and IEC 68-2-2
Lifespan test	+85°C/1000 hours; function	IEC 68-2-2
Damp heat, cyclic	+25°C...+55°C; >90% rH	IEC 68-2-30
Vibration Shock	10-500 Hz; 2 hours/axis; 5g; function 30g/11ms (halfsine); 3 Shock/axis; no function	IEC 68-2-6 IEC 68-2-27
Metallographic investigations		IPC-QE-650

Note: This specification is preliminary and yet subject to confirmation.

Table 9: Environmental Specification

6 Product Lineup

6.1 Default Settings

Interface	Settings
Serial Port 1 Output	9600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, VTG, ZDA, TXT** Additional messages can be activated with appropriate input messages.
Serial Port 1 Input	9600 Baud, 8 bits, no parity bit, 1 stop bit, Autobauding disabled Automatically accepts following protocols without need of explicit configuration: **UBX, NMEA, RTCM** The GPS receiver supports interleaved UBX and NMEA messages.
Serial Port 2 Output	57600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only following UBX and no NMEA messages have been activated at start-up: **NAV-POSLLH, NAV-SOL, NAV-SVINFO, NAV-STATUS** MON-IO, MON-SCHD, MON-TXBUF, INF-Warning, INF-Error, INF-Notice Additional messages can be activated with appropriate input messages.
Serial Port 2 Input	57600 Baud, 8 bits, no parity bit, 1 stop bit, Autobauding disabled Automatically accepts following protocols without need of explicit configuration: **UBX, NMEA, RTCM** The GPS receiver supports interleaved UBX and NMEA messages.
TIMEPULSE	1 pulse per second, synchronized at rising edge, pulse length 100ms

Table 10: Available Protocols

6.2 Ordering Information

Ordering No.	Product	
TIM-LP-0-000-0	TIM-LP	TIM-LP GPS Receiver Macro Component Single samples
TIM-LP-0-000-1	TIM-LP	TIM-LP GPS Receiver Macro Component Tape on reel 100pcs
TIM-LP-0-000-5	TIM-LP	TIM-LP GPS Receiver Macro Component Tape on reel 500pcs

Table 11: Ordering Information

Parts of this product are patent protected.

Related Documents

[1] TIM-LC, TIM-LF, TIM-LP System Integration Manual, Docu. No GPS.G3-MS3-01001

[2] ANTARIS™ GPS Technology - Protocol Specification, Docu. No GPS.G3-X-03002

[3] ANTARIS™ EvalKit User's Guide, Docu. No GPS.G3-EK-02001

All these documents are available on our homepage (http://www.u-blox.com).

Contact

For further info, please contact us:

Headquarters

u-blox AG
Zuercherstrasse 68
CH-8800 Thalwil
Switzerland

Phone: +41 1 722 74 44
Fax: +41 1 722 74 47
E-mail: info@u-blox.com
www.u-blox.com

Subsidiaries

u-blox Deutschland GmbH
Berliner Ring 89
D-64625 Bensheim
Germany

Phone: +49 (0) 6251 17566-0
Fax: +49 (0) 6251 17566-11
E-mail: info_de@u-blox.de
www.u-blox.de

Technical Support:

Phone: +41 1 722 74 74
E-mail: support_de@u-blox.de

u-blox Europe Ltd.
Barham Court, Teston
Maidstone, Kent ME18 5BZ
United Kingdom

Phone: +44 1622 618628
Fax: +44 1622 618629
E-mail: info_uk@u-blox.co.uk
www.u-blox.co.uk

Technical Support:

Phone: +44 1622 618628
E-mail: support_uk@u-blox.co.uk

u-blox Asia Pacific Ltd.
Suite A, 8/F, Block 7
398 Castle Peak Road
Tsuen Wan, Hong Kong

Phone: +852-2940-0085
Fax: +852-2615-2285
E-mail: info_ap@u-blox.com
www.u-blox.com

u-blox Beijing Office
c/o Beijing Eastar Technology Co., Ltd.
Suite Z, No. 10
Haidian District, Beijing 100088
P.R. China

Phone: +86-10-6226-2091
Fax: +86-10-6223-4821
E-mail: info_ap@u-blox.com
www.u-blox.com

Technical Support:

Phone: +86-10-6226-2091
E-mail: support_ap@u-blox.com

u-blox America, Inc.
13800 Coppermine Road
Herndon, VA 20171
USA

Phone: +1 (703) 234 5290
Fax: +1 (703) 234 5770
E-mail: info_us@u-blox.com
www.u-blox.us

Technical Support:

Phone: +1 (703) 234 5290
E-mail: support_us@u-blox.us