The ATM Forum
Technical Committee

Conformance Abstract Test Suite for the SSCOP for UNI 3.1

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1. Introduction

This document provides the conformance abstract test suite for the Service Specific Connection Oriented Protocol (SSCOP) of the ATM Forum UNI Specification, Version 3.1[1] and ITU Recommendation Q.2110[2]. This test suite aligns with the principles defined in OSI Conformance Testing Methodology and Framework, ISO 9646 Parts 1-2[3][4]. The test scripts are written in the internationally standardized Tree and Tabular Combined Notation, TTCN, defined in ISO 9646 Part 3[5].

The Protocol Implementation eXtra Information for Testing (PIXIT) proforma is provided in Annex A. The PIXIT questionnaire needs to be completed for a particular System equipment (Implementation Under Test) prior to conformance testing.

1.1 Definition of Terminologies

This test suite uses valid, invalid, and inopportune Protocol Data Units (PDUs) to test the IUT behavior. These terms are defined as follows:

1.1.1 Valid PDU

A valid PDU is an expected PDU which arrives at the correct state or phase and does not belong to any of the categories listed under invalid PDUs.

1.1.2 Invalid PDU

An invalid PDU is a PDU which is syntactically incorrect.

1.1.3 Inopportune PDU

An inopportune PDU is a syntactically valid PDU arriving at a time (IUT's state) when it should be considered irrelevant by the IUT.

2. Methodology

This conformance test suite has been developed as described in ISO/IEC International Standard 9646-1 and 2 [3][4]. A testing matrix has been developed after study of the SSCOP Specification and a selection of the appropriate test groups. The remote single layer embedded (RSE) test method has been selected, as shown below, and test cases have been generated. The notation used in this abstract test suite is the Tree and Tabular Combined Notation (TTCN) as described in ISO/IEC IS 9646-3[5]. This version of the SSCOP conformance test suite uses sequential TTCN, but conversion into concurrent TTCN will bring some improvement in the test case description and implementation.

3. Test Configuration

The test configuration used for testing SSCOP is given in Figure 1. The system under test (SUT) includes the SSCOP of the IUT, the Service Specific Convergence Function (SSCF), and a higher layer, such as Q.2931. For the remote, single layer testing for the SSCOP, the tester has only one Point of Control and Observation (PCO).

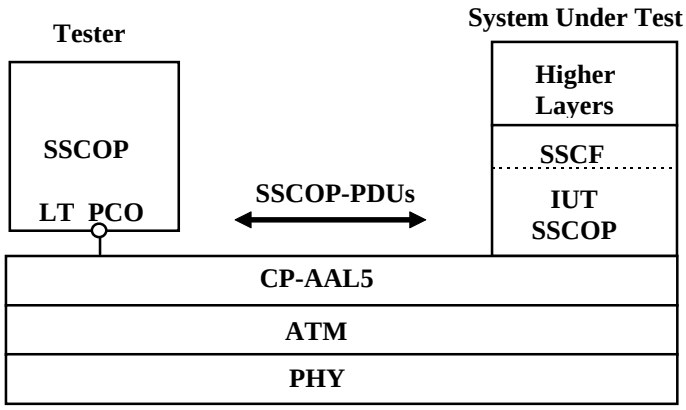

Figure 1. Example Configuration for SSCOP testing using RSE test method

4. Test Suite Structure

For the SSCOP test suite, there are two major groups, Protocol Capabilities (PC) and System Parameters (SP) group. In the PC group, there is a subgroup for each of the SSCOP states (state_x, where x = 1 - 10), each having a subgroup for valid, invalid, and inopportune tests, as defined in the Definitions of Terminologies section above. The System Parameters group includes tests for SSCOP system parameters (e.g., timers and counters).

The test structure for the SSCOP ATS is:

```
- SSCOP/
  - Protocol Capabilities (PC)
      - state_1
            - valid
            - invalid
            - inopportune
      - state_2
            - valid
            - invalid
            - inopportune
      :
      :
      - state_10
            - valid
            - invalid
            - inopportune
- System Parameters (SP)
      - Timer
      - Parm
```

5. Assumptions on the Capabilities of the Testers

5.1 Error Generation

The tester is asked to generate errors in some test cases, to allow for testing of error conditions.

6. Timers

Several timers have been defined for testing. These timers are:

(1) T_Wait is used to limit the test time waiting for "no response" from the IUT.
(2) T_Opr is used to allow sufficient time for a test operator to initiate some test action. This timer is used in conjunction with an "Implicit send" for test coordination.

These timers are not used to verify the exact timing of an implementation, but to limit the time which the test should wait for a PDU or to limit the total duration of the test.

7. Abbreviations

ATM	Asynchronous Transfer Mode
ATS	Abstract Test Suite
ISO/IEC	International Organization for Standardization/International Electrotechnical Commission
IUT	Implementation Under Test
PCO	Point of Control and Observation
PDU	Protocol Data Unit
PHY	Physical Layer
PICS	Protocol Implementation Conformance Statement
PIXIT	Protocol Implementation Extra Information for Testing
RSE	Remote Single Layer Embedded test method
SSCF	Service Specific Convergence Function
SSCOP	Service Specific Connection Oriented Protocol
SUT	System Under Test
TTCN	Tree and Tabular Combined Notation
UNI	User-Network Interface

8. References

[1] ATM Forum User-Network Interface (UNI) Specification 3.1.

[2] ITU Recommendation Q.2110, B-*ISDN - ATM Adaptation Layer - Service Specific Connection Oriented Protocol (SSCOP).*

[3] ISO/IEC 9646-1 *"Information Technology - Open Systems Interconnection - Conformance testing methodology and framework - Part 1: General Concepts", 1991.*

[4] ISO/IEC 9646-2 *"Information Technology - Open Systems Interconnection - Conformance testing methodology and framework - Part 2: Abstract test suite specification", 1991.*

[5] ISO/IEC 9646-3 *"Information Technology - Open Systems Interconnection - Conformance testing methodology and framework - Part 3: The tree and tabular combined notation", 1991.*

Annex A

Protocol Implementation eXtra Information for Testing (PIXIT) Proforma For SSCOP

IUT

Name:

Version:

Machine Configuration:

Operating System Identification:

IUT Identification:

PICS Reference for IUT:

Limitations of the IUT :

Timers

1. Enter the value for the timer that is used when no response is expected from the IUT.

_____

2. Enter the value for the timer that is long enough to allow test operator intervention.

_____

General

3. Can the IUT, at state 1, be forced to send BGN PDU when requested by test operator?

_____

4. Can the IUT, at state 4, be forced to send BGN PDU when requested by test operator?

_____

5. Can the IUT, at state 2, be forced to send END PDU when requested by test operator?

_____

6. Can the IUT, at state 5, be forced to send END PDU when requested by test operator?

_____

7. Can the IUT, at state 10, be forced to send END PDU when requested by test operator?

_____

8. Can the IUT, at state 10, be forced to send RS PDU when requested by test operator?

_____

9. Can the IUT, at state 10, be forced to send POLL PDU when requested by test operator?

_____

10. Can the IUT, at state 10, be forced to send SD PDU when requested by test operator?

_____

Annex B

Abstract Test Suite

I

Test Suite Overview

Test Suite Structure

Suite Name : ATMF_SSCOP
Standards Ref : ITU−T Recommendation Q.2110, Service Specific Connection Oriented Protocol(SSCOP)
PICS Ref : ITU−T Recommendation Q.2110, Annex B
PIXIT Ref : ATM Forum/af−test−0067.000, Conformance ATS for the SSCOP for UNI 3.1, Annex A
Test Method(s) : Remote Single Layer Embedded Test Method
Comments :

Detailed Comments :

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PC/STATE_1/VAL/	S1_V_A1		Verify that the IUT generates the BGN PDU on demand at state 1.	91
PC/STATE_1/VAL/	S1_V_P1		Verify that the IUT sends a BGREJ PDU on reception of retransmitted BGN PDU.	91
PC/STATE_1/VAL/	S1_V_P2		Verify that the IUT goes to state 3 on reception of BGN PDU at state 1.	92
PC/STATE_1/VAL/	S1_V_P5		Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 1.	93
PC/STATE_1/VAL/	S1_V_P6		Verify that the IUT ignores a ENDAK PDU and remains at state 1.	93
PC/STATE_1/VAL/	S1_V_P16		Verify that the IUT accpets a UD PDU at state 1.	94
PC/STATE_1/VAL/	S1_V_P17		Verify that the IUT accpets a MD PDU at state 1.	94
PC/STATE_1/INV/	S1_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 1.	95
PC/STATE_1/INV/	S1_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 1.	96
PC/STATE_1/INV/	S1_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 1.	96
PC/STATE_1/INV/	S1_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 1.	97
PC/STATE_1/INV/	S1_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 1.	97
PC/STATE_1/INV/	S1_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 1.	98
PC/STATE_1/INV/	S1_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 1.	98
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PC/STATE_1/INV/	S1_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 1.	100
PC/STATE_1/INV/	S1_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 1.	101
PC/STATE_1/INV/	S1_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 1.	102
PC/STATE_1/INV/	S1_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 1.	103
PC/STATE_1/INV/	S1_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 1.	104
PC/STATE_1/INV/	S1_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 1.	105
PC/STATE_1/INV/	S1_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 1.	106
PC/STATE_1/INV/	S1_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 1.	107
PC/STATE_1/INV/	S1_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 1.	108

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_1/INV/	S1_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 1.	109
PC/STATE_1/INV/	S1_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 1.	110
PC/STATE_1/INV/	S1_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 1.	111
PC/STATE_1/INV/	S1_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 1.	112
PC/STATE_1/INV/	S1_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 1.	113
PC/STATE_1/INV/	S1_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 1.	114
PC/STATE_1/INV/	S1_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 1.	115
PC/STATE_1/INV/	S1_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 1.	116
PC/STATE_1/INV/	S1_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 1.	117

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PC/STATE_1/INV/	S1_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 1.	119
PC/STATE_1/INV/	S1_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 1.	120
PC/STATE_1/INV/	S1_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 1.	121
PC/STATE_1/INV/	S1_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 1.	122
PC/STATE_1/INOP/	S1_IO_P3		Verify that the IUT sends a END PDU on reception of a BGAK PDU at state 1.	122
PC/STATE_1/INOP/	S1_IO_P4		Verify that the IUT ignores a BGREJ PDU and remains at state 1.	123
PC/STATE_1/INOP/	S1_IO_P8		Verify that the IUT sends a END PDU on reception of a RS PDU at state 1.	123
PC/STATE_1/INOP/	S1_IO_P9		Verify that the IUT sends a END PDU on reception of a RSAK PDU at state 1.	124
PC/STATE_1/INOP/	S1_IO_P10		Verify that the IUT sends a END PDU on reception of a ER PDU at state 1.	124
PC/STATE_1/INOP/	S1_IO_P11		Verify that the IUT sends a END PDU on reception of a ERAK PDU at state 1.	125
PC/STATE_1/INOP/	S1_IO_P12		Verify that the IUT sends a END PDU on reception of a SD PDU at state 1.	125
PC/STATE_1/INOP/	S1_IO_P13		Verify that the IUT sends a END PDU on reception of a POLL PDU at state 1.	126
PC/STATE_1/INOP/	S1_IO_P14		Verify that the IUT sends a END PDU on reception of a STAT PDU at state 1.	126

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PC/STATE_1/INOP/	S1_IO_P15		Verify that the IUT sends a END PDU on reception of a USTAT PDU at state 1.	127
PC/STATE_2/VAL/	S2_V_A3		Verify that the IUT generates the END PDU on demand at state 2.	127
PC/STATE_2/VAL/	S2_V_P1		Verify that the IUT ignores a retransmitted BGN PDU at state 2.	128
PC/STATE_2/VAL/	S2_V_P2		Verify that the IUT sends a BGAK PDU on reception of BGN PDU and goes to state 10.	128
PC/STATE_2/VAL/	S2_V_P3		Verify that the IUT goes to state 10 on reception of BGAK PDU at state 2.	129
PC/STATE_2/VAL/	S2_V_P4		Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 2.	130
PC/STATE_2/VAL/	S2_V_P5		Verify that the IUT ignores a END PDU and remains at state 2.	130
PC/STATE_2/VAL/	S2_V_P6		Verify that the IUT ignores a ENDAK PDU and remains at state 2.	131
PC/STATE_2/VAL/	S2_V_P8		Verify that the IUT ignores a RS PDU and remains at state 2.	132
PC/STATE_2/VAL/	S2_V_P9		Verify that the IUT ignores a RSAK PDU and remains at state 2.	133
PC/STATE_2/VAL/	S2_V_P10		Verify that the IUT ignores a ER PDU and remains at state 2.	134
PC/STATE_2/VAL/	S2_V_P11		Verify that the IUT ignores a ERAK PDU and remains at state 2.	135
PC/STATE_2/VAL/	S2_V_P12		Verify that the IUT ignores a SD PDU and remains at state 2.	135
PC/STATE_2/VAL/	S2_V_P13		Verify that the IUT ignores a POLL PDU and remains at state 2.	136
PC/STATE_2/VAL/	S2_V_P14		Verify that the IUT ignores a STAT PDU and remains at state 2.	137
PC/STATE_2/VAL/	S2_V_P15		Verify that the IUT ignores a USTAT PDU and remains at state 2.	138
PC/STATE_2/VAL/	S2_V_P16		Verify that the IUT accpets a UD PDU at state 2.	139

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PC/STATE_2/INV/	S2_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 2.	140
PC/STATE_2/INV/	S2_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 2.	141
PC/STATE_2/INV/	S2_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 2.	141
PC/STATE_2/INV/	S2_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 2.	142
PC/STATE_2/INV/	S2_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 2.	142
PC/STATE_2/INV/	S2_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 2.	143
PC/STATE_2/INV/	S2_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 2.	143
PC/STATE_2/INV/	S2_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 2.	144
PC/STATE_2/INV/	S2_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 2.	145
PC/STATE_2/INV/	S2_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 2.	146
PC/STATE_2/INV/	S2_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 2.	147

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PC/STATE_2/INV/	S2_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 2.	149
PC/STATE_2/INV/	S2_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 2.	150
PC/STATE_2/INV/	S2_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 2.	151
PC/STATE_2/INV/	S2_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 2.	152
PC/STATE_2/INV/	S2_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 2.	153
PC/STATE_2/INV/	S2_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 2.	154
PC/STATE_2/INV/	S2_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 2.	155
PC/STATE_2/INV/	S2_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 2.	156

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
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PC/STATE_2/INV/	S2_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 2.	158
PC/STATE_2/INV/	S2_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 2.	159
PC/STATE_2/INV/	S2_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 2.	160
PC/STATE_2/INV/	S2_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 2.	161
PC/STATE_2/INV/	S2_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 2.	162
PC/STATE_2/INV/	S2_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 2.	163
PC/STATE_2/INV/	S2_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 2.	164
PC/STATE_2/INV/	S2_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 2.	165

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PC/STATE_2/INV/	S2_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 2.	167
PC/STATE_4/VAL/	S4_V_A1		Verify that the IUT generates the BGN PDU on demand at state 4.	167
PC/STATE_4/VAL/	S4_V_P1		Verify that the IUT sends a BGAK and END PDU on reception of retransmitted BGN PDU at state 4.	168
PC/STATE_4/VAL/	S4_V_P2		Verify that the IUT goes to state 3 on reception of BGN PDU at state 4.	169
PC/STATE_4/VAL/	S4_V_P3		Verify that the IUT ignores a BGAK PDU and remains at state 4.	169
PC/STATE_4/VAL/	S4_V_P4		Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 4.	170
PC/STATE_4/VAL/	S4_V_P5		Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 4.	170
PC/STATE_4/VAL/	S4_V_P6		Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 4.	171
PC/STATE_4/VAL/	S4_V_P8		Verify that the IUT ignores a RS PDU and remains at state 4.	172
PC/STATE_4/VAL/	S4_V_P9		Verify that the IUT ignores a RSAK PDU and remains at state 4.	173
PC/STATE_4/VAL/	S4_V_P10		Verify that the IUT ignores a ER PDU and remains at state 4.	174
PC/STATE_4/VAL/	S4_V_P11		Verify that the IUT ignores a ERAK PDU and remains at state 4.	175
PC/STATE_4/VAL/	S4_V_P12		Verify that the IUT ignores a SD PDU and remains at state 4.	175
PC/STATE_4/VAL/	S4_V_P13		Verify that the IUT ignores a POLL PDU and remains at state 4.	176
PC/STATE_4/VAL/	S4_V_P14		Verify that the IUT ignores a STAT PDU and remains at state 4.	177

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PC/STATE_4/VAL/	S4_V_P16		Verify that the IUT accpets a UD PDU at state 4.	179
PC/STATE_4/VAL/	S4_V_P17		Verify that the IUT accpets a MD PDU at state 4.	179
PC/STATE_4/INV/	S4_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 4.	180
PC/STATE_4/INV/	S4_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 4.	181
PC/STATE_4/INV/	S4_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 4.	181
PC/STATE_4/INV/	S4_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 4.	182
PC/STATE_4/INV/	S4_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 4.	182
PC/STATE_4/INV/	S4_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 4.	183
PC/STATE_4/INV/	S4_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 4.	183
PC/STATE_4/INV/	S4_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 4.	184
PC/STATE_4/INV/	S4_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 4.	185
PC/STATE_4/INV/	S4_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 4.	186

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PC/STATE_4/INV/	S4_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 4.	188
PC/STATE_4/INV/	S4_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 4.	189
PC/STATE_4/INV/	S4_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 4.	190
PC/STATE_4/INV/	S4_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 4.	191
PC/STATE_4/INV/	S4_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 4.	192
PC/STATE_4/INV/	S4_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 4.	193
PC/STATE_4/INV/	S4_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 4.	194
PC/STATE_4/INV/	S4_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 4.	195

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PC/STATE_4/INV/	S4_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 4.	199
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PC/STATE_4/INV/	S4_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 4.	201
PC/STATE_4/INV/	S4_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 4.	202
PC/STATE_4/INV/	S4_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 4.	203
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PC/STATE_4/INV/	S4_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 4.	207
PC/STATE_5/VAL/	S5_V_A3		Verify that the IUT generates the END PDU on demand at state 5.	207
PC/STATE_5/VAL/	S5_V_P1		Verify that the IUT sends a BGAK and RS PDU on reception of retransmitted BGN PDU at state 5.	208
PC/STATE_5/VAL/	S5_V_P2		Verify that the IUT goes to state 3 on reception of BGN PDU at state 5	209
PC/STATE_5/VAL/	S5_V_P3		Verify that the IUT ignores a BGAK PDU and remains at state 5.	209
PC/STATE_5/VAL/	S5_V_P5		Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 5.	210
PC/STATE_5/VAL/	S5_V_P7		Verify that the IUT ignores a retransmitted RS PDU and remains at state 5.	210
PC/STATE_5/VAL/	S5_V_P8		Verify that the IUT sends a RSAK PDU on reception of RS PDU and goes to state 10.	211
PC/STATE_5/VAL/	S5_V_P9		Verify that the IUT goes to state 10 on reception of RSAK PDU at state 5.	212
PC/STATE_5/VAL/	S5_V_P10		Verify that the IUT ignores a ER PDU and remains at state 5.	213
PC/STATE_5/VAL/	S5_V_P11		Verify that the IUT ignores a ERAK PDU and remains at state 5.	214
PC/STATE_5/VAL/	S5_V_P12		Verify that the IUT ignores a SD PDU and remains at state 5.	214
PC/STATE_5/VAL/	S5_V_P13		Verify that the IUT ignores a POLL PDU and remains at state 5.	215

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PC/STATE_5/VAL/	S5_V_P15		Verify that the IUT ignores a USTAT PDU and remains at state 5.	217
PC/STATE_5/VAL/	S5_V_P16		Verify that the IUT accpets a UD PDU at state 5.	218
PC/STATE_5/VAL/	S5_V_P17		Verify that the IUT accpets a MD PDU at state 5.	218
PC/STATE_5/INV/	S5_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 5.	219
PC/STATE_5/INV/	S5_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 5.	220
PC/STATE_5/INV/	S5_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 5.	220
PC/STATE_5/INV/	S5_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 5.	221
PC/STATE_5/INV/	S5_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 5.	221
PC/STATE_5/INV/	S5_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 5.	222
PC/STATE_5/INV/	S5_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 5.	222
PC/STATE_5/INV/	S5_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 5.	223
PC/STATE_5/INV/	S5_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 5.	224
PC/STATE_5/INV/	S5_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 5.	225

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PC/STATE_5/INV/	S5_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 5.	227
PC/STATE_5/INV/	S5_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 5.	228
PC/STATE_5/INV/	S5_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 5.	229
PC/STATE_5/INV/	S5_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 5.	230
PC/STATE_5/INV/	S5_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 5.	231
PC/STATE_5/INV/	S5_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 5.	232
PC/STATE_5/INV/	S5_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 5.	233
PC/STATE_5/INV/	S5_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 5.	234

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PC/STATE_5/INV/	S5_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 5.	236
PC/STATE_5/INV/	S5_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 5.	237
PC/STATE_5/INV/	S5_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 5.	238
PC/STATE_5/INV/	S5_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 5.	239
PC/STATE_5/INV/	S5_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 5.	240
PC/STATE_5/INV/	S5_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 5.	241
PC/STATE_5/INV/	S5_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 5.	242
PC/STATE_5/INV/	S5_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 5.	243

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PC/STATE_5/INV/	S5_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 5.	245
PC/STATE_5/INV/	S5_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 5.	246
PC/STATE_5/INOP/	S5_IO_P4		Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 5.	246
PC/STATE_5/INOP/	S5_IO_P6		Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 5.	247
PC/STATE_7/VAL/	S7_V_P2		Verify that the IUT goes to state 3 on reception of BGN PDU at state 7.	248
PC/STATE_7/VAL/	S7_V_P5		Verify that the IUT sends a ENDAK PDU and goes to state 1 on reception of a END PDU at state 7.	249
PC/STATE_7/VAL/	S7_V_P8		Verify that the IUT goes to state 6 on reception of RS PDU at state 7.	250
PC/STATE_7/VAL/	S7_V_P11		Verify that the IUT sends a ERAK PDU and goes to state 8 on reception of a ER PDU at state 7.	251
PC/STATE_7/VAL/	S7_V_P12		Verify that the IUT goes to state 8 on reception of ERAK PDU at state 7.	252
PC/STATE_7/VAL/	S7_V_P19		Verify that the IUT ignores a SD PDU and remains at state 7.	252
PC/STATE_7/VAL/	S7_V_P21		Verify that the IUT ignores a POLL PDU and remains at state 7.	253
PC/STATE_7/VAL/	S7_V_P26		Verify that the IUT ignores a STAT PDU and remains at state 7.	254
PC/STATE_7/VAL/	S7_V_P36		Verify that the IUT ignores a USTAT PDU and remains at state 7.	255
PC/STATE_7/VAL/	S7_V_P40		Verify that the IUT accpets a UD PDU at state 7.	256

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PC/STATE_7/INV/	S7_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 7.	257
PC/STATE_7/INV/	S7_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 7.	258
PC/STATE_7/INV/	S7_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 7.	258
PC/STATE_7/INV/	S7_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 7.	259
PC/STATE_7/INV/	S7_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 7.	259
PC/STATE_7/INV/	S7_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 7.	260
PC/STATE_7/INV/	S7_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 7.	260
PC/STATE_7/INV/	S7_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 7.	261
PC/STATE_7/INV/	S7_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 7.	262
PC/STATE_7/INV/	S7_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 7.	263
PC/STATE_7/INV/	S7_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 7.	264

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PC/STATE_7/INV/	S7_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 7.	265
PC/STATE_7/INV/	S7_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 7.	266
PC/STATE_7/INV/	S7_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 7.	267
PC/STATE_7/INV/	S7_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 7.	268
PC/STATE_7/INV/	S7_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 7.	269
PC/STATE_7/INV/	S7_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 7.	270
PC/STATE_7/INV/	S7_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 7.	271
PC/STATE_7/INV/	S7_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 7.	272
PC/STATE_7/INV/	S7_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 7.	273

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PC/STATE_7/INV/	S7_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 7.	274
PC/STATE_7/INV/	S7_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 7.	275
PC/STATE_7/INV/	S7_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 7.	276
PC/STATE_7/INV/	S7_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 7.	277
PC/STATE_7/INV/	S7_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 7.	278
PC/STATE_7/INV/	S7_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 7.	279
PC/STATE_7/INV/	S7_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 7.	280
PC/STATE_7/INV/	S7_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 7.	281
PC/STATE_7/INV/	S7_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 7.	282

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PC/STATE_7/INV/	S7_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 7.	283
PC/STATE_7/INV/	S7_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 7.	284
PC/STATE_7/INOP/	S7_IO_P1		Verify that the IUT ignores a retransmitted BGN PDU and remains at state 7.	284
PC/STATE_7/INOP/	S7_IO_P3		Verify that the IUT ignores a BGAK PDU and remains at state 7.	285
PC/STATE_7/INOP/	S7_IO_P4		Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 7.	285
PC/STATE_7/INOP/	S7_IO_P6		Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 7.	286
PC/STATE_7/INOP/	S7_IO_P7		Verify that the IUT ignores a retransmitted RS PDU and remains at state 7.	286
PC/STATE_7/INOP/	S7_IO_P9		Verify that the IUT ignores a RSAK PDU and remains at state 7.	287
PC/STATE_7/INOP/	S7_IO_P10		Verify that the IUT ignores a retransmitted ER PDU and remains at state 7.	287
PC/STATE_10/VAL/	S10_V_A3		Verify that the IUT, at state 10, generates the END PDU on demand.	288
PC/STATE_10/VAL/	S10_V_A5		Verify that the IUT, at state 10, generates the RS PDU on demand.	289
PC/STATE_10/VAL/	S10_V_P1		Verify that the IUT, at state 10, sends a BGAK PDU on reception of a retransmitted BGN PDU.	290
PC/STATE_10/VAL/	S10_V_P2		Verify that the IUT, at state 10, goes to state 3 on reception of BGN PDU.	291
PC/STATE_10/VAL/	S10_V_P3		Verify that the IUT, at state 10, ignores a BGAK PDU and remains.	292
PC/STATE_10/VAL/	S10_V_P5		Verify that the IUT, at state 10, sends a ENDAK PDU and goes to state 1 on reception of a END PDU.	292

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PC/STATE_10/VAL/	S10_V_P7		Verify that the IUT, at state 10, sends a RSAK PDU on reception of a retransmitted RS PDU.	293
PC/STATE_10/VAL/	S10_V_P8		Verify that the IUT, at state 10, goes to state 6 on reception of RS PDU.	294
PC/STATE_10/VAL/	S10_V_P9		Verify that the IUT, at state 10, ignores a RSAK PDU and remains.	295
PC/STATE_10/VAL/	S10_V_P10		Verify that the IUT, at state 10, sends a ERAK PDU on reception of a retransmitted ER PDU.	296
PC/STATE_10/VAL/	S10_V_P11		Verify that the IUT, at state 10, goes to state 9 on reception of ER PDU.	297
PC/STATE_10/VAL/	S10_V_P12		Verify that the IUT, at state 10, ignores a ERAK PDU and remains.	298
PC/STATE_10/VAL/	S10_V_P13		Verify that the IUT, at state 10, sends a USTAT PDU on reception of SD PDU out of the window.	299
PC/STATE_10/VAL/	S10_V_P14		Verify that the IUT, at state 10, ignores a SD PDU that is out of the window when window is not available.	300
PC/STATE_10/VAL/	S10_V_P15		Verify that the IUT, at state 10, saves the next highest expected SD PDU.	301
PC/STATE_10/VAL/	S10_V_P17		Verify that the IUT, at state 10, saves a SD PDU that sequence number is between the sequence number of the next in sequence and the next highest expected SD PDU.	302
PC/STATE_10/VAL/	S10_V_P18		Verify that the IUT, at state 10, sends a ER PDU on reception of a SD PDU that sequence number is between the sequence number of the next in sequence and the next highest expected SD PDUs and is already in RX BUFFER.	303

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PC/STATE_10/VAL/	S10_V_P19		Verify that the IUT, at state 10, accepts the next in sequence SD PDU.	304
PC/STATE_10/VAL/	S10_V_P21		Verify that the IUT, at state 10, sends a ER PDU on reception of a POLL PDU that sequence number is less than that of the next highest expected SD PDU.	305
PC/STATE_10/VAL/	S10_V_P22		Verify that the IUT, at state 10, sends a STAT PDU on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.	306
PC/STATE_10/VAL/	S10_V_P23_1		Verify that the IUT, at state 10, sends a STAT PDU on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.	307
PC/STATE_10/VAL/	S10_V_P23_2		Verify that the IUT, at state 10, sends a STAT PDUs(with segmenting) on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.	308
PC/STATE_10/VAL/	S10_V_P24		Verify that the IUT, at state 10 and having no missing gap of received SD PDUs, sends a STAT PDU on reception of a POLL PDU that sequence number is less than or equal to that of the next highest expected SD PDU and is within the window.	310
PC/STATE_10/VAL/	S10_V_P25		Verify that the IUT, at state 10 and having a missing gap of received SD PDUs, sends a STAT PDU on reception of a POLL PDU that sequence number is less than or equal to that of the next highest expected SD PDU and is within the window.	311

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/VAL/	S10_V_P26		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number is incorrect.	312
PC/STATE_10/VAL/	S10_V_P27		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number is correct but SD PDU sequence number is incorrect.	313
PC/STATE_10/VAL/	S10_V_P32		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number and SD PDU sequence number are correct but its list element has incorrect sequence number.	314
PC/STATE_10/VAL/	S10_V_P33		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number and SD PDU sequence number are correct but its list elements are not increasing order.	315
PC/STATE_10/VAL/	S10_V_P38_1		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list element has incorrect sequence number.	317
PC/STATE_10/VAL/	S10_V_P38_2		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list elements are not increasing order.	319
PC/STATE_10/VAL/	S10_V_P39		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list elements are not increasing order.	321
PC/STATE_10/VAL/	S10_V_P40		Verify that the IUT accpets a UD PDU at state 10.	322

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/VAL/	S10_V_P41		Verify that the IUT accpets a MD PDU at state 10.	323
PC/STATE_10/INV/	S10_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 10.	324
PC/STATE_10/INV/	S10_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 10.	325
PC/STATE_10/INV/	S10_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 10.	325
PC/STATE_10/INV/	S10_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 10.	326
PC/STATE_10/INV/	S10_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 10.	326
PC/STATE_10/INV/	S10_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 10.	327
PC/STATE_10/INV/	S10_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 10.	327
PC/STATE_10/INV/	S10_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 10.	328
PC/STATE_10/INV/	S10_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 10.	329
PC/STATE_10/INV/	S10_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 10.	330
PC/STATE_10/INV/	S10_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 10.	331

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/INV/	S10_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 10.	332
PC/STATE_10/INV/	S10_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 10.	333
PC/STATE_10/INV/	S10_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 10.	334
PC/STATE_10/INV/	S10_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 10.	335
PC/STATE_10/INV/	S10_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 10.	336
PC/STATE_10/INV/	S10_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 10.	337
PC/STATE_10/INV/	S10_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 10.	338
PC/STATE_10/INV/	S10_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 10.	339
PC/STATE_10/INV/	S10_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 10.	340

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/INV/	S10_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 10.	341
PC/STATE_10/INV/	S10_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 10.	342
PC/STATE_10/INV/	S10_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 10.	343
PC/STATE_10/INV/	S10_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 10.	344
PC/STATE_10/INV/	S10_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 10.	345
PC/STATE_10/INV/	S10_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 10.	346
PC/STATE_10/INV/	S10_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 10.	347
PC/STATE_10/INV/	S10_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 10.	348
PC/STATE_10/INV/	S10_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 10.	349

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/INV/	S10_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 10.	350
PC/STATE_10/INV/	S10_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 10.	351
PC/STATE_10/INOP/	S10_IO_P4		Verify that the IUT, at state 10, goes to state 1 on reception of BGREJ PDU.	351
PC/STATE_10/INOP/	S10_IO_P6		Verify that the IUT, at state 10, goes to state 1 on reception of ENDAK PDU.	352
SP/TIMER/	S2_CC_T1		Verify that the IUT, at state 2, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.	353
SP/TIMER/	S4_CC_T1		Verify that the IUT, at state 4, goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.	354
SP/TIMER/	S5_CC_T1		Verify that the IUT, at state 5, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.	355
SP/TIMER/	S7_CC_T1		Verify that the IUT, at state 7, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.	356
SP/TIMER/	S10_POLL_T3		Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_POLL is expired.	357

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
SP/TIMER/	S10_KEEP_ALIVE_T4		Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_KEEP_ALIVE is expired.	358
SP/TIMER/	S10_IDLE_T5		Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_IDLE is expired.	359
SP/TIMER/	S10_NO_RESPONSE_T6		Verify that the IUT, at state 10, sends a END PDU when the Timer Timer_NO_RESPONSE is expired.	360
SP/PARAM/	SP3_MaxPD		Check the value of MaxPD system parameter(Maximum number of SD PDUs before transmission of a POLL PDU).	361

Detailed Comments :

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Detailed Comments :

II

Declarations Part

ASN.1 Type Definition
Type Name : LIST_ELEMENT_TYPE **Comments :** Used for STAT PDU Type definition
Type Definition

SEQUENCE {
PAD OCTET STRING(SIZE (1..1)),
LE BIT STRING(SIZE (24..24))
}

Detailed Comments :

ASN.1 Type Definition
Type Name : LIST_TYPE **Comments :** Used for STAT PDU Type definition
Type Definition
SEQUENCE OF LIST_ELEMENT_TYPE
Detailed Comments :

Test Suite Operation Definition	
Operation Name	: INC_MOD_8(parIN, amount:INTEGER)
Result Type	: INTEGER
Comments	:
Description	
INC_MOD_8(parIN, amount) is the modulo incremented value of "parIN" in the amount of "amount". The modulus equals 2E8(256). For example: INC_MOD_8(3,4)=7 INC_MOD_8(255,1)=0	
Detailed Comments	:

Test Suite Operation Definition	
Operation Name	: INC_MOD_24(parIN, amount:INTEGER)
Result Type	: INTEGER
Comments	:
Description	
INC_MOD_24(parIN, amount) is the modulo incremented value of "parIN" in the amount of "amount". The modulus equals 2E24(16777216). For example: INC_MOD_24(3,2)=5 INC_MOD_24(16777215,1)=0	
Detailed Comments	:

Test Suite Operation Definition	
Operation Name	: GET_VR_MR
Result Type	: INTEGER
Comments	:
Description	
This operation is used to set the Maximum acceptable Receive state value(VR(MR)). Updating VR(MR) is implementation dependent, but VR(MR) should not be set to a value < VR(H). An example of how VR)MR) may be determined is included in Appendix IV of Recommendation Q.2110.	
Detailed Comments	:

Test Suite Operation Definition

Operation Name : CHECK_N_PS(parPA,parN_PS,parPS:INTEGER)

Result Type : BOOLEAN

Comments :

Description

This operation is used to check if the value of parameter "N(PS)" in STAT PDU is valid or not.
This operation returns a BOOLEAN value "TRUE" when the value of "parN_PS" is between parPA and parPS (VT(PA)<=STAT.N(PS)<=VT(PS)).

Detailed Comments :

Test Suite Operation Definition

Operation Name : APPEND_LIST(parLIST:LIST_TYPE;parLE:INTEGER)

Result Type : LIST_TYPE

Comments :

Description

This operation is used to append new element of value "parLE" to existing list "parLIST".
The procedures of this operation is as follows:

1. Make a instance of LIST_ELEMENT_TYPE
   which has "00"O as PAD field and bitstring of encoded value of "parLE" as LE field.
2. Append the instance of above to existing list of "parLIST".
3. Return the new list.

Detailed Comments :

Test Suite Operation Definition

Operation Name : GEN_OCTET(parLEN:INTEGER)

Result Type : OCTETSTRING

Comments :

Description

This operation is used to generate a OCTETSTRING of length "parLEN" .
For example: GEN_OCTET(3):='000000'O
GEN_OCTET(10):='00000000000000000000'O

Detailed Comments :

Test Suite Parameter Declarations			
Parameter Name	**Type**	**PICS/PIXIT Ref**	**Comments**
Max_CC	INTEGER	PICS SP1	Maximum Number of transmissions of a BGN, END, ER, or RS PDU(MaxCC)
Max_PD	INTEGER	PICS SP2	Maximum Number of SD PDUs before transmission of a POLL PDU(MaxPD)
Max_STAT	INTEGER	PICS SP3	Maximum Number of list elements placed in a STAT PDU
Info_Max_Len	INTEGER	PICS SP4	The maximum length of information field in SD, UD, MD PDUs. This value may be derived from the maximum langth PDU size. (Info_Max_Len = PICS SP4 − 4)
TimerPOLLtime	INTEGER	PICS SP5	The time between transmission of POLL PDU at active phase
TimerKEEP_ALIVEtime	INTEGER	PICS SP6	The time between transmission of POLL PDU at transient phase
TimerNO_RESPONSEtime	INTEGER	PICS SP7	The maximum time interval during which at least one STAT PDU needs to be received.
TimerIDLEtime	INTEGER	PICS SP8	may be considerably greater than Timer_KEEP_ALIVE
TimerCCtime	INTEGER	PICS SP9	The time between transmission of BGN, END, ER, or RS PDU
UU_Max_Len	INTEGER	PICS SP10	Maximum length of variable length SSCOP−UU field
WAITtime	INTEGER	PIXIT 1	Used to limit the test time waiting for "no response" from the IUT
TESTtime	INTEGER	PIXIT 2	The value for the timer that is long enough to allow test operator intervention
Detailed Comments :			

Test Suite Variable Declarations			
Variable Name	**Type**	**Value**	**Comments**
VT_SQ	INTEGER	0	Transmitter Connection Sequence state variable
VR_SQ	INTEGER	0	Receiver Connection Sequence state variable
Detailed Comments :			

Test Case Variable Declarations			
Variable Name	**Type**	**Value**	**Comments**
VT_MS	INTEGER		Maximum Send state variable
VR_MR	INTEGER		Maximum Receive state variable
VT_S	INTEGER	0	Send state variable
VT_PS	INTEGER	0	Poll Send state variable
VT_A	INTEGER	0	Acknowledge state variable
VT_PA	INTEGER	0	Poll Acknowledge state variable
VT_PD	INTEGER	0	Poll Data state variable
VR_R	INTEGER	0	Receive state variable
VR_H	INTEGER	0	Highest expected state variable
count	INTEGER		general purpose counter
TCV_OCT	OCTETSTRING		general purpose
TCV_N_SQ	INTEGER		to handle N(SQ)
TCV_N_MR	INTEGER		to handle N(MR)
TCV_N_PS	INTEGER		to handle N(PS)
TCV_LIST	LIST_TYPE		to handle LIST field of STAT PDU
TCV_LIST1	LIST_TYPE		to handle LIST field of STAT PDU
Detailed Comments :			

PCO Declarations			
PCO Name	**PCO Type**	**Role**	**Comments**
LT_PCO	L_SSCOP	LT	Lower boundary of SSCOP
Detailed Comments :			

Timer Declarations			
Timer Name	**Duration**	**Unit**	**Comments**
T_Opr	TESTtime	s	This timer is used to allow test operator intervention
Timer_CC	TimerCCtime	s	The time between transmission of BGN, END, ER, or RS PDU
Timer_POLL	TimerPOLLtime	s	The time between transmission of POLL PDU at active phase
Timer_KEEP_ALIVE	TimerKEEP_ALIVEtime	s	The time between transmission of POLL PDU at transient phase
Timer_IDLE	TimerIDLEtime	s	may be considerably greater than Timer_KEEP_ALIVE
Timer_NO_RESPONSE	TimerNO_RESPONSEtime	s	The maximum time interval during which at least one STAT PDU needs to be received.
T_Wait	WAITtime	s	This timer is used when no response is expected from IUT
Detailed Comments :			

TTCN PDU Type Definition

PDU Name : SD
PCO Type : L_SSCOP
Comments :

Field Name	Field Type	Comments
Information	OCTETSTRING[0..Info_Max_Len]	
PAD	OCTETSTRING[0..3]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
N_S	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : POLL
PCO Type : L_SSCOP
Comments :

Field Name	Field Type	Comments
RESERVED1	OCTETSTRING[1]	
N_PS	BITSTRING[24]	
RESERVED2	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_S	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : STAT
PCO Type : L_SSCOP
Comments :

Field Name	Field Type	Comments
LIST	LIST_TYPE	
RSVD1	OCTETSTRING[1]	
N_PS	BITSTRING[24]	
RSVD2	OCTETSTRING[1]	
N_MR	BITSTRING[24]	
RESERVED	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_R	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : USTAT
PCO Type : L_SSCOP
Comments :

Field Name	Field Type	Comments
PAD1	OCTETSTRING[1]	
LE1	BITSTRING[24]	
PAD2	OCTETSTRING[1]	
LE2	BITSTRING[24]	
RESERVED1	OCTETSTRING[1]	
N_MR	BITSTRING[24]	
RESERVED2	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_R	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : UD
PCO Type : L_SSCOP
Comments :

Field Name	Field Type	Comments
Information	OCTETSTRING[0..Info_Max_Len]	
PAD	OCTETSTRING[0..3]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
RESERVED	OCTETSTRING[3]	

Detailed Comments :

TTCN PDU Type Definition		
PDU Name : MD **PCO Type :** L_SSCOP **Comments :**		
Field Name	**Field Type**	**Comments**
Information	OCTETSTRING[0..Info_Max_Len]	
PAD	OCTETSTRING[0..3]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
RESERVED	OCTETSTRING[3]	
Detailed Comments :		

TTCN PDU Type Definition		
PDU Name : BGN **PCO Type :** L_SSCOP **Comments :**		
Field Name	**Field Type**	**Comments**
UU	OCTETSTRING[0..UU_Max_Len]	
PAD	OCTETSTRING[0..3]	
RESERVED	OCTETSTRING[3]	
N_SQ	BITSTRING[8]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	
Detailed Comments :		

TTCN PDU Type Definition

PDU Name : BGAK
PCO Type : L_SSCOP
Comments :

Field Name	Field Type	Comments
UU	OCTETSTRING[0..UU_Max_Len]	
PAD	OCTETSTRING[0..3]	
RESERVED	OCTETSTRING[4]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : BGREJ
PCO Type : L_SSCOP
Comments :

Field Name	Field Type	Comments
UU	OCTETSTRING[0..UU_Max_Len]	
PAD	OCTETSTRING[0..3]	
RESERVED1	OCTETSTRING[4]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
RESERVED2	OCTETSTRING[3]	

Detailed Comments :

TTCN PDU Type Definition		
PDU Name : END **PCO Type :** L_SSCOP **Comments :**		
Field Name	**Field Type**	**Comments**
UU	OCTETSTRING[0..UU_Max_Len]	
PAD	OCTETSTRING[0..3]	
RESERVED1	OCTETSTRING[4]	
PL	BITSTRING[2]	
RR	BITSTRING[1]	"R" is a reserved word in TTCN.
S	BITSTRING[1]	
PDU_Type	BITSTRING[4]	
RESERVED2	OCTETSTRING[3]	
Detailed Comments :		

TTCN PDU Type Definition		
PDU Name : ENDAK **PCO Type :** L_SSCOP **Comments :**		
Field Name	**Field Type**	**Comments**
RESERVED1	OCTETSTRING[4]	
RESERVED2	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
RESERVED3	OCTETSTRING[3]	
Detailed Comments :		

TTCN PDU Type Definition		
PDU Name : RS **PCO Type :** L_SSCOP **Comments :**		
Field Name	**Field Type**	**Comments**
UU	OCTETSTRING[0..UU_Max_Len]	
PAD	OCTETSTRING[0..3]	
RESERVED	OCTETSTRING[3]	
N_SQ	BITSTRING[8]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	
Detailed Comments :		

TTCN PDU Type Definition		
PDU Name : RSAK **PCO Type :** L_SSCOP **Comments :**		
Field Name	**Field Type**	**Comments**
RESERVED1	OCTETSTRING[4]	
RESERVED2	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	
Detailed Comments :		

TTCN PDU Type Definition		
PDU Name : ER **PCO Type :** L_SSCOP **Comments :**		
Field Name	**Field Type**	**Comments**
RESERVED	OCTETSTRING[3]	
N_SQ	BITSTRING[8]	
RSVD	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	
Detailed Comments :		

TTCN PDU Type Definition		
PDU Name : ERAK **PCO Type :** L_SSCOP **Comments :**		
Field Name	**Field Type**	**Comments**
RESERVED	OCTETSTRING[4]	
RSVD	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	
Detailed Comments :		

TTCN PDU Type Definition

PDU Name : IVSD
PCO Type : L_SSCOP
Comments : Used to generate a SD PDU of incorrect length

Field Name	Field Type	Comments
InformationandPAD	OCTETSTRING[0..INFINITY]	to generate a PDU of incorrect length
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
N_S	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVPOLL
PCO Type : L_SSCOP
Comments : Used to generate a POLL PDU of incorrect length

Field Name	Field Type	Comments
INVALID	OCTETSTRING[0..4]	
RESERVED1	OCTETSTRING[1]	
N_PS	BITSTRING[24]	
RESERVED2	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_S	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVSTAT
PCO Type : L_SSCOP
Comments : Used to generate a STAT PDU whcih is not 32−bit aligned

Field Name	Field Type	Comments
INVALID	OCTETSTRING[0..4]	
LIST	LIST_TYPE	
RSVD1	OCTETSTRING[1]	
N_PS	BITSTRING[24]	
RSVD2	OCTETSTRING[1]	
N_MR	BITSTRING[24]	
RESERVED	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_R	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVUSTAT
PCO Type : L_SSCOP
Comments : Used to generate a USTAT PDU of incorrect length

Field Name	Field Type	Comments
INVALID	OCTETSTRING[0..4]	
PAD1	OCTETSTRING[1]	
LE1	BITSTRING[24]	
PAD2	OCTETSTRING[1]	
LE2	BITSTRING[24]	
RESERVED1	OCTETSTRING[1]	
N_MR	BITSTRING[24]	
RESERVED2	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_R	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVUD
PCO Type : L_SSCOP
Comments : Used to generate a UD PDU of incorrect langth

Field Name	Field Type	Comments
InformationandPAD	OCTETSTRING[0..INFINITY]	to generate a PDU of incorrect length
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
RESERVED	OCTETSTRING[3]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVMD
PCO Type : L_SSCOP
Comments : Used to generate a MD PDU of incorrect langth

Field Name	Field Type	Comments
InformationandPAD	OCTETSTRING[0..INFINITY]	to generate a PDU of incorrect length
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
RESERVED	OCTETSTRING[3]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVBGN
PCO Type : L_SSCOP
Comments : Used to generate a BGN PDU of incorrect length

Field Name	Field Type	Comments
UUandPAD	OCTETSTRING[0..INFINITY]	to generate a PDU of incorrect length
RESERVED	OCTETSTRING[3]	
N_SQ	BITSTRING[8]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	

Detailed Comments : PAD field can be 6 octets(normally 3 octets).

TTCN PDU Type Definition

PDU Name : IVBGAK
PCO Type : L_SSCOP
Comments : Used to generate a BGAK PDU of incorrect length

Field Name	Field Type	Comments
UUandPAD	OCTETSTRING[0..INFINITY]	to generate a PDU of incorrect length
RESERVED	OCTETSTRING[4]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVBGREJ
PCO Type : L_SSCOP
Comments : Used to generate a BGREJ PDU of incorrect length

Field Name	Field Type	Comments
UUandPAD	OCTETSTRING[0..INFINITY]	to generate a PDU of incorrect length
RESERVED1	OCTETSTRING[4]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
RESERVED2	OCTETSTRING[3]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVEND
PCO Type : L_SSCOP
Comments : Used to generate a END PDU of incorrec length

Field Name	Field Type	Comments
UUandPAD	OCTETSTRING[0..INFINITY]	to generate a PDU of incorrect length
RESERVED1	OCTETSTRING[4]	
PL	BITSTRING[2]	
RR	BITSTRING[1]	"R" is a reserved word in TTCN.
S	BITSTRING[1]	
PDU_Type	BITSTRING[4]	
RESERVED2	OCTETSTRING[3]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVENDAK
PCO Type : L_SSCOP
Comments : Used to generate a ENDAK PDU of incorrect length

Field Name	Field Type	Comments
INVALID	OCTETSTRING[0..4]	
RESERVED1	OCTETSTRING[4]	
RESERVED2	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
RESERVED3	OCTETSTRING[3]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVRS
PCO Type : L_SSCOP
Comments : Used to generate a RS PDU of incorrect length

Field Name	Field Type	Comments
UUandPAD	OCTETSTRING[0..INFINITY]	to generate a PDU of incorrect length
RESERVED	OCTETSTRING[3]	
N_SQ	BITSTRING[8]	
PL	BITSTRING[2]	
RSVD	BITSTRING[2]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVRSAK
PCO Type : L_SSCOP
Comments : Used to generate a RSAK PDU of incorrect length

Field Name	Field Type	Comments
INVALID	OCTETSTRING[0..4]	
RESERVED1	OCTETSTRING[4]	
RESERVED2	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVER
PCO Type : L_SSCOP
Comments : Used to generate a ER PDU of incorrect length

Field Name	Field Type	Comments
INVALID	OCTETSTRING[0..4]	
RESERVED	OCTETSTRING[3]	
N_SQ	BITSTRING[8]	
RSVD	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	

Detailed Comments :

TTCN PDU Type Definition

PDU Name : IVERAK
PCO Type : L_SSCOP
Comments : Used to generate a ERAK PDU of incorrect length

Field Name	Field Type	Comments
INVALID	OCTETSTRING[0..4]	
RESERVED	OCTETSTRING[4]	
RSVD	BITSTRING[4]	
PDU_Type	BITSTRING[4]	
N_MR	BITSTRING[24]	

Detailed Comments :

III

Constraints Part

TTCN PDU Constraint Declaration		
Constraint Name : SD_R_GEN		
PDU Type : SD		
Derivation Path :		
Comments : General RECEIVE constraint		
Field Name	**Field Value**	**Comments**
Information	*	
PAD	*	
PL	?	
RSVD	’00’B	
PDU_Type	’1000’B	
N_S	INT_TO_BIT(VR_R, 24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : SD_S_GEN		
PDU Type : SD		
Derivation Path :		
Comments : Constraint for normal SEND		
Field Name	**Field Value**	**Comments**
Information	’0000000000’O	Must be acceptable by IUT’s upper layers
PAD	’000000’O	
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1000’B	
N_S	INT_TO_BIT(VT_S,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : SD_S_N_S(parN_S:INTEGER)		
PDU Type : SD		
Derivation Path :		
Comments : Constraint for SEND with N_S variation		
Field Name	**Field Value**	**Comments**
Information	’0000000000’O	
PAD	’000000’O	
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1000’B	
N_S	INT_TO_BIT(parN_S,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : SD_S_INV		
PDU Type : SD		
Derivation Path :		
Comments : an invalid SD PDU which is not 32−bit aligned		
Field Name	**Field Value**	**Comments**
Information	’00000000000000000000’O	10 octets, PAD must be 2 octets
PAD	’000000’O	3 octets
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1000’B	
N_S	INT_TO_BIT(VT_S,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : POLL_R_GEN		
PDU Type : POLL		
Derivation Path :		
Comments : General RECEIVE constraint		
Field Name	**Field Value**	**Comments**
RESERVED1	’00’O	
N_PS	?	
RESERVED2	’0000’B	
PDU_Type	’1010’B	
N_S	?	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : POLL_S_GEN		
PDU Type : POLL		
Derivation Path :		
Comments : Constraint for SEND		
Field Name	**Field Value**	**Comments**
RESERVED1	’00’O	
N_PS	INT_TO_BIT(VT_PS,24)	
RESERVED2	’0000’B	
PDU_Type	’1010’B	
N_S	INT_TO_BIT(VT_S,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : POLL_S_N_S(parN_S:INTEGER)		
PDU Type : POLL		
Derivation Path :		
Comments : Constraint for SEND with N_S variation		
Field Name	**Field Value**	**Comments**
RESERVED1	’00’O	
N_PS	INT_TO_BIT(VT_PS,24)	
RESERVED2	’0000’B	
PDU_Type	’1010’B	
N_S	INT_TO_BIT(parN_S,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : STAT_R_N_R(parN_R:INTEGER)		
PDU Type : STAT		
Derivation Path :		
Comments : Constraint for RECEIVE without element		
Field Name	**Field Value**	**Comments**
LIST	−	
RSVD1	’00’O	
N_PS	?	
RSVD2	’00’O	
N_MR	?	
RESERVED	’0000’B	
PDU_Type	’1011’B	
N_R	INT_TO_BIT(parN_R, 24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : STAT_R_LIST(parLIST:LIST_TYPE; parN_R:INTEGER)		
PDU Type : STAT		
Derivation Path :		
Comments : Constraint for RECEIVE with elements		
Field Name	**Field Value**	**Comments**
LIST	parLIST	
RSVD1	’00’O	
N_PS	?	
RSVD2	’00’O	
N_MR	?	
RESERVED	’0000’B	
PDU_Type	’1011’B	
N_R	INT_TO_BIT(parN_R, 24)	
Detailed Comments :		

TTCN PDU Constraint Declaration

Constraint Name : STAT_S_N_PS_N_R(parLIST:LIST_TYPE; parN_PS,parN_R:INTEGER)
PDU Type : STAT
Derivation Path :
Comments : Constraint for SEND with N_PS and N_R variations.

Field Name	Field Value	Comments
LIST	parLIST	
RSVD1	'00'O	
N_PS	INT_TO_BIT(parN_PS,24)	
RSVD2	'00'O	
N_MR	INT_TO_BIT(VR_MR, 24)	
RESERVED	'0000'B	
PDU_Type	'1011'B	
N_R	INT_TO_BIT(parN_R, 24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : USTAT_R_LIST(parLE1,parLE2:INTEGER; parN_R:INTEGER)
PDU Type : USTAT
Derivation Path :
Comments : Constraint for RECEIVE with LE variation

Field Name	Field Value	Comments
PAD1	?	
LE1	INT_TO_BIT(parLE1, 24)	
PAD2	?	
LE2	INT_TO_BIT(parLE2, 24)	
RESERVED1	'00'O	
N_MR	?	
RESERVED2	'0000'B	
PDU_Type	'1100'B	
N_R	INT_TO_BIT(parN_R, 24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : USTAT_S_LIST(parLE1,parLE2:INTEGER; parN_R:INTEGER)
PDU Type : USTAT
Derivation Path :
Comments : Constraint for SEND with elements variation.

Field Name	Field Value	Comments
PAD1	’00’O	
LE1	INT_TO_BIT(parLE1,24)	
PAD2	’00’O	
LE2	INT_TO_BIT(parLE2,24)	
RESERVED1	’00’O	
N_MR	INT_TO_BIT(VR_MR,24)	
RESERVED2	’0000’B	
PDU_Type	’1100’B	
N_R	INT_TO_BIT(parN_R, 24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : UD_R_GEN
PDU Type : UD
Derivation Path :
Comments : General RECEIVE constraint

Field Name	Field Value	Comments
Information	*	
PAD	*	
PL	?	
RSVD	’00’B	
PDU_Type	’1101’B	
RESERVED	’000000’O	

Detailed Comments :

TTCN PDU Constraint Declaration		
Constraint Name : UD_S_GEN		
PDU Type : UD		
Derivation Path :		
Comments : Constraint for normal SEND		
Field Name	**Field Value**	**Comments**
Information	’0000000000’O	
PAD	’000000’O	
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1101’B	
RESERVED	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : UD_S_INV		
PDU Type : UD		
Derivation Path :		
Comments : an invalid UD PDU which is not 32−bit aligned		
Field Name	**Field Value**	**Comments**
Information	’00000000000000000000’O	10 octets, PAD must be 2 octets
PAD	’000000’O	3 octets
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1101’B	
RESERVED	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : MD_R_GEN		
PDU Type : MD		
Derivation Path :		
Comments : General RECEIVE constraint		
Field Name	**Field Value**	**Comments**
Information	*	
PAD	*	
PL	?	
RSVD	’00’B	
PDU_Type	’1110’B	
RESERVED	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : MD_S_GEN		
PDU Type : MD		
Derivation Path :		
Comments : Constraint for normal SEND		
Field Name	**Field Value**	**Comments**
Information	’0000000000’O	
PAD	’000000’O	
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1110’B	
RESERVED	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration

Constraint Name : MD_S_INV
PDU Type : MD
Derivation Path :
Comments : an invalid MD PDU which is not 32−bit aligned

Field Name	Field Value	Comments
Information	’00000000000000000000’O	10 octets, PAD must be 2 octets
PAD	’000000’O	3 octets
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1110’B	
RESERVED	’000000’O	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : BGN_R_GEN
PDU Type : BGN
Derivation Path :
Comments : General RECEIVE constraint

Field Name	Field Value	Comments
UU	*	
PAD	*	
RESERVED	’000000’O	
N_SQ	COMPLEMENT(INT_TO_BIT(VR_SQ,8))	retransmitted BGN PDU check
PL	?	
RSVD	’00’B	
PDU_Type	’0001’B	
N_MR	?	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : BGN_R_RET(parN_SQ,parN_MR:INTEGER)
PDU Type : BGN
Derivation Path :
Comments : constraint for retransmitted BGN PDU

Field Name	Field Value	Comments
UU	*	
PAD	*	
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(parN_SQ,8)	
PL	?	
RSVD	’00’B	
PDU_Type	’0001’B	
N_MR	INT_TO_BIT(parN_MR,24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : BGN_S_GEN
PDU Type : BGN
Derivation Path :
Comments :

Field Name	Field Value	Comments
UU	−	
PAD	−	
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0001’B	
N_MR	INT_TO_BIT(VR_MR,24)	

Detailed Comments :

TTCN PDU Constraint Declaration		
Constraint Name : BGN_S_INV		
PDU Type : BGN		
Derivation Path :		
Comments : an invalid BGN PDU which is not 32−bit aligned		
Field Name	**Field Value**	**Comments**
UU	’00000000000000000000’O	10 octets, PAD must be 2 octets
PAD	’000000’O	3 octets
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0001’B	
N_MR	INT_TO_BIT(VR_MR,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : BGN_S_CODE		
PDU Type : BGN		
Derivation Path :		
Comments : an invalid PDU which has an unknown PDU type code		
Field Name	**Field Value**	**Comments**
UU	−	
PAD	−	
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0000’B	
N_MR	INT_TO_BIT(VR_MR,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : BGAK_R_GEN		
PDU Type : BGAK		
Derivation Path :		
Comments : General RECEIVE constraint		
Field Name	**Field Value**	**Comments**
UU	*	
PAD	*	
RESERVED	’00000000’O	
PL	?	
RSVD	’00’B	
PDU_Type	’0010’B	
N_MR	?	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : BGAK_S_GEN		
PDU Type : BGAK		
Derivation Path :		
Comments :		
Field Name	**Field Value**	**Comments**
UU	−	
PAD	−	
RESERVED	’00000000’O	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0010’B	
N_MR	INT_TO_BIT(VR_MR,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : BGAK_S_INV		
PDU Type : BGAK		
Derivation Path :		
Comments : an invalid BGAK PDU which is not 32−bit aligned		
Field Name	**Field Value**	**Comments**
UU	’00000000000000000000’O	10 octets, PAD must be 2 octets
PAD	’000000’O	3 octets
RESERVED	’00000000’O	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0010’B	
N_MR	INT_TO_BIT(VR_MR,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : BGREJ_R_GEN		
PDU Type : BGREJ		
Derivation Path :		
Comments : General RECEIVE constraint		
Field Name	**Field Value**	**Comments**
UU	*	
PAD	*	
RESERVED1	’00000000’O	
PL	?	
RSVD	’00’B	
PDU_Type	’0111’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : BGREJ_S_GEN		
PDU Type : BGREJ		
Derivation Path :		
Comments :		
Field Name	**Field Value**	**Comments**
UU	−	
PAD	−	
RESERVED1	’00000000’O	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0111’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : BGREJ_S_INV		
PDU Type : BGREJ		
Derivation Path :		
Comments : an invali BGREJ PDU which is not 32−bit aligned		
Field Name	**Field Value**	**Comments**
UU	’00000000000000000000’O	10 octets, PAD must be 2 octets
PAD	’000000’O	3 octets
RESERVED1	’00000000’O	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0111’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : END_R_GEN		
PDU Type : END		
Derivation Path :		
Comments : general RECEIVE constraint		
Field Name	**Field Value**	**Comments**
UU	*	
PAD	*	
RESERVED1	’00000000’O	
PL	?	
RR	’0’B	
S	?	IUT resend the last END PDU sent
PDU_Type	’0011’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : END_R_USER		
PDU Type : END		
Derivation Path :		
Comments : RECEIVE constraint for USER initiated release		
Field Name	**Field Value**	**Comments**
UU	*	
PAD	*	
RESERVED1	’00000000’O	
PL	?	
RR	’0’B	
S	’0’B	user initiated release
PDU_Type	’0011’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : END_R_SSCOP		
PDU Type : END		
Derivation Path :		
Comments : RECEIVE constraint for SSCOP initiated release		
Field Name	**Field Value**	**Comments**
UU	–	
PAD	–	
RESERVED1	’00000000’O	
PL	’00’B	
RR	’0’B	
S	’1’B	SSCOP initiated release
PDU_Type	’0011’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : END_S_USER		
PDU Type : END		
Derivation Path :		
Comments : SEND constraint for USER initiated release		
Field Name	**Field Value**	**Comments**
UU	–	
PAD	–	
RESERVED1	’00000000’O	
PL	’00’B	
RR	’0’B	
S	’0’B	
PDU_Type	’0011’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : END_S_SSCOP		
PDU Type : END		
Derivation Path :		
Comments : SEND constraint for SSCOP initiated release		
Field Name	**Field Value**	**Comments**
UU	−	
PAD	−	
RESERVED1	’00000000’O	
PL	’00’B	
RR	’0’B	
S	’1’B	
PDU_Type	’0011’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : END_S_INV		
PDU Type : END		
Derivation Path :		
Comments : an invalid END PDU which is not 32−bit aligned		
Field Name	**Field Value**	**Comments**
UU	’00000000000000000000’O	10 octets, PAD must be 2 octets
PAD	’000000’O	3 octets
RESERVED1	’00000000’O	
PL	’00’B	
RR	’0’B	
S	’0’B	
PDU_Type	’0011’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration

Constraint Name : ENDAK_R_GEN
PDU Type : ENDAK
Derivation Path :
Comments : General RECEIVE constraint

Field Name	Field Value	Comments
RESERVED1	'00000000'O	
RESERVED2	'0000'B	
PDU_Type	'0100'B	
RESERVED3	'000000'O	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : ENDAK_S_GEN
PDU Type : ENDAK
Derivation Path :
Comments : Constraint for normal SEND

Field Name	Field Value	Comments
RESERVED1	'00000000'O	
RESERVED2	'0000'B	
PDU_Type	'0100'B	
RESERVED3	'000000'O	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : RS_R_GEN
PDU Type : RS
Derivation Path :
Comments : General RECEIVE constraint

Field Name	Field Value	Comments
UU	*	
PAD	*	
RESERVED	'000000'O	
N_SQ	COMPLEMENT(INT_TO_BIT(VR_SQ,8))	retransmitted RS PDU check
PL	?	
RSVD	'00'B	
PDU_Type	'0101'B	
N_MR	?	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : RS_R_RET(parN_SQ,parN_MR:INTEGER)
PDU Type : RS
Derivation Path :
Comments : constraint for retransmitted RS PDU

Field Name	Field Value	Comments
UU	*	
PAD	*	
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(parN_SQ,8)	
PL	?	
RSVD	’00’B	
PDU_Type	’0101’B	
N_MR	INT_TO_BIT(parN_MR,24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : RS_S_GEN
PDU Type : RS
Derivation Path :
Comments :

Field Name	Field Value	Comments
UU	−	
PAD	−	
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0101’B	
N_MR	INT_TO_BIT(VR_MR,24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : RS_S_INV
PDU Type : RS
Derivation Path :
Comments : an invalid RS PDU which is not 32−bit aligned

Field Name	Field Value	Comments
UU	’00000000000000000000’O	10 octets, PAD must be 2 octets
PAD	’000000’O	3 octets
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0101’B	
N_MR	INT_TO_BIT(VR_MR,24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : RSAK_R_GEN
PDU Type : RSAK
Derivation Path :
Comments : General RECEIVE constraint

Field Name	Field Value	Comments
RESERVED1	’00000000’O	
RESERVED2	’0000’B	
PDU_Type	’0110’B	
N_MR	?	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : RSAK_S_GEN
PDU Type : RSAK
Derivation Path :
Comments : Constraint for normal SEND

Field Name	Field Value	Comments
RESERVED1	’00000000’O	
RESERVED2	’0000’B	
PDU_Type	’0110’B	
N_MR	INT_TO_BIT(VR_MR, 24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : ER_R_GEN
PDU Type : ER
Derivation Path :
Comments : General RECEIVE constraint

Field Name	Field Value	Comments
RESERVED	'000000'O	
N_SQ	COMPLEMENT(INT_TO_BIT(VR_SQ,8))	retransmitted ER PDU check
RSVD	'0000'B	
PDU_Type	'1001'B	
N_MR	?	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : ER_R_RET(parN_SQ,parN_MR:INTEGER)
PDU Type : ER
Derivation Path :
Comments : constraint for retransmitted RS PDU

Field Name	Field Value	Comments
RESERVED	'000000'O	
N_SQ	INT_TO_BIT(parN_SQ,8)	
RSVD	'0000'B	
PDU_Type	'1001'B	
N_MR	INT_TO_BIT(parN_MR,24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : ER_S_GEN
PDU Type : ER
Derivation Path :
Comments : Constraint fro normal SEND

Field Name	Field Value	Comments
RESERVED	'000000'O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
RSVD	'0000'B	
PDU_Type	'1001'B	
N_MR	INT_TO_BIT(VR_MR,24)	

Detailed Comments :

TTCN PDU Constraint Declaration		
Constraint Name : ERAK_R_GEN		
PDU Type : ERAK		
Derivation Path :		
Comments : General RECEIVE constraint		
Field Name	**Field Value**	**Comments**
RESERVED	’00000000’O	
RSVD	’0000’B	
PDU_Type	’1111’B	
N_MR	?	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : ERAK_S_GEN		
PDU Type : ERAK		
Derivation Path :		
Comments : Constraint for normal SEND		
Field Name	**Field Value**	**Comments**
RESERVED	’00000000’O	
RSVD	’0000’B	
PDU_Type	’1111’B	
N_MR	INT_TO_BIT(VR_MR, 24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : IVSD_S_INV(parInformationandPAD:OCTETSTRING)		
PDU Type : IVSD		
Derivation Path :		
Comments : Used to generate a SD PDU of incorrect length		
Field Name	**Field Value**	**Comments**
InformationandPAD	parInformationandPAD	to generate a PDU of incorrect length
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1000’B	
N_S	INT_TO_BIT(VT_S,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration

Constraint Name : IVPOLL_S_INV(parINVALID:OCTETSTRING)
PDU Type : IVPOLL
Derivation Path :
Comments : Constraint for SEND

Field Name	Field Value	Comments
INVALID	parINVALID	
RESERVED1	’00’O	
N_PS	INT_TO_BIT(VT_PS,24)	
RESERVED2	’0000’B	
PDU_Type	’1010’B	
N_S	INT_TO_BIT(VT_S,24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : IVSTAT_S_INV(parLIST:LIST_TYPE;parINVALID:OCTETSTRING)
PDU Type : IVSTAT
Derivation Path :
Comments : an STAT PDU which is not 32−bit aligned

Field Name	Field Value	Comments
INVALID	parINVALID	
LIST	parLIST	
RSVD1	’00’O	
N_PS	INT_TO_BIT(VT_PS,24)	
RSVD2	’00’O	
N_MR	INT_TO_BIT(VR_MR, 24)	
RESERVED	’0000’B	
PDU_Type	’1011’B	
N_R	INT_TO_BIT(VR_R, 24)	

Detailed Comments :

TTCN PDU Constraint Declaration		
Constraint Name : IVUSTAT_S_INV(parLE1,parLE2:INTEGER; parINVALID:OCTETSTRING)		
PDU Type : IVUSTAT		
Derivation Path :		
Comments : Constraint for SEND with elements variation.		
Field Name	**Field Value**	**Comments**
INVALID	parINVALID	
PAD1	'00'O	
LE1	INT_TO_BIT(parLE1,24)	
PAD2	'00'O	
LE2	INT_TO_BIT(parLE2,24)	
RESERVED1	'00'O	
N_MR	INT_TO_BIT(VR_MR,24)	
RESERVED2	'0000'B	
PDU_Type	'1100'B	
N_R	INT_TO_BIT(VR_R, 24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : IVUD_S_INV(parInformationandPAD:OCTETSTRING)		
PDU Type : IVUD		
Derivation Path :		
Comments : Used to generate a UD PDU of incorrect length		
Field Name	**Field Value**	**Comments**
InformationandPAD	parInformationandPAD	to generate a PDU of incorrect length
PL	'11'B	
RSVD	'00'B	
PDU_Type	'1101'B	
RESERVED	'000000'O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : IVMD_S_INV(parInformationandPAD:OCTETSTRING)		
PDU Type : IVMD		
Derivation Path :		
Comments : Used to generate a MD PDU of incorrect length		
Field Name	**Field Value**	**Comments**
InformationandPAD	parInformationandPAD	to generate a PDU of incorrect length
PL	’11’B	
RSVD	’00’B	
PDU_Type	’1110’B	
RESERVED	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : IVBGN_S_INV(parUUandPAD:OCTETSTRING)		
PDU Type : IVBGN		
Derivation Path :		
Comments : Used to generate a BGN PDU of incorrect length		
Field Name	**Field Value**	**Comments**
UUandPAD	parUUandPAD	to generate a PDU of incorrect length
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0001’B	
N_MR	INT_TO_BIT(VR_MR,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : IVBGAK_S_INV(parUUandPAD:OCTETSTRING)		
PDU Type : IVBGAK		
Derivation Path :		
Comments : Used to generate a BGN PDU of incorrect length		
Field Name	**Field Value**	**Comments**
UUandPAD	parUUandPAD	to generate a PDU of incorrect length
RESERVED	’00000000’O	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0010’B	
N_MR	INT_TO_BIT(VR_MR,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : IVBGREJ_S_INV(parUUandPAD:OCTETSTRING)		
PDU Type : IVBGREJ		
Derivation Path :		
Comments : Used to generate a BGREJ PDU of incorrect length		
Field Name	**Field Value**	**Comments**
UUandPAD	parUUandPAD	to generate a PDU of incorrect length
RESERVED1	’00000000’O	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0111’B	
RESERVED2	’000000’O	
Detailed Comments :		

TTCN PDU Constraint Declaration

Constraint Name : IVEND_S_INV(parUUandPAD:OCTETSTRING)
PDU Type : IVEND
Derivation Path :
Comments : Used to generate a END PDU of incorrect length

Field Name	Field Value	Comments
UUandPAD	parUUandPAD	to generate a PDU of incorrect length
RESERVED1	'00000000'O	
PL	'00'B	
RR	'0'B	
S	'0'B	
PDU_Type	'0011'B	
RESERVED2	'000000'O	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : IVENDAK_S_INV(parINVALID:OCTETSTRING)
PDU Type : IVENDAK
Derivation Path :
Comments : an ENDAK PDU of incorrect length

Field Name	Field Value	Comments
INVALID	parINVALID	
RESERVED1	'00000000'O	
RESERVED2	'0000'B	
PDU_Type	'0100'B	
RESERVED3	'000000'O	

Detailed Comments :

TTCN PDU Constraint Declaration		
Constraint Name : IVRS_S_INV(parUUandPAD:OCTETSTRING)		
PDU Type : IVRS		
Derivation Path :		
Comments : Used to generate a END PDU of incorrect length		
Field Name	**Field Value**	**Comments**
UUandPAD	parUUandPAD	to generate a PDU of incorrect length
RESERVED	’000000’O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
PL	’00’B	
RSVD	’00’B	
PDU_Type	’0101’B	
N_MR	INT_TO_BIT(VR_MR,24)	
Detailed Comments :		

TTCN PDU Constraint Declaration		
Constraint Name : IVRSAK_S_INV(parINVALID:OCTETSTRING)		
PDU Type : IVRSAK		
Derivation Path :		
Comments : an RSAK PDU of incorrect length		
Field Name	**Field Value**	**Comments**
INVALID	parINVALID	
RESERVED1	’00000000’O	
RESERVED2	’0000’B	
PDU_Type	’0110’B	
N_MR	INT_TO_BIT(VR_MR, 24)	
Detailed Comments :		

TTCN PDU Constraint Declaration

Constraint Name : IVER_S_INV(parINVALID:OCTETSTRING)
PDU Type : IVER
Derivation Path :
Comments : an ER PDU of incorrect length

Field Name	Field Value	Comments
INVALID	parINVALID	
RESERVED	'000000'O	
N_SQ	INT_TO_BIT(VT_SQ,8)	
RSVD	'0000'B	
PDU_Type	'1001'B	
N_MR	INT_TO_BIT(VR_MR,24)	

Detailed Comments :

TTCN PDU Constraint Declaration

Constraint Name : IVERAK_S_INV(parINVALID:OCTETSTRING)
PDU Type : IVERAK
Derivation Path :
Comments : an ERAK PDU of incorrect length

Field Name	Field Value	Comments
INVALID	parINVALID	
RESERVED	'00000000'O	
RSVD	'0000'B	
PDU_Type	'1111'B	
N_MR	INT_TO_BIT(VR_MR, 24)	

Detailed Comments :

IV

Dynamic Part

Test Case Dynamic Behaviour

Test Case Name : S1_V_A1
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT generates the BGN PDU on demand at state 1.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(5 of 51)/PICS PC11

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		<IUT!BGN>	BGN_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?BGN(VR_SQ:=BIT_TO_INT(BGN.N_SQ), VT_MS:=BIT_TO_INT(BGN.N_MR))	BGN_R_GEN		
5		+S2_VERIFY			
6		+postamble			return the IUT in STATE 1
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Opr			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_V_P1
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT sends a BGREJ PDU on reception of retransmitted BGN PDU.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(5 of 51)/PICS PC12

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?BGREJ	BGREJ_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_V_P2
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT goes to state 3 on reception of BGN PDU at state 1.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(5 and 11 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)<>VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN	(P)	assume a AA−ESTABLISH .response from SSCF UNI
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_V_P5
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 1.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(5 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!END	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_V_P6
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT ignores a ENDAK PDU and remains at state 1.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(5 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_V_P16
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 1.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_V_P17
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 1.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I1
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	BGN_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I2
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I3
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I4
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!END	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I6
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!RS	RS_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I10
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!SD	SD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I14
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I15
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I16

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	IVBGN_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I17

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGAK(VR_MR:=GET_VR_MR( ))	IVBGAK_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I18

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I19

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I20_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I20_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I21

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I22_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I22_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I23_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I23_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I24_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I24_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I25
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I26_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I26_2
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I27_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5,, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'00000000'O)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I27_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5,, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'0000'O)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I28_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I28_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I29

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I30

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IV_I31
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_CODE		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P3
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a BGAK PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(6 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_GEN		
3		START T_Wait			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P4
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT ignores a BGREJ PDU and remains at state 1.
Configuration :
Default :
Comments : Fig. 20(5 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P8
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a RS PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(7 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!RS(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	RS_S_GEN		
3		START Timer_CC			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P9
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a RSAK PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(7 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!RSAK(VR_MR:=GET_VR_MR())	RSAK_S_GEN		
3		START T_Wait			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P10
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a ER PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(5 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!ER(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	ER_S_GEN		
3		START Timer_CC			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P11
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a ERAK PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!ERAK(VR_MR:=GET_VR_MR())	ERAK_S_GEN		
3		START T_Wait			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P12
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a SD PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		
3		START T_Wait			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P13
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a POLL PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_GEN		
3		START T_Wait			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P14
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a STAT PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
3		START T_Wait			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S1_IO_P15
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a USTAT PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!USTAT(VR_MR:=GET_VR_MR())	USTAT_S_LIST(1,3, 1)		elements have no meaning
3		START T_Wait			
4	LB1	LT_PCO?END	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_A3
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT generates the END PDU on demand at state 2.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(9 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		<IUT!END>	END_R_USER		
3		START T_Opr			
4	LB1	LT_PCO?END	END_R_USER	(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Opr			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P1
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a retransmitted BGN PDU at state 2
Configuration :
Default :
Comments : Fig. 20(10 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P2
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT sends a BGAK PDU on reception of BGN PDU and goes to state 10.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(10 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)<>VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN	(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P3
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT goes to state 10 on reception of BGAK PDU at state 2.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?POLL	POLL_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P4
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 2.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P5
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a END PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!END	END_S_USER		
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P6
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a ENDAK PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P8
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a RS PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(10 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!RS(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	RS_S_GEN		
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P9
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a RSAK PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(10 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!RSAK(VR_MR:=GET_VR_MR())	RSAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P10
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a ER PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!ER(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	ER_S_GEN		
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P11
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a ERAK PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!ERAK(VR_MR:=GET_VR_MR())	ERAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P12
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a SD PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P13
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a POLL PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P14
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a STAT PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P15
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a USTAT PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!USTAT(VR_MR:=GET_VR_MR())	USTAT_S_LIST(1,3,1)		elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P16
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 2.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_V_P17
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 2.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I1
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	BGN_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I2
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I3
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I4
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!END	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I6
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!RS	RS_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I10
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!SD	SD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I14
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I15
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I16

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	IVBGN_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I17

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGAK(VR_MR:=GET_VR_MR( ))	IVBGAK_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I18

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I19

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I20_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I20_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I21

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I22_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I22_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I23_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I23_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I24_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I24_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I25

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I26_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I26_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I27_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'00000000'O)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I27_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'0000'O)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I28_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I28_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I29

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I30

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_IV_I31
Group : PC/STATE_2/INV/
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 2.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_CODE		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_A1
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT generates the BGN PDU on demand at state 4.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(14 of 51)/PICS PC11

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		<IUT!BGN>	BGN_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?BGN(VR_SQ:=BIT_TO_INT(BGN.N_SQ), VT_MS:=BIT_TO_INT(BGN.N_MR))	BGN_R_GEN		
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Opr			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P1
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT sends a BGAK and END PDU on reception of retransmitted BGN PDU at state 4.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(16 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN		
5		START T_Wait			
6	LB2	LT_PCO?END	END_R_GEN	(P)	resend the last END PDU sent
7		+S4_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB2			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB2			
13		+TS_Wait			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB1			
16		LT_PCO?UD	UD_R_GEN		
17		GOTO LB1			
18		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P2
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT goes to state 3 on reception of BGN PDU at state 4.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(16 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)<>VR(SQ) (s3)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN	(P)	(s10)
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P3
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a BGAK PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P4
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 4.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(15 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P5
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 4.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(15 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!END	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P6
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 4.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(15 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P8
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a RS PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(16 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!RS(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	RS_S_GEN		
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P9
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a RSAK PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(16 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!RSAK(VR_MR:=GET_VR_MR())	RSAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P10
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a ER PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(16 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!ER(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	ER_S_GEN		
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P11
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a ERAK PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(15 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!ERAK(VR_MR:=GET_VR_MR())	ERAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P12
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a SD PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P13
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a POLL PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P14
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a STAT PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P15
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a USTAT PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!USTAT(VR_MR:=GET_VR_MR())	USTAT_S_LIST(1,3,1)		elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P16
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 4.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_V_P17
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 4.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I1
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	BGN_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I2
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I3
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I4
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!END	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I6
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!RS	RS_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I10
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!SD	SD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I14
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I15
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I16

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	IVBGN_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I17

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGAK(VR_MR:=GET_VR_MR( ))	IVBGAK_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I18

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I19

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I20_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I20_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I21

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I22_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I22_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I23_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I23_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I24_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I24_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I25

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I26_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I26_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I27_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'00000000'O)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I27_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'0000'O)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I28_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I28_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I29

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I30

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_IV_I31
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_CODE		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_A3
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT generates the END PDU on demand at state 5.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(18 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		<IUT!END>	END_R_USER		
3		START T_Opr			
4	LB1	LT_PCO?END	END_R_USER	(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Opr			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P1
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT sends a BGAK and RS PDU on reception of retransmitted BGN PDU at state 5
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(17 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN		
5		START T_Wait			
6	LB2	LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ), VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)	(P)	
7		+S5_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB2			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB2			
13		+TS_Wait			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB1			
16		LT_PCO?UD	UD_R_GEN		
17		GOTO LB1			
18		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P2
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT goes to state 3 on reception of BGN PDU at state 5.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(17 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)<>VR(SQ)(s3)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN	(P)	(s10)
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P3
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a BGAK PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(19 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P5
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 5.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(17 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!END	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P7
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a retransmitted RS PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(19 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!RS(VR_MR:=GET_VR_MR())	RS_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P8
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT sends a RSAK PDU on reception of RS PDU and goes to state 10.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(19 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!RS(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	RS_S_GEN		N(SQ)<>VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?RSAK(VT_MS:=BIT_TO_INT(RSAK.N_MR))	RSAK_R_GEN	(P)	assume a AA−RESYNC.response from SSCF UNI
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P9
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT goes to state 10 on reception of RSAK PDU at state 5.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(19 of 51)/PICS PC6

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!RSAK(VR_MR:=GET_VR_MR())	RSAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?POLL	POLL_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P10
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a ER PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(17 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!ER(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	ER_S_GEN		
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P11
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a ERAK PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(19 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!ERAK(VR_MR:=GET_VR_MR())	ERAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P12
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a SD PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(19 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P13
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a POLL PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(17 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P14
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a STAT PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(18 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P15
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a USTAT PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(18 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!USTAT(VR_MR:=GET_VR_MR())	USTAT_S_LIST(1,3,1)		elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P16
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 5.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_V_P17
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 5.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I1
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	BGN_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I2
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I3
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I4
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!END	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I6
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!RS	RS_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I10
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!SD	SD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I14
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I15
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I16

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	IVBGN_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I17

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGAK(VR_MR:=GET_VR_MR( ))	IVBGAK_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I18

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I19

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I20_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I20_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I21

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I22_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I22_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I23_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I23_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I24_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I24_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I25

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I26_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I26_2
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I27_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'00000000'O)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I27_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'0000'O)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I28_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I28_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I29

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I30

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IV_I31
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_CODE		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IO_P4
Group : PC/STATE_5/INOP/
Purpose : Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 5.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(17 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_IO_P6
Group : PC/STATE_5/INOP/
Purpose : Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 5.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(17 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P2
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT goes to state 3 on reception of BGN PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(25 and 11 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)<>VR(SQ)(s3)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN	(P)	assume a AA−ESTABLISH .response from SSCF UNI (s10)
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P5
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT sends a ENDAK PDU and goes to state 1 on reception of a END PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(23 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!END	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P8
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT goes to state 6 on reception of RS PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(26 and 11 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!RS(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	RS_S_GEN		N(SQ)<>VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?RSAK(VT_MS:=BIT_TO_INT(RSAK.N_MR))	RSAK_R_GEN	(P)	assume a AA−RESYNC.response from SSCF UNI
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P11
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT sends a ERAK PDU and goes to state 8 on reception of a ER PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 i, Fig. 20(25 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!ER(VT_SQ:=INC_MOD_8(VT_SQ, 1),VR_MR:=GET_VR_MR())	ER_S_GEN		N(SQ)<>VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?ERAK(VT_MS:=BIT_TO_INT(ERAK.N_MR))	ERAK_R_GEN	(P)	assume a AA−RECOVER. response from SSCF UNI
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P12
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT goes to state 8 on reception of ERAK PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 i, Fig. 20(23 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!ERAK(VR_MR:=GET_VR_MR())	ERAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P19
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT ignores a SD PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(25 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P21
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT ignores a POLL PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(24 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P26
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT ignores a STAT PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(24 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P36
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT ignores a USTAT PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(24 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!USTAT(VR_MR:=GET_VR_MR())	USTAT_S_LIST(1,3,1)		elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P40
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 7.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_V_P41
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 7.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I1
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	BGN_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I2
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I3
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I4
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!END	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I6
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!RS	RS_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I10
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!SD	SD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I14
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I15
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I16

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	IVBGN_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I17

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGAK(VR_MR:=GET_VR_MR( ))	IVBGAK_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I18

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I19

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I20_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I20_2
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I21

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I22_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I22_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I23_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I23_2
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I24_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I24_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I25

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I26_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I26_2
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I27_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'00000000'O)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I27_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'0000'O)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I28_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I28_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I29

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I30

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IV_I31
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_CODE		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IO_P1
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT ignores a retransmitted BGN PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(25 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IO_P3
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT ignores a BGAK PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(23 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IO_P4
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(23 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IO_P6
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(23 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IO_P7
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT ignores a retransmitted RS PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(19 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!RS(VR_MR:=GET_VR_MR())	RS_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IO_P9
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT ignores a RSAK PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(23 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!RSAK(VR_MR:=GET_VR_MR())	RSAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_IO_P10
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT ignores a retransmitted ER PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(25 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!ER(VR_MR:=GET_VR_MR())	ER_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_A3
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, generates the END PDU on demand.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(34 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!END>	END_R_USER		
3		START T_Opr			
4	LB1	LT_PCO?END	END_R_USER	(P)	
5		+S4_VERIFY			
6		+postamble			return the IUT in STATE 1
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Opr			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_A5
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, generates the RS PDU on demand.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(34 of 51)/PICS PC6

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!RS>	RS_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ), VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_GEN	(P)	
5		+S5_VERIFY			
6		+postamble			return the IUT in STATE 1
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Opr			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P1
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a BGAK PDU on reception of a retransmitted BGN PDU.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(35 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN	(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?POLL	POLL_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P2
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, goes to state 3 on reception of BGN PDU.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(35 and 11 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())	BGN_S_GEN		N(SQ)<>VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN	(P)	assume a AA−ESTABLISH .response from SSCF UNI
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P3
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, ignores a BGAK PDU and remains.
Configuration :
Default :
Comments : Fig. 20(34 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P5
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a ENDAK PDU and goes to state 1 on reception of a END PDU.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(36 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!END	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P7
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a RSAK PDU on reception of a retransmitted RS PDU.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(36 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!RS(VR_MR:=GET_VR_MR())	RS_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?RSAK(VT_MS:=BIT_TO_INT(RSAK.N_MR))	RSAK_R_GEN	(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?POLL	POLL_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P8
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, goes to state 6 on reception of RS PDU.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(36 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!RS(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	RS_S_GEN		N(SQ)<>VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?RSAK(VT_MS:=BIT_TO_INT(RSAK.N_MR))	RSAK_R_GEN	(P)	assume a AA−RESYNC.response from SSCF UNI
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?POLL	POLL_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P9
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, ignores a RSAK PDU and remains.
Configuration :
Default :
Comments : Fig. 20(34 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!RSAK(VR_MR:=GET_VR_MR())	RSAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P10
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a ERAK PDU on reception of a retransmitted ER PDU.
Configuration :
Default :
Comments : Fig. 20(35 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!ER(VR_MR:=GET_VR_MR())	ER_S_GEN		N(SQ)=VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?ERAK(VT_MS:=BIT_TO_INT(ERAK.N_MR))	ERAK_R_GEN	(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?POLL	POLL_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P11
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, goes to state 9 on reception of ER PDU.
Configuration :
Default :
Comments : Ref. 5.0 i, Fig. 20(35 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!ER(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	ER_S_GEN		N(SQ)<>VR(SQ)
3		START Timer_CC			
4	LB1	LT_PCO?ERAK(VT_MS:=BIT_TO_INT(ERAK.N_MR))	ERAK_R_GEN	(P)	assume a AA−RECOVER. response from SSCF UNI
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?POLL	POLL_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_CC			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P12
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, ignores a ERAK PDU and remains.
Configuration :
Default :
Comments : Fig. 20(34 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!ERAK(VR_MR:=GET_VR_MR())	ERAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_V_P13
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a USTAT PDU on reception of SD PDU out of the window.
Configuration :
Default :
Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		VR(R)=VR(H)=1
3		LT_PCO!SD	SD_S_N_S(VT_MS+2)		SD.N(S)>=VR(MR)
4		START T_Wait			
5	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT(USTAT.N_MR))	USTAT_R_LIST(VT_S+1, VT_MS, VT_S+1)	(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_Wait			

Detailed Comments : SD.N(S)>=VR(MR), VR(H)<VR(MR)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P14
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, ignores a SD PDU that is out of the window when window is not available.
Configuration :
Default :
Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		VR(R)=VR(H)=1
3		LT_PCO!SD	SD_S_N_S(VT_MS+2)		
4		START T_Wait			
5	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT (USTAT.N_MR))	USTAT_R_LIST(VT_S+1, VT_MS, VT_S+1)		VR(H)=VR(MR)
6		LT_PCO!SD	SD_S_N_S(VT_MS+2)		SD.N(S)>=VR(MR)
7		START T_Wait			
8	LB2	?TIMEOUT T_Wait		(P)	
9		+S10_VERIFY			
10		+postamble			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB2			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB2			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB2			
17		LT_PCO?OTHERWISE		(F)	
18		+postamble			
19		LT_PCO?POLL	POLL_R_GEN		
20		GOTO LB1			
21		LT_PCO?MD	MD_R_GEN		
22		GOTO LB1			
23		LT_PCO?UD	UD_R_GEN		
24		GOTO LB1			
25		+TS_Wait			

Detailed Comments : SD.N(S)>=VR(MR), VR(H)>=VR(MR)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P15
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, saves the next highest expected SD PDU.
Configuration :
Default :
Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_N_S(VT_S+2)		SD.N(S)>VR(H) IUT saves this SD PDU
3		START T_Wait			
4	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT(USTAT.N_MR))	USTAT_R_LIST(VT_S, VT_S+2,VT_S)		VR(R)=0, VR(H)=3
5		LT_PCO!SD	SD_S_N_S(VT_S+3)		SD.N(S)=VR(H) IUT saves this SD PDU
6		LT_PCO!SD	SD_S_N_S(VT_S)		IUT indicate PDU(0) VR(R)=1, VR(H)=4
7		LT_PCO!SD	SD_S_N_S(VT_S+1)		IUT indicate PDUs(1,2,3) VR(R)=4, VR(H)=4
8		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_N_S(VT_S+4)		
9		START T_Wait			
10	LB2	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)](VT_MS:=BIT_TO_INT(STAT.N_MR))	STAT_R_N_R(VT_S+4)	(P)	list_length=0
11		+S10_VERIFY			
12		+postamble			
13		LT_PCO?POLL	POLL_R_GEN		
14		GOTO LB2			
15		LT_PCO?MD	MD_R_GEN		
16		GOTO LB2			
17		LT_PCO?UD	UD_R_GEN		
18		GOTO LB2			
19		+TS_Wait			
20		LT_PCO?POLL	POLL_R_GEN		
21		GOTO LB1			
22		LT_PCO?MD	MD_R_GEN		
23		GOTO LB1			
24		LT_PCO?UD	UD_R_GEN		
25		GOTO LB1			
26		+TS_Wait			

Detailed Comments : SD.N(S)<VR(MR), SD.N(S)<>VR(R),SD.N(S)=VR(H)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P17

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, saves a SD PDU that sequence number is between the sequence number of the next in sequence and the next highest expected SD PDUs.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_N_S(VT_S+2)		SD.N(S)>VR(H) IUT saves this SD PDU
3		START T_Wait			
4	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT(USTAT.N_MR))	USTAT_R_LIST(VT_S, VT_S+2,VT_S)		VR(R)=0, VR(H)=3
5		LT_PCO!SD	SD_S_N_S(VT_S+1)		SD.N(S)<VR(H) IUT saves this SD PDU
6		LT_PCO!SD	SD_S_N_S(VT_S)		IUT indicate PDU(0,1,2) VR(R)=3, VR(H)=3
7		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_N_S(VT_S+3)		
8		START T_Wait			
9	LB2	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)](VT_MS:=BIT_TO_INT(STAT.N_MR))	STAT_R_N_R(VT_S+3)	(P)	list_length=0
10		+S10_VERIFY			
11		+postamble			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB2			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB2			
16		LT_PCO?UD	UD_R_GEN		
17		GOTO LB2			
18		+TS_Wait			
19		LT_PCO?POLL	POLL_R_GEN		
20		GOTO LB1			
21		LT_PCO?MD	MD_R_GEN		
22		GOTO LB1			
23		LT_PCO?UD	UD_R_GEN		
24		GOTO LB1			
25		+TS_Wait			

Detailed Comments : SD.N(S)<VR(MR), SD.N(S)<>VR(R), SD.N(S)<VR(H), SD.N(S) not in RX BUFFER

Test Case Dynamic Behaviour

Test Case Name : S10_V_P18

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU on reception of a SD PDU that sequence number is between the sequence number of the next in sequence and the next highest expected SD PDUs and is already in RX BUFFER.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_N_S(VT_S+2)		SD.N(S)>VR(H) IUT saves this SD PDU
3		START T_Wait			
4	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT(USTAT.N_MR))	USTAT_R_LIST(VT_S, VT_S+2, VT_S)		VR(R)=0, VR(H)=3
5		LT_PCO!SD	SD_S_N_S(VT_S+2)		SD.N(S)<VR(H) this PDU is already in RX BUFFER
6		START T_Wait			
7	LB2	LT_PCO?ER(VR_SQ:=BIT_TO_INT (ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
8		+S7_VERIFY			
9		+postamble			
10		LT_PCO?POLL	POLL_R_GEN		
11		GOTO LB2			
12		LT_PCO?MD	MD_R_GEN		
13		GOTO LB2			
14		LT_PCO?UD	UD_R_GEN		
15		GOTO LB2			
16		+TS_Wait			
17		LT_PCO?POLL	POLL_R_GEN		
18		GOTO LB1			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB1			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB1			
23		+TS_Wait			

Detailed Comments : SD.N(S)<VR(MR), SD.N(S)<>VR(R), SD.N(S)<VR(H), SD.N(S) in RX BUFFER

Test Case Dynamic Behaviour

Test Case Name : S10_V_P19
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, accepts the next in sequence SD PDU.
Configuration :
Default :
Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		SD.N(S)=VR(R) =VR(H)
3		(VT_S:=INC_MOD_24(VT_S,1))			
4		LT_PCO!SD	SD_S_GEN		SD.N(S)=VR(R) =VR(H)
5		(VT_S:=INC_MOD_24(VT_S,1))			
6		LT_PCO!POLL(VT_PS:=INC_MOD_ 24(VT_PS,1))	POLL_S_GEN		
7		START T_Wait			
8	LB1	LT_PCO?STAT[CHECK_N_PS(V T_PA,BIT_TO_INT(STAT.N_PS),V T_PS)](VT_MS:=BIT_TO_INT(STA T.N_MR))	STAT_R_N_R(VT_S)	(P)	list_length=0
9		+S10_VERIFY			
10		+postamble			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB1			
17		+TS_Wait			

Detailed Comments : SD.N(S)<VR(MR), SD.N(S)=VR(R)=VR(H)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P21
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a ER PDU on reception of a POLL PDU that sequence number is less than that of the next highest expected SD PDU.
Configuration :
Default :
Comments : Ref. 5.0 i, Fig. 20(41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		VT_S=0
3		(VT_S:=INC_MOD_24(VT_S,1))			
4		LT_PCO!SD	SD_S_GEN		VT_S=1
5		(VT_S:=INC_MOD_24(VT_S,1))			
6		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_N_S(VT_S−2)		POLL.N(S)<VR(H)
7		START T_Wait			
8	LB1	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
9		+S7_VERIFY			
10		+postamble			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB1			
17		+TS_Wait			

Detailed Comments : POLL.N(S)<VR(H)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P22

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a STAT PDU on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41 and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_N_S(VT_MS+2)		POLL.N(S)>=VR(H),POLL.N(S)>VR(MR),VR(R)=VR(H)
3		START T_Wait			
4		(TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_MS))			
5	LB1	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)]	STAT_R_LIST(TCV_LIST, VT_S)	(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_Wait			

Detailed Comments : POLL.N(S)>=VR(H), POLL.N(S)>VR(MR), VR(R)=VR(H)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P23_1
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a STAT PDU on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.
Configuration :
Default :
Comments : Ref. 5.0 a, h, Fig. 20(41and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		send SD(0)
3		(VT_S:=INC_MOD_24(VT_S,1))			
4		LT_PCO!SD	SD_S_N_S(VT_S+3)		send SD(4)
5		START T_Wait			
6	LB1	LT_PCO?USTAT	USTAT_R_LIST(VT_S,VT_S+3,VT_S)		
7		(TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+3), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+4))			element1=1 element2=4 element3=5
8		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_N_S(VT_S+4)		POLL(5)
9		START T_Wait			
10	LB2	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)]	STAT_R_LIST(TCV_LIST, VT_S)	(P)	
11		+S10_VERIFY			
12		+postamble			
13		LT_PCO?POLL	POLL_R_GEN		
14		GOTO LB2			
15		LT_PCO?MD	MD_R_GEN		
16		GOTO LB2			
17		LT_PCO?UD	UD_R_GEN		
18		GOTO LB2			
19		+TS_Wait			
20		LT_PCO?POLL	POLL_R_GEN		
21		GOTO LB1			
22		LT_PCO?MD	MD_R_GEN		
23		GOTO LB1			
24		LT_PCO?UD	UD_R_GEN		
25		GOTO LB1			
26		+TS_Wait			

Detailed Comments : POLL.N(S)>=VR(H), POLL.N(S)>VR(MR), VR(R)<VR(H)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P23_2

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a STAT PDUs(with segmenting) on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41 and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(count:=0)			
3		LT_PCO!SD	SD_S_GEN		send SD(0)
4		(TCV_LIST:=APPEND_LIST(TCV_LIST, VT_S+1), count:=count+1)			LE=1
5	LB1	LT_PCO!SD(VT_S:=INC_MOD_24(VT_S,2))	SD_S_GEN		send SD(2,4,...)
6		START T_Wait			
7	LB4	LT_PCO?USTAT	USTAT_R_LIST(VT_S−1, VT_S, VT_S−1)		
8		(TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+1))			LE=2,4, ... LE=3,5, ...
9		(count:=count+2)			
10		[count<Max_STAT]			
11		GOTO LB1			
12		[count>=Max_STAT]			
13		LT_PCO!SD(VT_S:=INC_MOD_24(VT_S,2))	SD_S_GEN		send SD(x+2)
14		(TCV_LIST1:=APPEND_LIST(TCV_LIST1,VT_S), TCV_LIST1:=APPEND_LIST(TCV_LIST1,VT_S+1), TCV_LIST1:=APPEND_LIST(TCV_LIST1,VT_S+2))			LE=X+1 LE=x+2 LE=VT_MS
15		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_N_S(VT_S+2)		
16		START T_Wait			
17	LB2	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)]	STAT_R_LIST(TCV_LIST, 1)		
18		START T_Wait			
19	LB3	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)]	STAT_R_LIST(TCV_LIST1, 1)	(P)	
20		+S10_VERIFY			
21		+postamble			
22		LT_PCO?POLL	POLL_R_GEN		

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Test Case Dynamic Behaviour					
Nr	**Label**	**Behaviour Description**	**Constraints Ref**	**Verdict**	**Comments**
23		GOTO LB3			
24		LT_PCO?MD	MD_R_GEN		
25		GOTO LB3			
26		LT_PCO?UD	UD_R_GEN		
27		GOTO LB3			
28		+TS_Wait			
29		LT_PCO?POLL	POLL_R_GEN		
30		GOTO LB2			
31		LT_PCO?MD	MD_R_GEN		
32		GOTO LB2			
33		LT_PCO?UD	UD_R_GEN		
34		GOTO LB2			
35		+TS_Wait			
36		LT_PCO?POLL	POLL_R_GEN		
37		GOTO LB4			
38		LT_PCO?MD	MD_R_GEN		
39		GOTO LB4			
40		LT_PCO?UD	UD_R_GEN		
41		GOTO LB4			
42		LT_PCO?OTHERWISE		(I)	
43		+postamble			
44		?TIMEOUT T_Wait			
45		+postamble		(I)	
Detailed Comments : POLL.N(S)>=VR(H), POLL.N(S)>VR(MR), VR(R)<VR(H)					

Test Case Dynamic Behaviour

Test Case Name : S10_V_P24

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10 and having no missing gap of received SD PDUs, sends a STAT PDU on reception of a POLL PDU that sequence number is less than or equal to that of the next highest expected SD PDU and is within the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41 and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		send SD(0)
3		LT_PCO!SD	SD_S_N_S(VT_S+1)		send SD(1)
4		LT_PCO!SD	SD_S_N_S(VT_S+2)		send SD(2)
5		LT_PCO!POLL(VT_PS:=INC_MOD_24 (VT_PS,1))	POLL_S_N_S(VT_S+3)		POLL.N(S)>=VR (H),POLL.N(S), =VR(MR),VR(R) =VR(H)
6		START T_Wait			
7	LB1	LT_PCO?STAT[CHECK_N_PS(VT _PA,BIT_TO_INT(STAT.N_PS),VT_ PS)]	STAT_R_N_R(VT_S+3)	(P)	STAT.LIST=null STAT.N_R=3
8		+S10_VERIFY			
9		+postamble			
10		LT_PCO?POLL	POLL_R_GEN		
11		GOTO LB1			
12		LT_PCO?MD	MD_R_GEN		
13		GOTO LB1			
14		LT_PCO?UD	UD_R_GEN		
15		GOTO LB1			
16		+TS_Wait			

Detailed Comments : POLL.N(S)>=VR(H), POLL.N(S)<=VR(MR), VR(R)=VR(H)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P25

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10 and having a missing gap of received SD PDU, sends a STAT PDU on reception of a POLL PDU that sequence number is less than or equal to that of the next highest expected SD PDU and is within the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41 and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		send SD(0)
3		LT_PCO!SD	SD_S_N_S(VT_S+1)		send SD(1)
4		LT_PCO!SD	SD_S_N_S(VT_S+3)		send SD(3)
5		START T_Wait			
6	LB1	LT_PCO?USTAT	USTAT_R_LIST(VT_S+2,VT_S+3,VT_S+2)		
7		CANCEL T_Wait			
8		(TCV_LIST:=APPEND_LIST(TCV_LIST1,VT_S+2), TCV_LIST:=APPEND_LIST(TCV_LIST1,VT_S+3), TCV_LIST:=APPEND_LIST(TCV_LIST1,VT_S+4))			LE=X+1 LE=x+2 LE=VT_MS
9		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_N_S(VT_S+4)		POLL.N(S)>=VR(H),POLL.N(S),=VR(MR),VR(R)<VR(H)
10		START T_Wait			
11	LB2	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)]	STAT_R_LIST(TCV_LIST, VT_S+2)	(P)	POLL.LIST=null POLL.N_R=3
12		+S10_VERIFY			
13		+postamble			
14		LT_PCO?POLL	POLL_R_GEN		
15		GOTO LB2			
16		LT_PCO?MD	MD_R_GEN		
17		GOTO LB2			
18		LT_PCO?UD	UD_R_GEN		
19		GOTO LB2			
20		+TS_Wait			
21		LT_PCO?POLL	POLL_R_GEN		
22		GOTO LB1			
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB1			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB1			
27		+TS_Wait			

Detailed Comments : POLL.N(S)>=VR(H), POLL.N(S)<=VR(MR), VR(R)<VR(H)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P26

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number is incorrect.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(44 and 41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			VT(PA)=0 VT(PS)=0
2		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,3,VR_R)		STAT.N(PS)=3
3		START T_Wait			
4	LB1	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?POLL	POLL_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_Wait			

Detailed Comments : not(VT(PA)<=STAT.N(PS)<=VT(PS))

Test Case Dynamic Behaviour

Test Case Name : S10_V_P27

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number is correct but SD PDU sequence number is incorrect.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(44 and 41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			VT(PA)=0 VT(PS)=0
2		<IUT!POLL>	POLL_R_GEN		VT(PA)=1 VT(PS)=1
3		START T_Opr			
4	LB1	LT_PCO?POLL(TCV_N_PS:=BIT_TO_INT(POLL.N_PS))	POLL_R_GEN		
5		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,3)		STAT.N(R)=3
6		START T_Wait			
7	LB2	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
8		+S7_VERIFY			
9		+postamble			
10		LT_PCO?POLL	POLL_R_GEN		
11		GOTO LB2			
12		LT_PCO?MD	MD_R_GEN		
13		GOTO LB2			
14		LT_PCO?UD	UD_R_GEN		
15		GOTO LB2			
16		+TS_Wait			
17		LT_PCO?MD	MD_R_GEN		
18		GOTO LB1			
19		LT_PCO?UD	UD_R_GEN		
20		GOTO LB1			
21		+TS_Opr			

Detailed Comments : VT(PA)<=STAT.N(PS)<=VT(PS), not(VT(A)<=STAT.N(R)<=VT(S))

Test Case Dynamic Behaviour

Test Case Name : S10_V_P32

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number and SD PDU sequence number are correct but its list element has incorrect sequence number.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(44, 45 and 41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			VT(PA)=0 VT(PS)=0
2		<IUT!POLL>	POLL_R_GEN		VT(PA)=1 VT(PS)=1
3		START T_Opr			
4	LB1	LT_PCO?POLL(TCV_N_PS:=BIT_TO_INT(POLL.N_PS))	POLL_R_GEN		
5		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list element has incorrect sequence number(>VT(S))
6		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_R)		
7		START T_Wait			
8	LB2	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
9		+S7_VERIFY			
10		+postamble			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB2			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB2			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB2			
17		+TS_Wait			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB1			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB1			
22		+TS_Opr			

Detailed Comments : VT(PA)<=STAT.N(PS)<=VT(PS), VT(A)<=STAT.N(R)<=VT(S), list element<=VT(S)

Test Case Dynamic Behaviour

Test Case Name : S10_V_P33

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number and SD PDU sequence number are correct but its list elements are not increasing order.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(44, 45 and 41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!SD>	SD_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
5		<IUT!SD>	SD_R_GEN		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
8		<IUT!SD>	SD_R_GEN		
9		START T_Opr			
10	LB3	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
11		<IUT!POLL>	POLL_R_GEN		
12		START T_Opr			
13	LB4	LT_PCO?POLL(TCV_N_PS:=BIT_TO_INT(POLL.N_PS))	POLL_R_GEN		
14		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R−1), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R−2))			list elements are not increasing order
15		LT_PCO!STAT(VR_MR:=GET_VR_MR())	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_R)		
16		START T_Wait			
17	LB5	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
18		+S7_VERIFY			
19		+postamble			
20		LT_PCO?POLL	POLL_R_GEN		
21		GOTO LB5			
22		LT_PCO?MD	MD_R_GEN		
23		GOTO LB5			
24		LT_PCO?UD	UD_R_GEN		
25		GOTO LB5			

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Test Case Dynamic Behaviour					
Nr	**Label**	**Behaviour Description**	**Constraints Ref**	**Verdict**	**Comments**
26		+TS_Wait			
27		LT_PCO?MD	MD_R_GEN		
28		GOTO LB4			
29		LT_PCO?UD	UD_R_GEN		
30		GOTO LB4			
31		+TS_Opr			
32		LT_PCO?POLL	POLL_R_GEN		
33		GOTO LB3			
34		LT_PCO?MD	MD_R_GEN		
35		GOTO LB3			
36		LT_PCO?UD	UD_R_GEN		
37		GOTO LB3			
38		+TS_Opr			
39		LT_PCO?POLL	POLL_R_GEN		
40		GOTO LB2			
41		LT_PCO?MD	MD_R_GEN		
42		GOTO LB2			
43		LT_PCO?UD	UD_R_GEN		
44		GOTO LB2			
45		+TS_Opr			
46		LT_PCO?POLL	POLL_R_GEN		
47		GOTO LB1			
48		LT_PCO?MD	MD_R_GEN		
49		GOTO LB1			
50		LT_PCO?UD	UD_R_GEN		
51		GOTO LB1			
52		+TS_Opr			
Detailed Comments : VT(PA)<=STAT.N(PS)<=VT(PS), VT(A)<=STAT.N(R)<=VT(S), list element n >= list element n+1					

Test Case Dynamic Behaviour

Test Case Name : S10_V_P38_1
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list element has incorrect sequence number.
Configuration :
Default :
Comments : Ref. 5.0 i, Fig. 20(43 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!SD>	SD_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
5		<IUT!SD>	SD_R_GEN		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
8		<IUT!SD>	SD_R_GEN		
9		START T_Opr			
10	LB3	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
11		LT_PCO!USTAT(VR_MR:=GET_VR_MR())	USTAT_S_LIST(VR_R+1,VR_R+2,VR_R−1)		list element has incorrect sequence number
12		START T_Wait			
13	LB4	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
14		+S7_VERIFY			
15		+postamble			
16		LT_PCO?POLL	POLL_R_GEN		
17		GOTO LB4			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB4			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB4			
22		+TS_Wait			
23		LT_PCO?POLL	POLL_R_GEN		
24		GOTO LB3			
25		LT_PCO?MD	MD_R_GEN		
26		GOTO LB3			
27		LT_PCO?UD	UD_R_GEN		
28		GOTO LB3			
29		+TS_Opr			
30		LT_PCO?POLL	POLL_R_GEN		

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Test Case Dynamic Behaviour					
Nr	**Label**	**Behaviour Description**	**Constraints Ref**	**Verdict**	**Comments**
31		GOTO LB2			
32		LT_PCO?MD	MD_R_GEN		
33		GOTO LB2			
34		LT_PCO?UD	UD_R_GEN		
35		GOTO LB2			
36		+TS_Opr			
37		LT_PCO?POLL	POLL_R_GEN		
38		GOTO LB1			
39		LT_PCO?MD	MD_R_GEN		
40		GOTO LB1			
41		LT_PCO?UD	UD_R_GEN		
42		GOTO LB1			
43		+TS_Opr			
Detailed Comments : VT(PA)<=STAT.N(PS)<=VT(PS), VT(A)<=STAT.N(R)<=VT(S), list element n >= list element n+1					

Test Case Dynamic Behaviour

Test Case Name : S10_V_P38_2
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list elements are not increasing order.
Configuration :
Default :
Comments : Ref. 5.0 i, Fig. 20(43 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!SD>	SD_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
5		<IUT!SD>	SD_R_GEN		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
8		<IUT!SD>	SD_R_GEN		
9		START T_Opr			
10	LB3	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
11		LT_PCO!USTAT(VR_MR:=GET_VR_MR())	USTAT_S_LIST(VR_R−1,VR_R−2,VR_R−1)		
12		START T_Wait			
13	LB4	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
14		+S7_VERIFY			
15		+postamble			
16		LT_PCO?POLL	POLL_R_GEN		
17		GOTO LB4			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB4			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB4			
22		+TS_Wait			
23		LT_PCO?POLL	POLL_R_GEN		
24		GOTO LB3			
25		LT_PCO?MD	MD_R_GEN		
26		GOTO LB3			
27		LT_PCO?UD	UD_R_GEN		
28		GOTO LB3			
29		+TS_Opr			
30		LT_PCO?POLL	POLL_R_GEN		
31		GOTO LB2			

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Test Case Dynamic Behaviour					
Nr	**Label**	**Behaviour Description**	**Constraints Ref**	**Verdict**	**Comments**
32		LT_PCO?MD	MD_R_GEN		
33		GOTO LB2			
34		LT_PCO?UD	UD_R_GEN		
35		GOTO LB2			
36		+TS_Opr			
37		LT_PCO?POLL	POLL_R_GEN		
38		GOTO LB1			
39		LT_PCO?MD	MD_R_GEN		
40		GOTO LB1			
41		LT_PCO?UD	UD_R_GEN		
42		GOTO LB1			
43		+TS_Opr			
Detailed Comments : VT(PA)<=STAT.N(PS)<=VT(PS), VT(A)<=STAT.N(R)<=VT(S), list element n >= list element n+1					

Test Case Dynamic Behaviour

Test Case Name : S10_V_P39
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that SD PDU sequence number is incorrect.
Configuration :
Default :
Comments : Ref. 5.0 i, Fig. 20(43 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!SD>	SD_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
5		<IUT!SD>	SD_R_GEN		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
8		<IUT!SD>	SD_R_GEN		
9		START T_Opr			
10	LB3	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
11		LT_PCO!USTAT(VR_MR:=GET_VR_MR())	USTAT_S_LIST(VR_R−1,VR_R,VR_R+1)		USTAT.N(R) > VT(S)
12		START T_Wait			
13	LB4	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN	(P)	
14		+S7_VERIFY			
15		+postamble			
16		LT_PCO?POLL	POLL_R_GEN		
17		GOTO LB4			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB4			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB4			
22		+TS_Wait			
23		LT_PCO?POLL	POLL_R_GEN		
24		GOTO LB3			
25		LT_PCO?MD	MD_R_GEN		
26		GOTO LB3			
27		LT_PCO?UD	UD_R_GEN		
28		GOTO LB3			
29		+TS_Opr			
30		LT_PCO?POLL	POLL_R_GEN		
31		GOTO LB2			

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Test Case Dynamic Behaviour					
Nr	**Label**	**Behaviour Description**	**Constraints Ref**	**Verdict**	**Comments**
32		LT_PCO?MD	MD_R_GEN		
33		GOTO LB2			
34		LT_PCO?UD	UD_R_GEN		
35		GOTO LB2			
36		+TS_Opr			
37		LT_PCO?POLL	POLL_R_GEN		
38		GOTO LB1			
39		LT_PCO?MD	MD_R_GEN		
40		GOTO LB1			
41		LT_PCO?UD	UD_R_GEN		
42		GOTO LB1			
43		+TS_Opr			
Detailed Comments : USTAT.N(R) > VT(S)					

Test Case Dynamic Behaviour					
Test Case Name : S10_V_P40					
Group : PC/STATE_10/VAL/					
Purpose : Verify that the IUT accepts a UD PDU at state 10.					
Configuration :					
Default :					
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2					
Nr	**Label**	**Behaviour Description**	**Constraints Ref**	**Verdict**	**Comments**
1		+S10_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			
Detailed Comments :					

Test Case Dynamic Behaviour

Test Case Name : S10_V_P41
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 10.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I1
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	BGN_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I2
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I3
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I4
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!END	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I6
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!RS	RS_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I10
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I14
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I15
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I16

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGN(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())	IVBGN_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I17

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGAK(VR_MR:=GET_VR_MR( ))	IVBGAK_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I18

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I19

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I20_1
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I20_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I21

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I22_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I22_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I23_1
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I23_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I24_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I24_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I25

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I26_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I26_2
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I27_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'00000000'O)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I27_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list elements have no meaning
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_LIST,'0000'O)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I28_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I28_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I29

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I30

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=GEN_OCTET(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IV_I31
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_CODE		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IO_P4
Group : PC/STATE_10/INOP/
Purpose : Verify that the IUT, at state 10, goes to state 1 on reception of BGREJ PDU.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(36 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IO_P6
Group : PC/STATE_10/INOP/
Purpose : Verify that the IUT, at state 10, goes to state 1 on reception of ENDAK PDU.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(36 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S2_CC_T1
Group : SP/TIMER/
Purpose : Verify that the IUT, at state 2, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.
Configuration :
Default :
Comments : Ref. 5.0 g, 7.6 d, Fig. 20(9 of 51)/PICS SP1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(count:=1)			
3	LB1	START Timer_CC			
4		?TIMEOUT Timer_CC			
5		START T_Wait			
6	LB2	LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		identical to the last BGN PDU
7		CANCEL T_Wait			
8		(count:=count+1)			
9		[count < Max_CC]			
10		GOTO LB1			
11		[count >=Max_CC]			
12		START Timer_CC			
13		?TIMEOUT Timer_CC			
14		START T_Wait			
15	LB3	LT_PCO?END	END_R_SSCOP	(P)	
16		+S1_VERIFY			
17		+postamble			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB3			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB3			
22		+TS_Wait			
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB2			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB2			
27		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S4_CC_T1
Group : SP/TIMER/
Purpose : Verify that the IUT, at state 4, goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.
Configuration :
Default :
Comments : Ref. 5.0 g, 7.6 d, Fig. 20(15 of 51)/PICS SP1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(count:=1)			
3	LB1	START Timer_CC			
4		?TIMEOUT Timer_CC			
5		START T_Wait			
6	LB2	LT_PCO?END	END_R_USER		identical to the last END PDU
7		CANCEL T_Wait			
8		(count:=count+1)			
9		[count < Max_CC]			
10		GOTO LB1			
11		[count >=Max_CC]			
12		START Timer_CC			
13		?TIMEOUT Timer_CC			
14		+S1_VERIFY			
15		+postamble			
16		LT_PCO?MD	MD_R_GEN		
17		GOTO LB2			
18		LT_PCO?UD	UD_R_GEN		
19		GOTO LB2			
20		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S5_CC_T1
Group : SP/TIMER/
Purpose : Verify that the IUT, at state 5, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.
Configuration :
Default :
Comments : Ref. 5.0 g, 7.6 d, Fig. 20(18 of 51)/PICS SP1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(count:=1)			
3	LB1	START Timer_CC			
4		?TIMEOUT Timer_CC			
5		START T_Wait			
6	LB2	LT_PCO?RS	RS_R_RET(VR_SQ,VT_MS)		identical to the last RS PDU
7		CANCEL T_Wait			
8		(count:=count+1)			
9		[count < Max_CC]			
10		GOTO LB1			
11		[count >=Max_CC]			
12		START Timer_CC			
13		?TIMEOUT Timer_CC			
14		START T_Wait			
15	LB3	LT_PCO?END	END_R_SSCOP	(P)	
16		+S1_VERIFY			
17		+postamble			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB3			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB3			
22		+TS_Wait			
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB2			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB2			
27		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S7_CC_T1
Group : SP/TIMER/
Purpose : Verify that the IUT, at state 7, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.
Configuration :
Default :
Comments : Ref. 5.0 g, 7.6 d, Fig. 20(24 of 51)/PICS SP1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(count:=1)			
3	LB1	START Timer_CC			
4		?TIMEOUT Timer_CC			
5		START T_Wait			
6	LB2	LT_PCO?ER	ER_R_RET(VR_SQ,VT_MS)		identical to the last ER PDU
7		CANCEL T_Wait			
8		(count:=count+1)			
9		[count < Max_CC]			
10		GOTO LB1			
11		[count >=Max_CC]			
12		START Timer_CC			
13		?TIMEOUT Timer_CC			
14		START T_Wait			
15	LB3	LT_PCO?END	END_R_SSCOP	(P)	
16		+S1_VERIFY			
17		+postamble			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB3			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB3			
22		+TS_Wait			
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB2			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB2			
27		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_POLL_T3
Group : SP/TIMER/
Purpose : Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_POLL is expired .
Configuration :
Default :
Comments : Ref. 7.6 a, Fig. 20(37 of 51)/PICS SP5

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		START Timer_POLL			
3		?TIMEOUT Timer_POLL			
4		START T_Wait			
5	LB1	LT_PCO?POLL	POLL_R_GEN	(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_KEEP_ALIVE_T4
Group : SP/TIMER/
Purpose : Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_KEEP_ALIVE is expired .
Configuration :
Default :
Comments : Ref. 7.6 b, Fig. 20(37 of 51)/PICS SP6

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		START Timer_POLL			
3		?TIMEOUT Timer_POLL			
4		START T_Wait			
5	LB1	LT_PCO?POLL	POLL_R_GEN		
6		CANCEL T_Wait			
7		START Timer_KEEP_ALIVE			
8		?TIMEOUT Timer_KEEP_ALIVE			
9		START T_Wait			
10	LB2	LT_PCO?POLL	POLL_R_GEN	(P)	
11		+S10_VERIFY			
12		+postamble			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB2			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB2			
17		+TS_Wait			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB1			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB1			
22		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_IDLE_T5
Group : SP/TIMER/
Purpose : Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_IDLE is expired .
Configuration :
Default :
Comments : Ref. 7.6 c, Fig. 20(37 of 51)/PICS SP8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		START Timer_POLL			
3		?TIMEOUT Timer_POLL			
4		START T_Wait			
5	LB1	LT_PCO?POLL(TCV_N_PS:= BIT_TO_INT(POLL.N_PS))	POLL_R_GEN		IUT start Timer_KEEP_ALIVE
6		CANCEL T_Wait			
7		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_R)		IUT start Timer_IDLE
8		START Timer_IDLE			
9		?TIMEOUT Timer_IDLE			
10		START T_Wait			
11	LB2	LT_PCO?POLL	POLL_R_GEN	(P)	
12		+S10_VERIFY			
13		+postamble			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB2			
16		LT_PCO?UD	UD_R_GEN		
17		GOTO LB2			
18		+TS_Wait			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB1			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB1			
23		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : S10_NO_RESPONSE_T6
Group : SP/TIMER/
Purpose : Verify that the IUT, at state 10, sends a END PDU when the Timer Timer_NO_RESPONSE is expired .
Configuration :
Default :
Comments : Ref. 7.6 a, Fig. 20(37 of 51)/PICS SP7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			IUT start Timer_NO_RESPONSE
2		START Timer_NO_RESPONSE			
3		?TIMEOUT Timer_NO_RESPONSE			
4		START T_Wait			
5	LB1	LT_PCO?END	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_Wait			

Detailed Comments :

Test Case Dynamic Behaviour

Test Case Name : SP3_MaxPD
Group : SP/PARAM/
Purpose : Check the value of MaxPD system parameter(Maximum number of SD PDUs before transmission of a POLL PDU).
Configuration :
Default :
Comments : Ref. 7.7 c/PICS SP2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(count:=0)			
3	LB1	[count>=Max_PD]		(F)	
4		[count<Max_PD]			
5		<IUT!SD>	SD_R_GEN		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1))	SD_R_GEN		
8		(count:=count+1)			
9		GOTO LB1			
10		LT_PCO?POLL	POLL_R_GEN	(P)	
11		+S10_VERIFY			
12		+postamble			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB2			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB2			
17		+TS_Opr			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : TS_Wait
Group : GENERAL/
Objective : Test Step of alternatives OTHERWISE, and TIMEOUT of T_Wait.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO?OTHERWISE		(F)	
2		+postamble			
3		?TIMEOUT T_Wait		(F)	
4		+postamble			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : TS_Opr
Group : GENERAL/
Objective : Test Step of alternatives OTHERWISE, and TIMEOUT of T_Opr.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO?OTHERWISE		(F)	
2		+postamble			
3		?TIMEOUT T_Opr		(F)	
4		+postamble			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : TS_CC
Group : GENERAL/
Objective : Test Step of alternatives OTHERWISE, and TIMEOUT of Timer_CC.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO?OTHERWISE		(F)	
2		+postamble			
3		?TIMEOUT Timer_CC		(F)	
4		+postamble			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : Initialize_State_Variables
Group : PROCEDURE/
Objective : Procedure used to initialize state variables when new connection is established.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VT_S:=0, VT_PS:=0, VT_A:=0)			
2		(VT_PA:=1, VT_PD:=0)			
3		(VR_R:=0, VR_H:=0)			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : postamble
Group :
Objective : Procedure used to place the IUT at state 1(IDLE) from any state.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!BGREJ	BGREJ_S_GEN		
2		START T_Wait			
3	LB1	?TIMEOUT T_Wait			
4		(count:=0)			
5	LB2	LT_PCO!END(count:=count+1)	END_S_USER		
6		START Timer_CC			
7	LB3	LT_PCO?ENDAK	ENDAK_R_GEN	R	
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB3			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB3			
12		?TIMEOUT Timer_CC			
13		[count < Max_CC]			
14		GOTO LB2			
15		[count >= Max_CC]		I	
16		LT_PCO?OTHERWISE		I	
17		LT_PCO?MD	MD_R_GEN		
18		GOTO LB1			
19		LT_PCO?UD	UD_R_GEN		
20		GOTO LB1			
21		LT_PCO?OTHERWISE		I	

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S1_PREAMBLE
Group : PREAMBLE/
Objective : Procedure used to place the IUT at state 1(IDLE) from any state.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!BGREJ	BGREJ_S_GEN		
2		START T_Wait			
3	LB1	?TIMEOUT T_Wait			
4		(count:=0)			
5	LB2	LT_PCO!END(count:=count+1)	END_S_USER		
6		START Timer_CC			
7	LB3	LT_PCO?ENDAK	ENDAK_R_GEN		
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB3			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB3			
12		?TIMEOUT Timer_CC			
13		[count < Max_CC]			
14		GOTO LB2			
15		[count >= Max_CC]		(I)	
16		LT_PCO?OTHERWISE		(I)	
17		LT_PCO?MD	MD_R_GEN		
18		GOTO LB1			
19		LT_PCO?UD	UD_R_GEN		
20		GOTO LB1			
21		LT_PCO?OTHERWISE		(I)	

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S2_PREAMBLE
Group : PREAMBLE/
Objective : Procedure used to place the IUT at state 2(OUTGOING CONNECTION PENDING) from any state.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		<IUT!BGN>	BGN_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?BGN(VR_SQ:=BIT_TO_INT(BGN.N_SQ), VT_MS:=BIT_TO_INT(BGN.N_MR))	BGN_R_GEN		
5		LT_PCO?MD	MD_R_GEN		
6		GOTO LB1			
7		LT_PCO?UD	UD_R_GEN		
8		GOTO LB1			
9		?TIMEOUT T_Opr		(I)	
10		LT_PCO?OTHERWISE		(I)	

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S4_PREAMBLE
Group : PREAMBLE/
Objective : Procedure used to place the IUT at state 4(OUTGOING DISCONNECTION PENDING) from any state.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!END>	END_R_USER		
3		START T_Opr			
4	LB1	LT_PCO?END	END_R_USER		
5		LT_PCO?POLL	POLL_R_GEN		
6		GOTO LB1			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		?TIMEOUT T_Opr		(I)	
12		LT_PCO?OTHERWISE		(I)	

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S5_PREAMBLE
Group : PREAMBLE/
Objective : Procedure used to place the IUT at state 5(OUTGOING RESYNCHRONIZATION PENDING) from any state.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!RS>	RS_R_GEN		
3		START T_Opr			
4	LB1	LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ), VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_GEN		
5		LT_PCO?POLL	POLL_R_GEN		
6		GOTO LB1			
7		LT_PCO?UD	UD_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		?TIMEOUT T_Opr		(I)	
12		LT_PCO?OTHERWISE		(I)	

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S7_PREAMBLE
Group : PREAMBLE/
Objective : Procedure used to place the IUT at state 7(OUTGOING RECOVERY PENDING) from any state.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN		VT_S=0
3		(VT_S:=INC_MOD_24(VT_S,1))			
4		LT_PCO?SD	SD_S_GEN		VT_S=1
5		(VT_S:=INC_MOD_24(VT_S,1))			
6		LT_PCO!POLL(VT_PS:=INC_MOD_24(VT_PS,1))	POLL_S_N_S(VT_S−2)		VR(H)>POLL.N(S)
7		START T_Wait			
8	LB1	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR))	ER_R_GEN		
9		LT_PCO?POLL	POLL_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		?TIMEOUT T_Wait		(I)	
16		LT_PCO?OTHERWISE		(I)	

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S10_PREAMBLE
Group : PREAMBLE/
Objective : Procedure used to place the IUT at state 10(DATA TRANSFER READY) from any state.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(count:=0)			
3		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
4	LB1	LT_PCO!BGN(count:=count+1)	BGN_S_GEN		
5		START Timer_CC			
6	LB2	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN		
7		+Initialize_State_Variables			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB2			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB2			
12		?TIMEOUT Timer_CC			
13		[count < Max_CC]			
14		GOTO LB1			
15		[count >= Max_CC]		(I)	
16		LT_PCO?OTHERWISE		(I)	

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S1_VERIFY
Group : VERIFY/
Objective : Procedure used to verify that the IUT is at state 1.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!BGAK(VR_MR:=GET_VR_MR())	BGAK_S_GEN		
2		START T_Wait			
3	LB1	LT_PCO?END	END_R_SSCOP	(P)	IUT was at state 1
4		LT_PCO?UD	UD_R_GEN		
5		GOTO LB1			
6		LT_PCO?MD	MD_R_GEN		
7		GOTO LB1			
8		+TS_Wait			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S2_VERIFY
Group : VERIFY/
Objective : Procedure used to verify that the IUT is at state 2.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!BGN(VT_SQ:=INC_MOD_8(VT_SQ, 1), VR_MR:=GET_VR_MR())	BGN_S_GEN		VR(SQ)<>N(SQ)
2		START T_Wait			
3	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN	(P)	IUT was at state 2
4		LT_PCO?UD	UD_R_GEN		
5		GOTO LB1			
6		LT_PCO?MD	MD_R_GEN		
7		GOTO LB1			
8		+TS_Wait			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S4_VERIFY
Group : VERIFY/
Objective : Procedure used to verify that the IUT is at state 4.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_GEN		VR(SQ)=N(SQ)
2		START T_Wait			
3	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN		
4		START T_Wait			
5	LB2	LT_PCO?END	END_R_GEN	(P)	IUT was at state 4
6		LT_PCO?UD	UD_R_GEN		
7		GOTO LB2			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB2			
10		+TS_Wait			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		+TS_Wait			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S5_VERIFY
Group : VERIFY/
Objective : Procedure used to verify that the IUT is at state 5.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!BGN(VR_MR:=GET_VR_MR())	BGN_S_GEN		VR(SQ)=N(SQ)
2		START T_Wait			
3	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN		
4		START T_Wait			
5	LB2	LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ), VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ, VT_MS)	(P)	IUT was at state 5
6		LT_PCO?UD	UD_R_GEN		
7		GOTO LB2			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB2			
10		+TS_Wait			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		+TS_Wait			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S7_VERIFY
Group : VERIFY/
Objective : Procedure used to verify that the IUT is at state 7.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!ER(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())	ER_S_GEN		VR(SQ)<>N(SQ)
2		START T_Wait			
3	LB1	LT_PCO?ERAK(VT_MS:=BIT_TO_INT(ERAK.N_MR))	ERAK_R_GEN	(P)	IUT was at state 7
4		LT_PCO?UD	UD_R_GEN		
5		GOTO LB1			
6		LT_PCO?MD	MD_R_GEN		
7		GOTO LB1			
8		+TS_Wait			

Detailed Comments :

Test Step Dynamic Behaviour

Test Step Name : S10_VERIFY
Group : VERIFY/
Objective : Procedure used to verify that the IUT is at state 10.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!SD	SD_S_N_S(VT_MS+3)		SD.N(S)>=VR(MR), VR(H)<VR(MR)
2		START T_Wait			
3	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT(USTAT.N_MR))	USTAT_R_LIST(VT_S, VT_MS, VT_S)	(P)	
4		LT_PCO?POLL	POLL_R_GEN		
5		GOTO LB1			
6		LT_PCO?UD	UD_R_GEN		
7		GOTO LB1			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		+TS_Wait			

Detailed Comments :