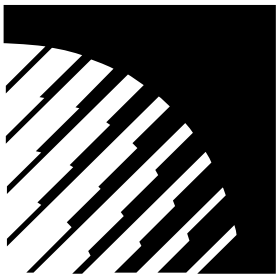

The ATM Forum
Technical Committee

WIRE
Workable Interface
Requirements Example

An example for the Interface at the reference point
between TC and PMD

ATM-Forum Document

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1. General Description

1.1 Scope

This document describes an interface between the TC (Transmission Convergence Layer Device) and the PMD (Physical Media Dependent Device). This is a natural interface as this is the point of change of technology from digital technology supporting moderate clock rates on the TC side to high speed, mixed mode technology on the PMD side.

The interface definition is kept very broad, so many implementations for various data rates can be realized within the same interface description.

PMD and TC sub-layers integrated or interfaced in a different manner will still provide the same service between the media and the SAR layers. On the other hand, there is an obvious benefit in the proliferation of devices that use a common interface mechanism.

2. Functional Description

The interface contains three groups of signals. The Data Group includes data and clock. These are required for the interface to function. The Framing Group may be used to coordinate byte and frame sync. The Signal Loss group may be used by the PMD to indicate loss of media signal.

2.1 Data Group

This group is required for the interface to function. Five configurations are possible, allowing either serial or 8, 16 or 32 bit data busses as well as combining multiple 8 bit busses.

2.1.1 Serial Interface

In this interface implementation, the data and clocks are exchanged in a serial manner. The levels used are PECL or LVDS and require implementation of special analog I/O drivers (or I/O-Arrangements) for the PECL/LVDS levels. In the case of serial PMDs with on-chip PLL, the clock direction is from PMD to TC, like in the parallel interface cases, as the PLL generates the reference clock for the TC. Serial PMDs without PLL, receive the clock from the TC, which is in most cases not used, as the PMD transmit section is really only an analog driver in this case.

2.1.2 8-Bit Parallel Interface

In this interface implementation, the 8-Bit parallel data is provided in a single segment of data from the TC to the PMD and from the PMD to the TC. This will provide for a word-rate of 1/8 bit rate, e.g. 19.44 MHz at a bit rate of 155 Mb/s and 77.76 MHz at a bit rate of 622 Mb/s.

2.1.3 16-Bit Parallel Interface

In this interface implementation, the 16-Bit parallel data is provided in a single segment of data from the TC to the PMD and from the PMD to the TC. This will provide for a word-rate of 1/16 bit rate, e.g. 38.88 MHz at a bit rate of 622 Mb/s.

2.1.4 Quad 8-Bit Parallel Interface

In this interface implementation, the 32-Bit parallel data is provided in a single segment of data from the TC to the PMD for transmission and in four independent 8-Bit parallel data streams for recovery and realignment. This is very important for future realizations of 622 Mb/s data over Unshielded Twisted-Pair. This requires multiple transmission at lower bit rates and re-assembly from these data streams.

2.1.5 32-Bit Parallel Interface

In this interface implementation, the 32-Bit parallel data is provided in a single segment of data from the PMD to the TC for 622 Mb/s transmission of 32-Bit words at 19.44 MHz intervals. The word-rate will increase as the bit rate is increased, like 77.76MHz word-rate for a bit rate of 2.488 GHz.

2.2 Framing Group

This group consists of two optional signals, Out Of Frame (OOF) and Frame Position (FP). At the PMD, a high level OOF is interpreted as a request for the PMD to scan for frame sync patterns and alert the TC by driving FP high when such a pattern is encountered. The PMD establishes byte sync and simplifies detection of frame sync. When the TC is satisfied that frame sync is valid, for example, by the occurrence of two FP indications 125 microseconds apart with no FP indications in between, it brings OOF low to disable the PMD pattern scan. The PMD retains its byte sync phasing as long as OOF is low.

The position within the frame at which FP is generated may be either of two locations: At the third A2 byte or after the last C1 byte of the SONET frame. The method of selecting between these two is implementation specific. This applies to the rates of OC-3 and OC-12.

2.3 Signal Loss Group

This group consists of one signal, Loss Of Signal (LOS). It is an optional signal that can be used to differentiate a vendor's product offering. It is defined here for clarification purposes. If utilized by the PMD, LOS will become active after loss of lock in the Clock and Data Recovery or a contingent time-out of the LOS timer. This provides an early warning to the TC that the received data may be invalid. The TC may respond to an activation of the LOS in any manner appropriate for its framing mechanism. Optionally, the TC may ignore LOS and rely on eventual frame sync loss as defined by the SONET framing specification.

2.4 Signal Description

Table 1 defines the functional signals in the interface. Table 2 shows which the specific signals and bus sizes applicable to each data path configuration.

Signal Name	Direction	Description
TXC	PMD-TC TC-PMD	Clocks TX-Data out of the TC into the PMD (Required) Serial PMDs with PLL provide the clock also to the TC Serial PMDs without PLL receive the clock from the TC
TXD	TC-PMD	Transmit data from TC to PMD (Required)
REFCLK	PMD	Master reference clock for the PMD. (Required)
RXC	PMD-TC	Clocks data into the TC (Required)
RXD	PMD-TC	Receive data from PMD to TC (Required)
OOF	TC-PMD	Requests frame sync pattern scan (Optional)
FP	PMD-TC	Indicates frame sync pattern detection (Optional)
LOS	PMD-TC	Indication that PMD has lost the receive clock. (Optional)

Table 1: Interface Signals between the PMD and the TC devices

	Serial I/F	8-Bit I/F	16-Bit I/F	Quad 8-Bit I/F	32-Bit I/F
TXC	TXCP/TXCN	TXCLK	TXCLK	TXCLK	TXCLK
TXD	TXDP/TXDN	TXD[7..0]	TXD[15..0]	TXD[31..0]	TXD[31..0]
REFCLK		REFCLK	REFCLK	REFCLK	REFCLK
RXC	RXCP/RXCN	RXCLK	RXCLK	RXCLK[3..0]	RXCLK
RXD	RXDP/RXDN	RXD[7..0]	RXD[15..0]	RXD[31..0]	RXD[31..0]
OOF		OOF	OOF	OOF	OOF
FP		FP	FP	FP	FP
LOS		LOS	LOS	LOS[3..0]	LOS

Table 2: Interface Signals For Each Data Path Configuration

3. Signal Timing

In order to scale with higher data rates, most timing parameters are expressed as a percentage of the clock the period. In some cases, absolute minimums are also specified to reasonably reflect performance of typical implementation processes.

3.1 Clock Symmetry

The duty cycle of TX-Clock and RX-Clock should be at least 40 percent and at most 60 percent.

3.2 Transmit Clock Referenced Timing

TX-Data is driven by the TC in response to the reference clock, REFCLK. REFCLK is the jitter attenuated clock out of the PMD. In the case of the master unit, REFCLK is derived from the local Crystal. In the case of the slave unit, REFCLK is derived from the recovered receive clock. The delay, t_X from each rising TX-Clock edge to stability of the resulting TX-Data establishes setup and hold times for the next rising edge of TX-Clock. This delay time should be, at minimum, 20 percent of the TX-Clock period or 2 ns, whichever is smaller and, at maximum, 80 percent of the TX-Clock period.

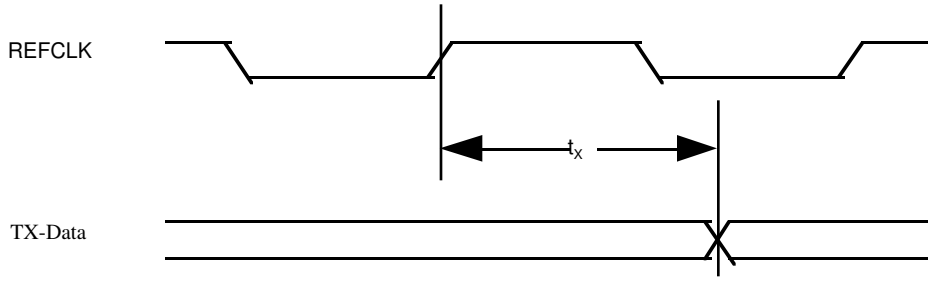

Figure 1: Transmit Clock Referenced Timing

3.3 Receive Clock Referenced Timing

RX-Data and FP are driven by the PMD in coordination with RX-Clock. The PMD is responsible to provide adequate setup and hold times, t_{RS} and t_{RH}. The setup time, t_{RS} , should be a minimum of 40 percent of the RX-Clock period and the hold time, t_{RH}, should be a minimum of 10 percent of RX-Clock period or 2 ns, whichever is less.

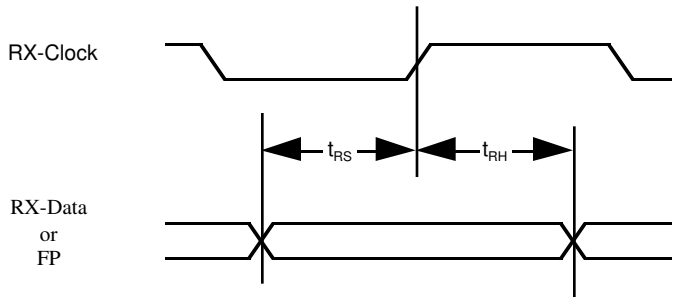

Figure 2: Received Clock Referenced Timing

3.4 OOF timing

The rising edge of OOF is inherently asynchronous. It is brought high on initialization or when the TC recognizes that there is no known reference to receive frames. The falling edge is only

affected after a stability period of at least two 125 microsecond frames. If the system remains stable, OOF will not have meaning for most of another 125 microsecond frame period. Data instability during or after falling of OOF will result in the same frame error detection by the TC so the time that OOF becomes low is immaterial.

4. Timing Sequences

4.1 Frame Detect Timing

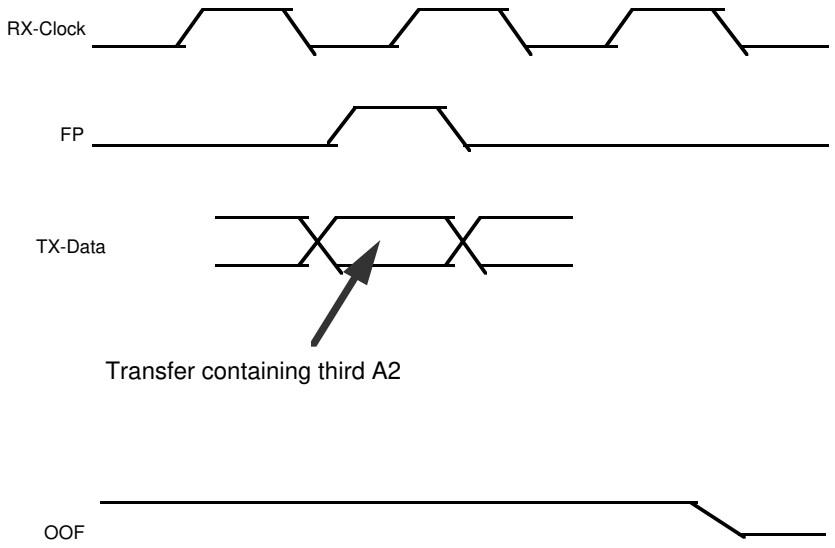

Figure 3: Frame Detect Timing

4.2 Serial Interface

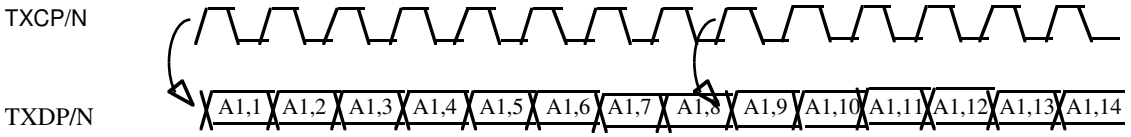

Figure 4: Serial Transmit Side Timing From TC To PMD

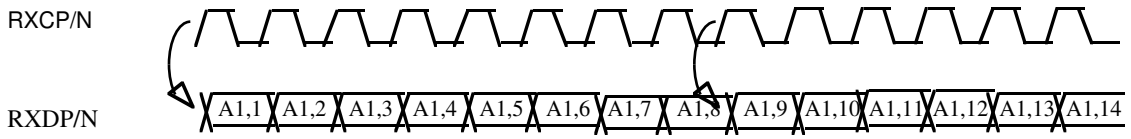

Figure 5: Serial Receive Side Timing From PMD To TC

4.3 8-bit Parallel Interface

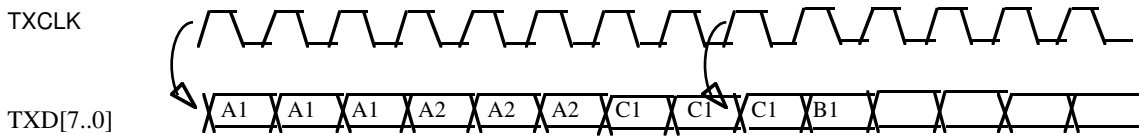

Figure 6: 8 Bit Transmit Side Timing From TC To PMD

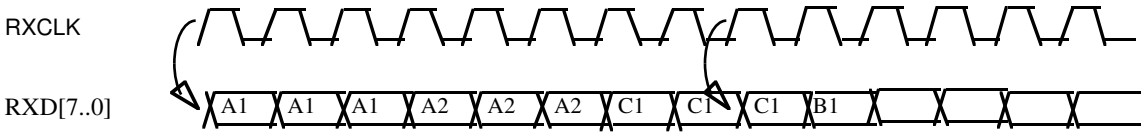

Figure 7: 8 Bit Receive Side Timing From PMD To TC

4.4 16-bit Parallel Interface

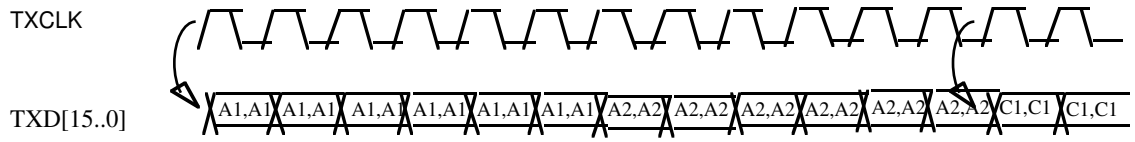

Figure 8: 16 Bit Transmit Side Timing From TC To PMD

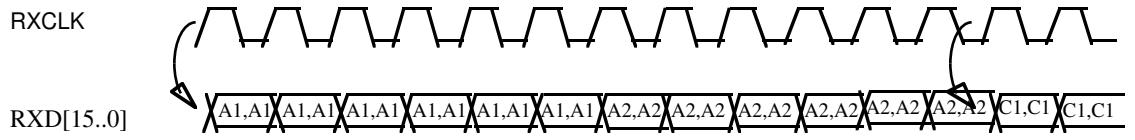

Figure 9: 16 Bit Receive Side Timing From PMD To TC

4.5 Quad 8-bit Parallel Interface

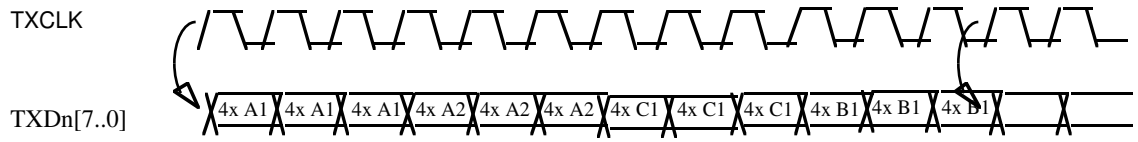

Figure 10: Quad 8 Bit Transmit Side Timing From TC To PMD

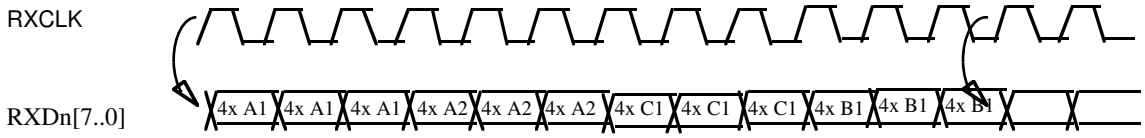

Figure 11: Quad 8 Bit Receive Side Timing From PMD To TC

4.6 32-bit Parallel Interface

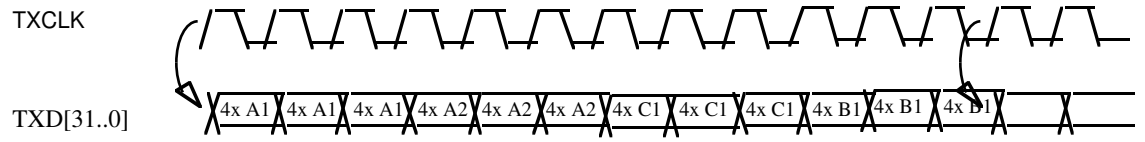

Figure 12: 32 Bit Transmit Side Timing From TC To PMD

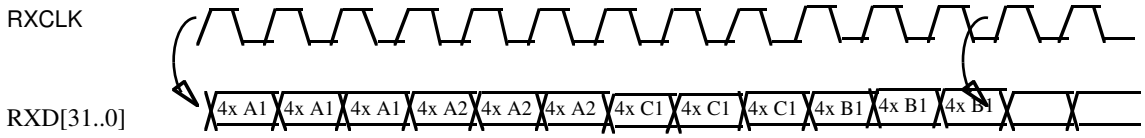

Figure 13: 32 Bit Receive Side Timing From PMD To TC

5. Application Examples

Figures 14, 15 and 16 illustrate connections, signal flow and possible architectures for a serial interface environment.

Figures 17 and 18 illustrate connections, signal flow and possible architectures for a parallel interface environment.

Note that an end unit device derives its clock from the network. A network device derives its clock from either a network device closer to the master clock source or from its own reference oscillator.

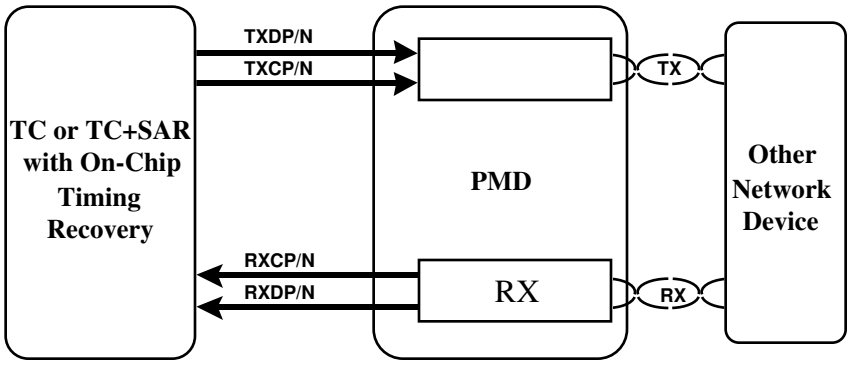

Figure 14: Serial Interface Setup for PMD without Timing Recovery

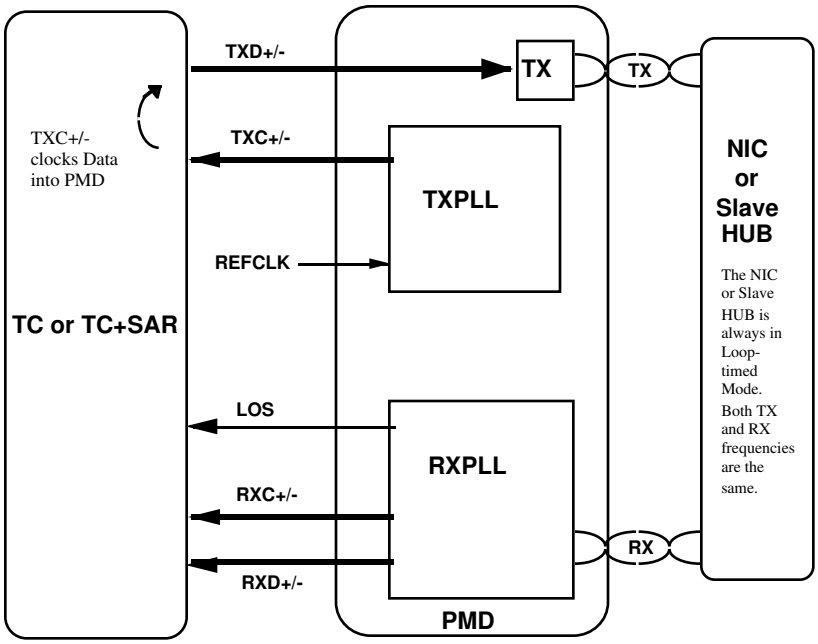

Figure 15: Serial Interface Setup Network Unit (Clock Master)

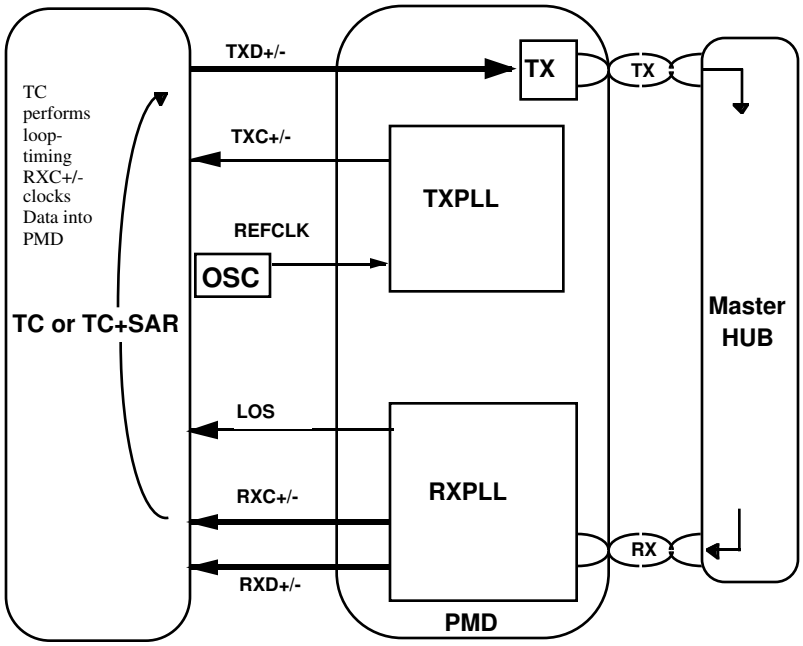

Figure 16: Serial Interface Setup End Unit (Clock Slave)

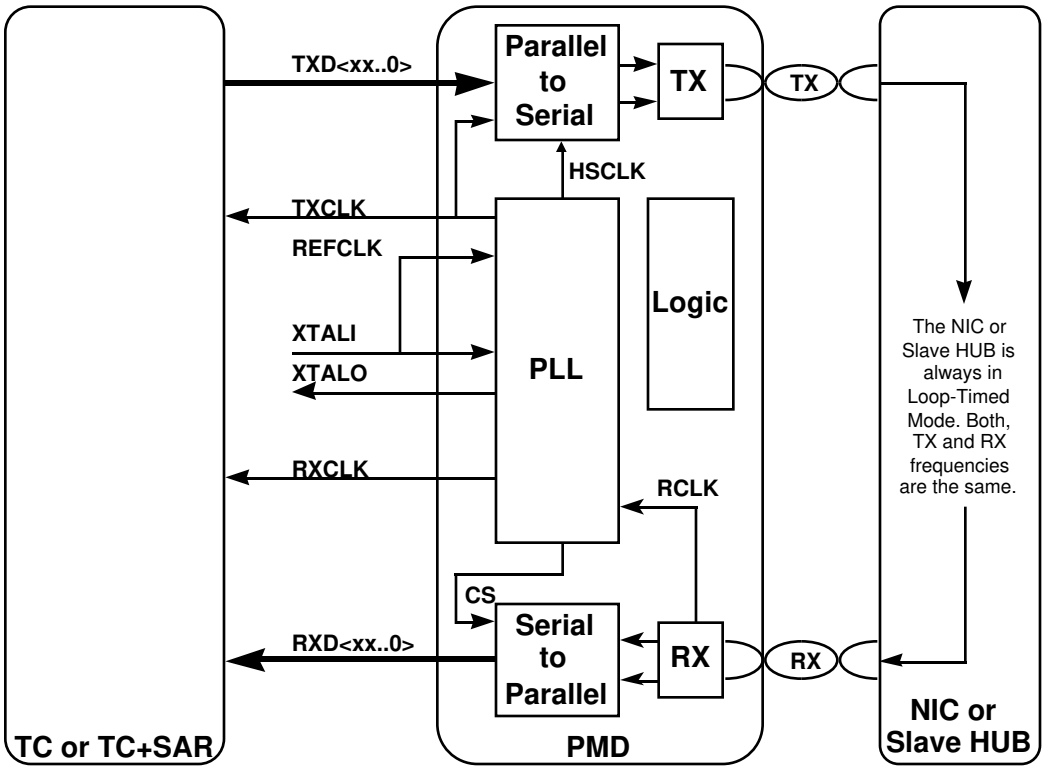

Figure 17: Parallel Interface Setup Network Unit (Clock Master)

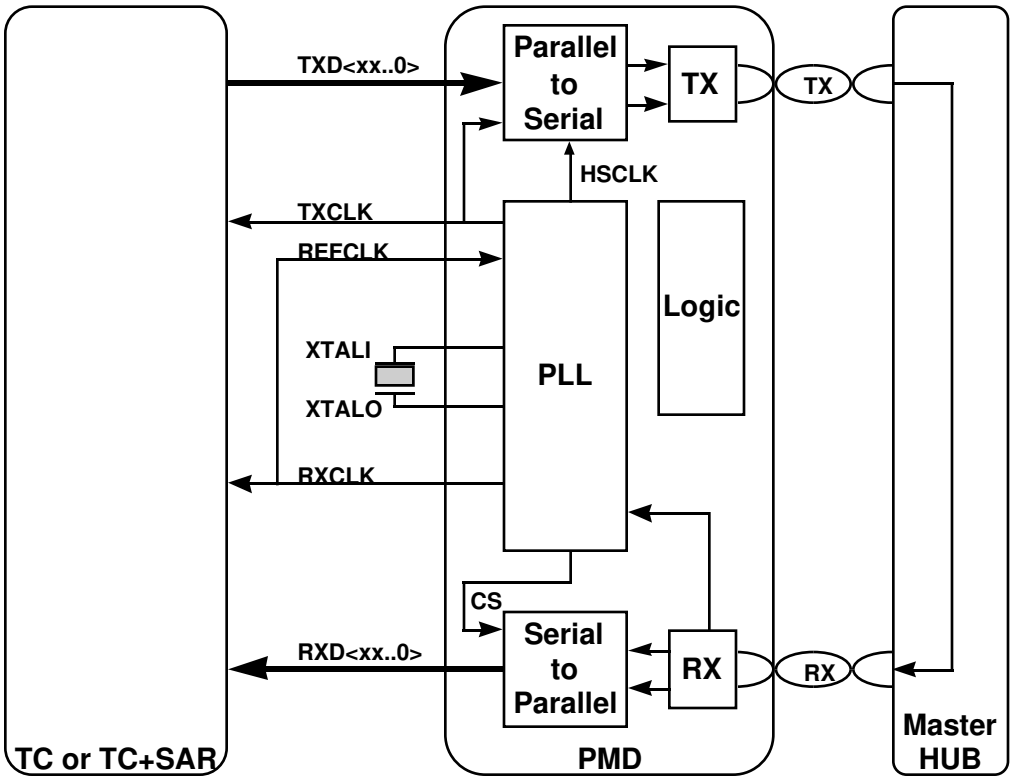

Figure 18: Parallel Interface Setup End Unit (Clock Slave)