The ATM Forum
Technical Committee

DS3 Physical Layer Interface Specification

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Annex

DS3/ATM Physical Layer Interface Specification
Version 4.0

1. Introduction

This document supersedes "Section 2.2 DS3 Physical Layer Interface" of ATM User-Network Interface Specification, Version 3.0, PTR Prentice Hall, 1993 and Version 3.1, PTR Prentice Hall, 1995. It describes the Physical Layer specifications for DS3 transmission systems used for ATM.

Two different mappings have been specified for transporting ATM cells over DS3 transmission systems, namely, a PLCP-based system and a direct mapped system. The two mappings are not compatible although both use the C-Bit Parity application of DS3 as the underlying transmission system.

For new implementations, the direct mapped version is preferred. However, the need to support existing implementations as previously defined in ANSI T1.624-1993, "Broadband ISDN User-Network Interfaces - Rates and Formats Specifications" (i.e., those utilizing PLCP-based mapping) should be taken into account by network operators and manufacturers (e.g., as a subscription option).

2. Physical Media Dependent Sublayer

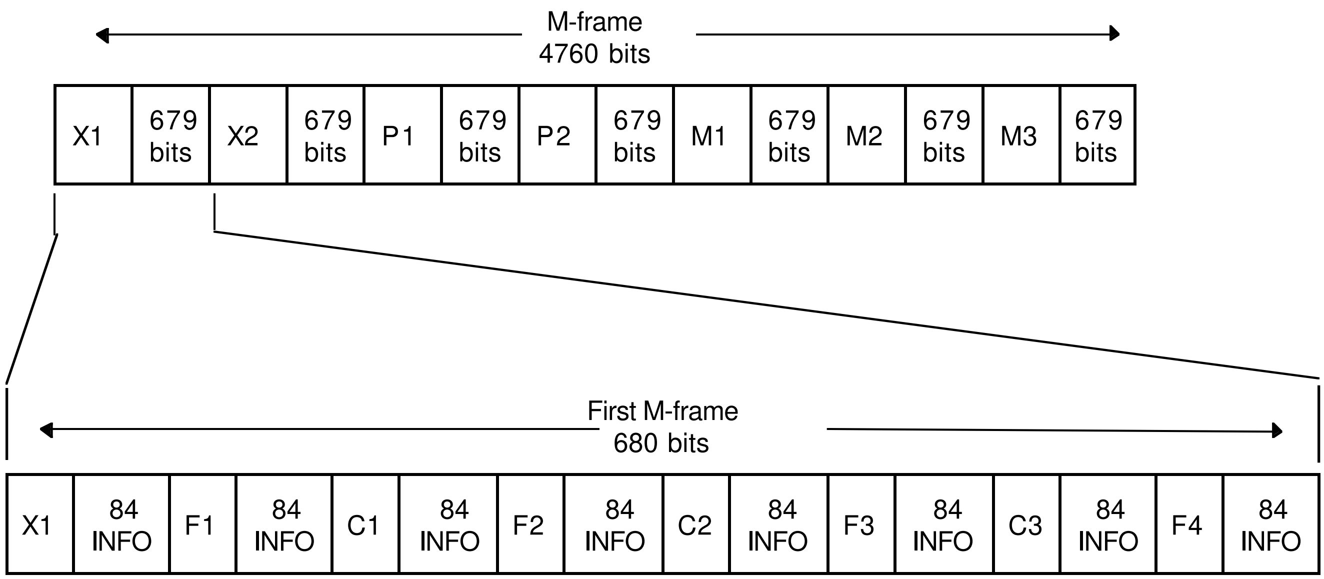
(R) The text of clause 9, Physical layer characteristics at 44.736 Mbit/s (DS3/ATM with direct mapping), from ANSI T1.646-1995, "Broadband ISDN - Physical Layer Specification for User-Network Interfaces Including DS1/ATM" shall apply as the preferred choice for transmission of ATM cells using DS3 equipment.

3. Transmission Convergence Sublayer

C-Bit Parity is an application of the basic DS3 framing format and is described in ANSI T1.107-1995, "Digital Hierarchy - Formats Specifications" and ANSI T1.404-1994, "Network-to-Customer Installation - DS3 Metallic Interface Specification".

The format is shown in Figure 1. Transmission is from left to right. ATM cells are directly mapped into the information payload; cells are nibble aligned and inserted as consecutive bits into consecutive 84-bit Info fields. Cells may start on any nibble boundary within any 84-bit Info field and may cross M-frame boundaries.

The ATM cell transfer capacity (for user information cells, signaling cells, OAM cells, and cells used for cell rate decoupling) is approximately 44.21 Mbit/s.



Overhead Bit Designation within M-subframes								
M-subframe 1	X1	F1	C1	F2	C2	F3	C3	F4
M-subframe 2	X2	F1	C1	F2	C2	F3	C3	F4
M-subframe 3	P1	F1	C1	F2	C2	F3	C3	F4
M-subframe 4	P2	F1	C1	F2	C2	F3	C3	F4
M-subframe 5	M1	F1	C1	F2	C2	F3	C3	F4
M-subframe 6	M2	F1	C1	F2	C2	F3	C3	F4
M-subframe 7	M3	F1	C1	F2	C2	F3	C3	F4

Notes:
1) See ANSI T1.107 for description of X1, X2, P1, and P2 bits.
2) The M-frame alignment signal shall be M1=0, M2=1, and M3=0.
3) The M-subframe alignment signal shall be F1=1, F2=0, F3=0, and F4=1.
4) C1, C2, and C3 bits shall be assigned according to ANSI T1.404 for the C-Bit Parity application.

Figure 1: DS3 C-Bit Parity Frame Format

For cell rate decoupling, the Physical Layer shall adapt the cell rate arriving from the ATM Layer to the payload capacity of the DS3 frame by inserting idle cells when assigned or unassigned cells are not available from the ATM layer. Idle cells shall have the header as shown in Figure 2. The content of idle cells shall be “0110 1010” repeated 48 times.

Octet 1	Octet 2	Octet 3	Octet 4	Octet 5
0000 0000	0000 0000	0000 0000	0000 0001	“the correct HEC”

Figure 2: Header Pattern for Idle Cells

Cell rate decoupling may be performed at the ATM Layer in which case unassigned cells shall be used and not idle cells as described in ANSI T1.627-1993, “Broadband ISDN - ATM Layer Functionality and Specification.” The idle cell[1] as defined here has an invalid cell header pattern. Idle cells shall not be passed to the ATM Layer.

(R) HEC generation, HEC check, self-synchronizing scrambler, cell delineation, cell rate decoupling shall be as described in ANSI T1.646 and ITU-T Recommendation I.432, i.e., the usual, ATM/B-ISDN related functionality.

(R) The electrical characteristics shall be as described in ANSI T1.646.

The physical media consists of two coaxial cables. A test load of 75 ohms ±5% is used to evaluate the electrical parameters. The line coding is B3ZS. Note that there are differences in specifying the electrical parameters depending on whether the interface is the Network Interface or is within the Customer Installation. ANSI T1.404 and ANSI T1.102-1993, “Telecommunications - Digital Hierarchy - Electrical Interfaces” are applicable for technical guidance.

The interface shall be symmetric, i.e., the bit rate shall be the same in both directions. The nominal line rate shall be 44.736 Mbit/s. Timing shall be traceable to a Primary Reference Source as specific in ANSI T1.101-1994, “Synchronization Interface Standard”. When timing is not synchronized, e.g., when synchronization with the network is lost, the tolerance shall be ± 20 ppm.

4. References

ATM User-Network Interface Specification, Versions 3.0, PTR Prentice Hall, 1993

ATM User-Network Interface Specification, Versions 3.1, PTR Prentice Hall, 1995

ANSI T1.624-1993, “Broadband ISDN User-Network Interfaces - Rates and Formats Specifications”

[1] ANSI T1.627 does not currently recognize idle cells for cell rate decoupling. The use of idle cells requires the ATM Layer to accept a non-continuous cell stream from the Physical Layer.

ANSI T1.646-1995, “Broadband ISDN - Physical Layer Specification for User-Network Interfaces Including DS1/ATM”

ANSI T1.107-1995, “Digital Hierarchy - Formats Specifications”

ANSI T1.404-1994, “Network-to-Customer Installation - DS3 Metallic Interface Specification”

ANSI T1.627-1993, “Broadband ISDN - ATM Layer Functionality and Specification”

ITU-T Recommendation I.432, “B-ISDN User-Network Interface - Physical Layer Specification,” 1993

ANSI T1.102-1993, “Telecommunications - Digital Hierarchy - Electrical Interfaces”

ANSI T1.101-1994, “Synchronization Interface Standard”

Annex A

This section is based on specifications in ANSI T1.646-1995, “Broadband ISDN - Physical Layer Specification for User-Network Interfaces Including DS1/ATM” for B-ISDN interfaces. The functions of the DS3 Physical Layer are grouped into Physical Media Dependent (PMD) Sublayer and the Transmission Convergence (TC) Sublayer as shown in Figure A.1.

Transmission Convergence Sublayer	HEC Generation/Verification PLCP Framing and Cell Delineation Path Overhead Utilization PLCP Timing (125 µs clock recovery) Nibble Stuffing
Physical Media Dependent	Bit Timing, Line Coding Physical Medium

Figure A.1: Physical Layer Functions

INTRODUCTION

Equipment designed to the specifications in The ATM User-Network Interface Specification, Versions 3.0 and 3.1, use a Physical Layer Convergence Protocol (PLCP) format to carry ATM cells.

(R) If the PLCP version of DS3 is used, the 44.736 Mbit/s interface shall comply with the specifications as referenced in this section.

Physical Media Dependent Sublayer

The interface at the Physical Layer is based on asynchronous DS3 using the C-bit Parity application as described in Annex A, “Physical layer characteristics at 44.736 Mbit/s (DS3/ATM with PLCP),” of ANSI T1.646-1995. ANSI T1.646 uses ANSI T1.404-1994, “Network-to-Customer Installation - DS3 Metallic Interface Specification,” as a primary reference.

Format at 44.736 Mbit/s

To carry ATM traffic over existing DS3 communications facilities, a Physical Layer Convergence Protocol (PLCP) for DS3 is defined in ANSI T1.646. This PLCP is a subset of the PLCP originally defined in IEEE 802.6. Mapping of ATM cells into the DS3 format is accomplished by first inserting the 53 octet ATM cells into the DS3 PLCP payload (see Figure A.2). The PLCP is then mapped into the DS3 information payload.

Extraction of ATM cells from the DS3 format operates by framing on the PLCP and then extracting the ATM cells from the PLCP payload.

PLCP Framing		POI	POH	PLCP Payload	
A1	A2	P11	Z6	First ATM Cell	
A1	A2	P10	Z5	Second ATM Cell	
A1	A2	P9	Z4		
A1	A2	P8	Z3		
A1	A2	P7	Z2	Succeeding	
A1	A2	P6	Z1	ATM	
A1	A2	P5	X	Cells	
A1	A2	P4	B1		
A1	A2	P3	G1		
A1	A2	P2	X		
A1	A2	P1	X		
A1	A2	P0	C1	Twelfth ATM Cell	Trailer
1 Octet	1 Octet	1 Octet	1 Octet	53 Octets	13 or 14 Nibbles

POI - Path Overhead Identifier
POH - Path Overhead
X - Unassigned

Figure A.2: DS3 PLCP Frame (125 μs)

PLCP Format

The ATM Physical Layer PLCP for DS3 defines the mapping of ATM cells onto existing DS3 facilities.

(R) The DS3 PLCP frame format (Figure A.2) shall consist of 12 rows by 57 octets with the last row containing a trailer of 13 or 14 nibbles. This format allows a DS3 PLCP frame to carry 12 ATM cells. The DS3 PLCP frame shall have a nominal duration of 125 µs and is transmitted at a nominal rate of 44.210 Mbit/s. PLCP nibble stuffing is required after the twelfth cell to frequency justify the 125 µs PLCP frame.

(R) The DS3 PLCP frame shall be mapped into the DS3 information payload at nibble boundaries. DS3 nibble bounders shall start at every control bit (F, X, P, C, or M) of the DS3 frame. Note that there is no predefined relationship between the start of the DS3 frame and the start of the DS3 PLCP frame.

Octets comprising the DS3 PLCP frame are described in the following sections.

Order of transmission of all PLCP bits is from left to right and top to bottom. Each octet has the most significant bit on the left and the least significant bit on the right.

PLCP Overhead Utilization

(R) The following PLCP overhead octets/nibbles are required to support the coding/functions (as defined) across the UNI.

- A1 - Frame Alignment
- A2 - Frame Alignment
- B1 - Bit Interleaved Parity
- C1 - Cycle/Stuff Counter
- G1 - PLCP Path Status
- Px - Path Overhead Identifier
- Zx - Growth Octets
- Trailer Nibbles

Framing Octets (A1, A2)

The PLCP framing octets use the same framing pattern as in SONET and SDH.

(R) The octets are defined as A1 = 1111 0110 and A2 = 0010 1000.

Bit Interleaved Parity - (B1)

The Bit Interleaved Parity - 8 (BIP-8) supports path error monitoring.

(R) The BIP-8 shall be calculated over the 12 x 54 octet structure consisting of the Path overhead (POH) field and the associated ATM cells (648 octets) of the previous PLCP frame and be inserted in the B1 octet. The n^{th} bit of B1 provides even parity over the n^{th} bits of the 648 octets of the 12 x 54 octet structure.

Cycle/Stuff Counter (C1)

The Cycle/Stuff Counter provides a nibble stuffing opportunity cycle and length indicator for the PLCP frame. A stuffing opportunity occurs every third frame of a 3 frame (375 µs) stuffing cycle.

(R) A Trailer of 13 nibbles shall be used in the first frame of the 3 frame stuffing cycle. A Trailer of 14 nibbles shall be used in the second frame of the 3 frame stuffing cycle. The Trailer of the third frame shall contain 14 nibbles if a stuff occurs and 13 nibbles if no stuff occurs. The value of the C1 octet is used as an indication of the phase of the 3 frame stuffing opportunity cycle (see Figure A.3).

C1 Code	Phase of 3 Frame Stuffing Cycle	Trailer Length
1111 1111	1	13
0000 0000	2	14
1001 1001	3 (stuff occurs)	14
0110 0110	3 (no stuff occurs)	13

Figure A.3: Cycle/Stuff Counter Designation

Trailer Nibbles

(R) The value of each of the nibbles in the Trailer shall be 1100.

PLCP Path Status (G1)

Figure A.4 illustrates the G1 octet subfields: a 4-bit Far End Block Error (FEBE), a 1-bit RAI (Yellow), and 3 X bits (X bits are ignored).

(R) Octet G1 contains a 4-bit Far End Block Error (FEBE) and a 1-bit Remote Alarm Indication (RAI) as shown in Figure A.4.

(R) FEBE shall provide a count of BIP-8 errors (ranging from 0000 to 1000) received in the previous frame. If the FEBE function is not implemented, those 4 bits shall be 1111. Values other than those in the range 0000 - 1000 shall be interpreted as 0 errors.

(R) RAI(Yellow) is used to alert the transmitting PLCP that a received failure has been declared along the path. When an incoming failure condition is detected and persists for a "soaking period" (typically 2-10 seconds), an RAI shall be sent to the far end by setting G1(RAI) = 1. The RAI shall be detected at the far end when G1(RAI) = 1 for 10 consecutive PLCP frames. When the incoming failure has ceased for 15 ± 5 sec, the failure indication is cleared by setting G1(RAI) = 0. At the receiving end removal of RAI is recognized when G1(RAI) = 0 for 10 consecutive frames.

(R) X bits are ignored by the receiver.

FEBE	RAI	X
4 Bits	1 Bit	3 Bits

Figure A.4: PLCP Path Status (G1) Definition

Path Overhead Identifier (P0-P11)

The POI identifies the adjacent POH octets.

(R) The POI and POH shall have the relationship defined in Figure A.5.

POI	POI Code	Associated POH
P11	0010 1100	Z6
P10	0010 1001	Z5
P9	0010 0101	Z4
P8	0010 0000	Z3
P7	0001 1100	Z2
P6	0001 1001	Z1
P5	0001 0101	X
P4	0001 0000	B1
P3	0000 1101	G1
P2	0000 1000	X
P1	0000 0100	X
P0	0000 0001	C1

Figure A.5: POI Code Definition

Growth Octets (Z1-Z6)

Growth octets are reserved for future use.

(R) The Growth octets Z1 - Z6 shall be set to 0000 0000 by the transmitter and shall be ignored by the receiver.

ATM TRANSFER CAPABILITY

Because of the overhead of the PLCP, the nominal bit rate available for the transport of ATM cells in the DS3 PLCP is 40.704 Mbit/s.

TIMING

(R) The PLCP frame from network equipment to the customer shall have timing traceable to a Primary Reference Source (PRS).

(R) The PLCP from the customer to the network shall have timing traceable to a PRS. The customer equipment may use the clock recovered from the network PLCP or other source traceable to a PRS.

CELL PAYLOAD SCRAMBLING

(R) The DS3 PLCP interface shall use the self-synchronizing scrambler described in ITU-T Recommendation I.432 and designated as $X^{43} + 1$.

(O) Because of existing equipment, the Cell Payload Scrambler may have the capability of being enabled or disabled. As a configurable option, the Cell Payload Scrambler may be disabled.

CELL DELINEATION

Cell delineation is prescribed by the PLCP frame.

CELL GENERATION/VERIFICATION

The Header Error Control (HEC) covers the entire cell header. Support of bit error detection is mandatory.

The transmitter calculates the HEC value for the first four octets of the cell header, and inserts the results into HEC field, the last octet of the header. The HEC field shall be an 8-bit sequence. It shall be the remainder of the division (modulo 2) by the generator polynomial $x^8 + x^2 + x + 1$ of the polynomial x^8 multiplied by the content of the header excluding the HEC field. A coset with the pattern “0101 0101” is XORed with the 8-bit remainder before being inserted in the last octet of the header as in ITU-T Recommendation I.432.

(R) Equipment supporting the UNI shall implement HEC error detection as defined in ITU-T Recommendation I.432.

(O) Equipment supporting the UNI may also implement single bit error correction in addition to error detection. In this case, the two modes of operation shall interact in accordance to the procedure defined in ITU-T Recommendation I.432.

(R) Equipment supporting the UNI shall generate the HEC octet as described in ITU-T Recommendation I.432.

(R) The generator polynomial and coset used shall be in accordance with ITU-T Recommendation I.432.