# The ATM Forum
## Technical Committee

# DS1 Physical Layer Specification

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# The ATM Forum Technical Committee DS1 Physical Layer Specification

## Preface

Since the publication of The ATM Forum ATM User-Network Interface Specification, Version 3.0 (UNI 3.0), the ATM Forum Technical Committee has completed the specification of additional physical layer interface agreements. These additional interfaces are:

- ATM Physical Medium Dependent Interface Specification for 155 Mb/s over Twisted Pair Cable
- Mid-range Physical Layer Specification for Category 3 Unshielded Twisted Pair
- DS1 Physical Layer Specification

This document contains the DS1 Physical Layer Specification.

## Acknowledgement

The assistance of John Jaeger who provided source material for this document is appreciated. Without his efforts this document could not have been assembled.

The material submitted is based upon documents that have been edited at various times by Daun Langston, Ken Brinkerhoff, Moshe DeLeon, Stanley Ooi, and David. Their assitance as well as all the members of The ATM Forum who have brought contributions towards, discussed and reviewed the enclosed information is appreciated.

Greg Ratta, Chief Editor

# The ATM Forum Technical Committee DS1 Physical Layer Specification

## 1 Introduction Introduction

This DS1 ATM UNI specification for a 1.544 Mbps interface rate is based on ANSI T1 (T1E1 LB 93-05) and ITU (G.804) documents to maintain consistency with existing standards for ATM over DS1.

This specification applies to the public UNI only. It is intended to operate over clear channel (transparent T 1) facilities.

## 2 Physical Media Dependent (PMD)Characteristics Physical Media Dependent (PMD)Characteristics

(R) The DS1 ATM UNI shall meet the PMD characteristics of Ia at the U reference point as specified in ANSI T1.408 Sections 5.2, 5.3.3, 5.4 -5.4.2.3, 5.5 and 5.6.1.

Specific implementation requirements, especially regarding the ESF Data Link, are related to selection of the interface at Ia of the U reference point in ANSI T1.408.

### 2.1 Interface Bit Rate.1 Interface Bit Rate

(R) The physical layer bit rate at the DS1 ATM UNI shall be nominally 1.544 Mbps.

### 2.2 ATM Transfer Rate.2 ATM Transfer Rate

(R) The nominal bit rate available for transport of ATM cells (user information cells, signaling cells and ATM higher layer OAM information cells) shall be 1.536 Mbps.

### 2.3 Interface Symmetry.3 Interface Symmetry

(R) The DS1 ATM UNI is symmetric (i.e. it provides the same 1.544 Mbps nominal bit rate in both transmission directions).

### 2.4 Synchronization.4 Synchronization

(R) The DS 1 ATM UNI shall meet the synchronization characteristics of Ia at the U reference point as described in ANSI T1.408 Sections 5.3.1.1 - 5.3.1.2.1 for public network access applications and Section 5.3.1.2.3 for leased line applications.

### 2.5 Line Code.5 Line Code

(R) The line code used on the DS1 ATM UNI shall be Bipolar 8 Zero Substitution (B8ZS) as specified in ANSI T1.408 Section 5.3.2 (excluding ZBTSI or interim solutions).

# 3 Transport Signal Format Transport Signal Format

## 3.1 Frame Format.1 Frame Format

(R) The physical layer interface format shall be the 24 frame multiframe Extended Superframe Format (ESF) for DS1 as defined in ANSI T1.408 Sections 6.1 - 6.3 and 7 (excluding ZBTSI).

## 3.2 ESF Maintenance Functions.2 ESF Maintenance Functions

This section is consistent with the required message-oriented and bit-oriented messages of ANSI T1.408 Section 8.

**(R)** The DS1 ATM UNI shall provide bit-oriented alarm messages of the ESF Data Link as specified in ANSI T1.408 Sections 8.1 and 8.2.

**(R)** The DS1 ATM UNI shall provide bit-oriented loopback messages of the ESF Data Link as specified in ANSI T1.408 Sections 8.3 (including Annex EPT FS and Ia FS required functions) and 8.3.1, 8.3.3 and 8.3.4.

**(R)** The DS1 ATM UNI shall provide the above bit-oriented messages in accordance with the conditions of the ESF Data Link as described in ANSI T1.408 Sections 8.4.1 - 8.4.2.2.

**(R)** The DS1 ATM UNI shall provide the message-oriented performance report messages of the ESF Data Link as specified in ANSI T1.408 Sections 8.4.3.1 - 8.4.3.1.2. These performance report messages shall have the format and meet the conditions described in ANSI T1.408 Sections 8.4.3.2 - 8.4.5.

# 4 Transmission Convergence (TC)Characteristics Transmission Convergence (TC)Characteristics

## 4.1 ATM Cell Mapping.1 ATM Cell Mapping

(R) ATM cells shall be carried in the DS1 payload (bits 2 -193), in accordance with ITU G.804 Section 2.1, by utilizing the direct mapping as shown by Figure 2-1. ATM cells are byte-aligned to the DS1 frame.

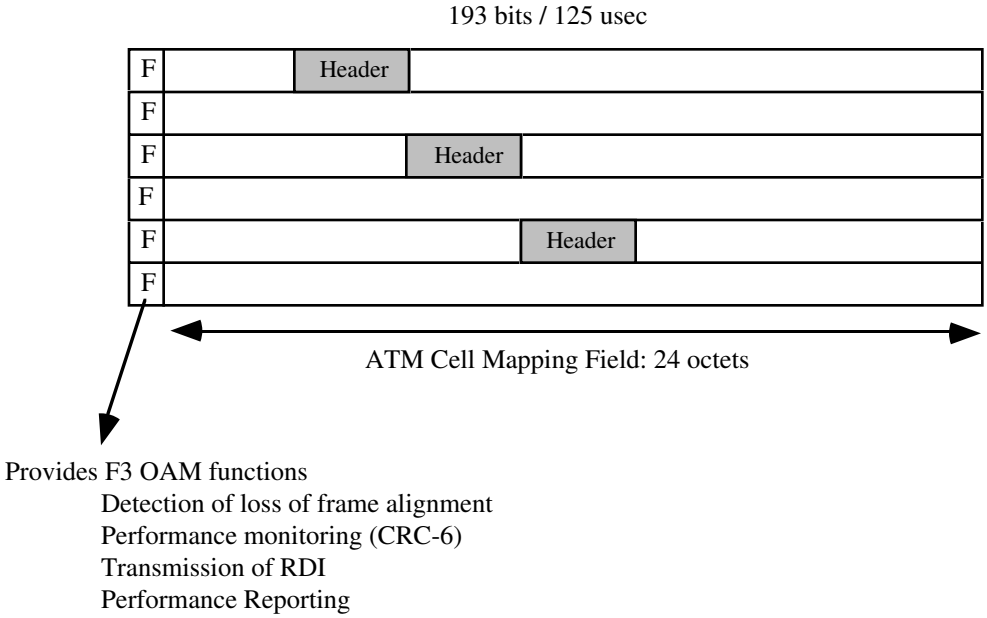


**Figure 4-1 ATM Cell Mapping4-1 ATM Cell Mapping**

## 4.2 Cell Rate Decoupling[1] .2 Cell Rate Decoupling[1]

(R) On the transmit side, the DS1 ATM UNI physical layer interface shall adapt the cell rate arriving from the ATM layer to the DS1 frame payload capacity by inserting unassigned or idle cells when assigned cells are not available from the ATM layer.

**(R)** The receive side of the interface shall be able to receive and filter unassigned cells and idle cells.

In the case that Generic Flow Control (GFC) is supported, the transmit side shall use unassigned cells when assigned cells are not available from the ATM layer.

The use of idle cells is described in ITU I.432 Section 4.4. The use of unassigned cells is described in ANSI T1.627 Sections 7.5.3 and 10.12 - 10.13 as well as ITU I.361.

## 4.3 Cell Delineation.3 Cell Delineation

(R) The cell delineation function shall be performed using the HEC mechanism as defined in ITU I.432 Section 4.5. Payload scrambling shall not be used.

## 4.4 HEC Generation/Verification.4 HEC Generation/Verification

The Header Error Control (HEC) covers the entire cell header.

**(R)** The HEC shall be generated as described in ITU I.432 Section 4.3.2.

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[1] See Section 3.4.2 on Cell Rate Decoupling in the ATM Forum UNI version 3.1 for further information regarding unassigned and assigned cells.

**(R)** The generator polynomial and coset used shall be in accordance with ITU I.432 Section 4.3.2.

**(R)** HEC error detection as defined in ITU I.432 Sections 4.3.1 - 4.3.2 shall be implemented.

**(O)** Single bit error correction may be implemented in addition to error detection. In this case, the two modes of operation shall interact in accordance with procedures defined in ITU I.432 Section 4.3.1.